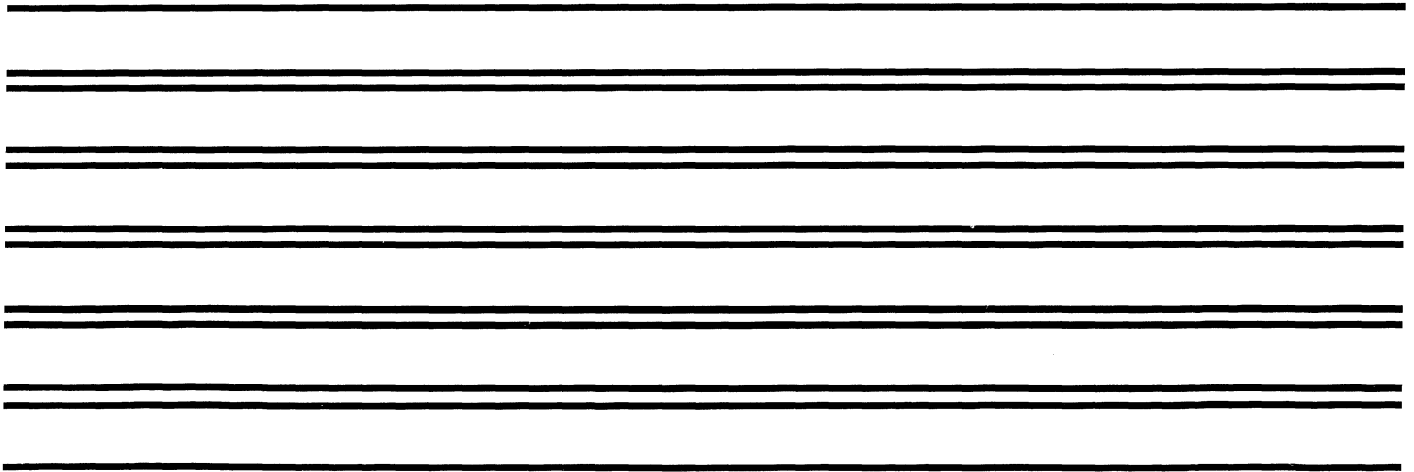


**SIGNETICS
LOGIC-TTL**

**DATA
MANUAL**



Edited by
Pat Kawakami and Rick McCarthy

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Signetics would like to thank you for your interest in our products. We hope you find the product information you need on the TTL data sheets contained in this data manual. The information is presented in a concise and consistent format for easy device and parameter location.

This manual contains product information on most of the Signetics TTL Logic devices. The majority of this book is dedicated to the four 54/74 families of products, i.e. 54/74, 54H/74H, 54S/74S and 54LS/74LS. The 54/74 data sheets in Section 3 are presented in numerical order for easy location. Each data sheet contains the unique dc and ac data for all of the 54/74 families covered by that device type. Family dc data, or that data which characterizes each family, is presented on the inside front and back covers, and also on a fold out in the back of the book. Any deviation from these family characteristics is contained on the individual data sheets.

The 8200 and 9300 MSI functions are presented in Sections 5 and 6 respectively. These data sheets are generally self contained with all pertinent dc and ac data included. The 82S00 products are included along with the associated 8200 device types. A number of TTL compatible interface devices are presented as the "8T" products in Section 7. These 8T products are being included primarily for reference, and more complete data sheets will be presented in an Interface Manual at a later date.

This book contains a compilation of most TTL products currently available. Signetics is continually developing new products. As you see new product announcements, you should contact your local Signetics sales office, representative or authorized distributor or write Signetics, c/o Information Services at 811 East Arques Avenue, P.O. Box 9052, Sunnyvale, California 94086, for the latest technical information.

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82S50	Binary-to-Octal Decoder	557
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82S51	BCD-to-Decimal Decoder	557
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82S52	BCD-to-Decimal Decoder	557
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8263	3-Input 4-Bit Digital Multiplexer	563
8264	3-Input 4-Bit Digital Multiplexer	563
8266	2-Input 4-Bit Digital Multiplexer	566
82S66	2-Input 4-Bit Digital Multiplexer	566
8267	2-Input 4-Bit Digital Multiplexer	566
82S67	2-Input 4-Bit Digital Multiplexer	566
8270	4-Bit Register	569
82S70	4-Bit Register	569
8271	4-Bit Register	569
82S71	4-Bit Register	569
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8274	10-Bit Serial-In Parallel-Out Shift Register	576
8277	Dual 8-Bit Shift Register	579
8280	BCD Decade Counter/Storage Element	581
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82582	4-Bit BCD Arithmetic Unit	586
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82S90	Presetable High Speed Decade Counter	594
8291	Presetable High Speed Binary Counter	594
82S91	Presetable High Speed Binary Counter	594
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NUMERICAL INDEX (Cont'd)

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9308	Dual 4-Bit Latch	611
9309	Dual 4-Input Multiplexer	615
9314	4-Bit Transparent Latch	618
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8T30	Dual TTL/DTL to MOS Transceiver/Port Controller	687
8T31	8-Bit Bidirectional Port	692
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8T380	Quad Bus Receiver with Hysteresis-Schmitt Trigger	720

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		Std.	S	LS		
Adder	80	X			1+1+Carry	121
Adders	83	X		X	4+4+Carry	124
Adders	283			X	4+4+Carry	421
Adder	—	—	— 82S83 —	—	4-Bit BCD	590
Arithmetic logic unit	—	—	— 82S82 —	—	4-Bit BCD	586
Arithmetic logic unit	181	X	X	X	4-Bit Binary	314
Carry lookahead unit	182	X	X		Lookahead over 16-Bits	320
Comparator magnitude	85	X	X	X	4	128
Encoder, priority	147	X			10-to-4	217
Encoder, priority	148	X			8-to-3	220
Multiply decoder	261			X	2X2	408
Parity generator/checker	180	X			8-Bit Odd/Even	311
Parity generator/checker	280		X		8-Bit Odd/Even	419
Parity generator/checker	—		8262/S62		9-Bit Odd/Even	560
Shifter	350		X		4-Bit, 4-Way Shifter	449

COUNTERS, ASYNCHRONOUS (RIPPLE)

FUNCTION	54/74 TYPE	FAMILIES			MODULO	PAGE
		STD	S	LS		
Decade	90	X		X	2x5	136
Divide-by-12	92	X		X	2x6	142
Binary	93	X		X	2x8	145
Decade	—	—	— 8280 —	—	2x5	581
Decade	—	—	8290/S90	—	2x5	594
Decade	196			X	2x5	352
Binary	—	—	— 8281 —	—	2x8	581
Binary	—	—	8291/S91	—	2x8	594
Binary	197			X	2x8	357
Decade	290			X	2x5	426
Binary	293			X	2x8	429
Dual decade	390			X	2x5x2x5	491
8-Bit binary	393			X	16x16	494
Dual decade	490			X	10x10	510

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FUNCTION	54/74 TYPE	FAMILIES			COUNTER TYPES	PAGE
		STD	S	LS		
Decade	160	X		X	BCD, Master Reset	251
Binary	161	X		X	4-Bit, Master Reset	256
Decade	162	X		X	BCD, Synchronous Reset	261
Binary	163	X		X	4-Bit, Synchronous Reset	266
U/D decade	168			X	BCD, Synchronous expansion	282
U/D binary	169			X	4-Bit, Synchronous expansion	287
U/D Decade	190	X		X	BCD, U/D Mode Control	326
U/D binary	191	X		X	4-Bit, U/D Mode Control	331
U/D decade	192	X		X	BCD, Separate U & D Clocks	336
U/D binary	193	X		X	4-Bit, Separate U & D Clocks	340
U/D decade	568			X	BCD, 3-State, Sync & Async Reset	513
U/D binary	569			X	4-Bit, 3-State, Sync & Async Reset	520

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DECODERS/DEMULPLEXERS

FUNCTION	54/74 TYPE	FAMILIES			FEATURES	PAGE
		STD	S	LS		
Dual 1-of-4	139		X	X	Separate address	212
Dual 1-of-4	155	X		X	Common address	238
Dual 1-of-4	156	X		X	O.C. outputs	241
Dual 1-of-4	256			X	Active HIGH outputs	393
1-of-8	138		X	X	3-enables	209
1-of-8	—	—	— 8250 —	—	Octal with enable	557
1-of-8	259			X	Active HIGH outputs	403
1-of-8	—	—	— 9334 —	—	Active HIGH outputs	625
1-of-10	42	X		X	BCD, blank above "9"	73
1-of-10	43	X			Excess 3-to-decimal	75
1-of-10	44	X			Excess 3-gray-to-decimal	77
1-of-10	45	X			80mA, 30V outputs	79
1-of-10	—	—	— 8251 —	—	BCD with enable	557
1-of-10	—	—	— 8252 —	—	BCD, blank above "9"	557
1-of-10	145	X		X	80mA, 15V outputs	215
1-of-10	445			X	80mA, 7V outputs	508
1-of-16	154	X		X	2-enables	235

DECODERS/DISPLAY DRIVERS

FUNCTION	54/74 TYPE	FAMILIES			FEATURES	PAGE
		Std	S	LS		
BCD-to-7-segment	46	X			40mA, 30V, active LOW outputs	81
BCD-to-7-segment	47	X			40mA, 15V, active LOW outputs	81
BCD-to-7-segment	48	X			8mA, active HIGH output	84
BCD-to-7-segment	—	—	— NE586 —	—	Latched, 25mA constant current	•
BCD-to-7-segment	—	—	— NE587 —	—	Latched, program- able constant current	•
BCD-to-7-segment	—	—	— DS8880 —	—	80V, gas filled display tube driver	•

NOTE

*See Signetics ANALOG DATA MANUAL for data sheets.

O.C. = Open collector

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LATCHES, TRANSPARENT

FUNCTION	54/74 TYPE	FAMILIES			FEATURES	PAGE
		STD	S	LS		
4-Bit D	75	X		X	True & Comp. outputs	111
4-Bit D	197			X	Also 4-Bit Counter	357
4-Bit D	375			X	True & Comp. outputs	478
4-Bit R-S	279	X		X	Switch debouncer	418
Dual 4-Bit	256			X	Addressable	393
Dual 4-Bit	100	X			Separate enables	160
Dual 4-Bit	116	X			Gated enable, Master Reset	185
8-Bit D	363			X	3-S, MOS compatible	454
8-Bit D	373			X	3-State	470
8-Bit	—	—	— 9334 —	—	Addressable	625
8-Bit	259			X	Addressable	403

MEMORIES (See Signetics Memory Manual for Larger Memories)

FUNCTION	54/74 TYPE	FAMILIES			FEATURES	PAGE
		STD	S	LS		
4x4 Register	170	X		X	Separate Read / Write Addresses	292
4x4 Register	670			X	LS170 with 3-state outputs	527
16x4 RAM	89		X	X	O.C., transparent while writing	133
16x4 RAM	189		X	X	3-State, disabled while writing	323
16x4 RAM	289		X	X	O.C., disabled while writing	424
16x4 RAM	—	—	— 3101A —	—	O.C., disabled while writing	424
16x4 RAM	—	—	— 8225 —	—	O.C., disabled while writing	424

MULTIPLEXERS

FUNCTION	54/74 TYPE	FAMILIES			FEATURES	PAGE
		STD	S	LS		
Quad 2-input	157	X	X	X	True outputs	244
Quad 2-input	158	X	X	X	Complement outputs	246
Quad 2-input	257		X	X	3-State "157", buffer outputs	397
Quad 2-input	258		X	X	3-State "158", buffer outputs	400
Quad 2-input	—	—	— 8266 —	—	True & Complement inputs	566
Quad 2-input	—	—	— 8267 —	—	True & Complement inputs, O.C. outputs	566
Quad 2-input	—	—	8233 / S33	—	True outputs	547
Quad 2-input	—	—	8234 / S34	—	Complement (O.C.) outputs	547
Quad 2-input	—	—	— 8235 —	—	True & Complement inputs open collector outputs	547
Quad 2-port	298	X		X	Register outputs	436
Quad 2-port	398			X	True & Complement register outputs	502
Quad 2-port	399			X	Register outputs	505
Quad 3-input	—	—	— 8263 —	—	True / Complement control	563
Quad 3-input	—	—	— 8264 —	—	True / Complement control	563
Dual 4-input	153	X	X	X	Separate enables	232
Dual 4-input	253		X	X	3-State "153"	390
8-input	151	X	X	X	True & Complement outputs	227
8-input	251		X	X	3-State "151", buffer outputs	386
8-input	—	—	8230 / S30	—	True & Complement outputs	544
8-input	—	—	8231 / S31	—	True & Complement open collector output	544
8-input	—	—	8232 / S32	—	True & Complement outputs	544
16-input	150	X			True & Complement outputs	223

O.C. = Open collector

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REGISTERS, PARALLEL IN—PARALLEL OUT

FUNCTION	54 / 74 TYPE	FAMILIES			FEATURES	PAGE
		STD	S	LS		
4-Bit	173	X		X	3-State outputs	301
4-Bit	175	X	X	X	True & Complement outputs, MR input	308
4-Bit	298	X		X	Multiplex data inputs	436
4-Bit	379			X	Clock enable input	487
4-Bit	398			X	Multiplex data inputs	502
4-Bit	399			X	Multiplex data inputs	505
4x4	170	X		X	4-Addressable register	292
4x4	670			X	3-State LS170	527
6-Bit	174	X	X	X	Master Reset input	305
6-Bit	378			X	Clock Enable input	484
8-Bit	273			X	Master Reset input	415
8-Bit	377			X	Clock Enable input	481
8-Bit	364			X	3-State MOS compatible outputs	458
8-Bit	374			X	3-State outputs	474
10-Bit	—	—	— 8200 —	—	Dual 5-Bit	541
10-Bit	—	—	— 8201 —	—	Dual 5-Bit, Inverted outputs	541
10-Bit	—	—	— 8202 —	—	10-Bit D F-F, Master Reset	541
10-Bit	—	—	— 8203 —	—	10-Bit D F-F, Inverted outputs	541
16-Bit	172		X		8x2, independent read & write ports	296

REGISTERS, SHIFT-LOAD

FUNCTION	54 / 74 TYPE	FAMILIES			FEATURES	PAGE
		STD	S	LS		
4-Bit	94	X			Parallel in-serial out	148
4-Bit	95	X		X	Separate shift and load clocks	152
4-Bit	—	—	— 8270 —	—	Asynchronous load	569
4-Bit	—	—	— 8271 —	—	Asynchronous load, Master Reset	569
4-Bit	194	X	X	X	Shift right / left parallel load	344
4-Bit	195	X	X	X	Shift right, parallel load	348
4-Bit	295			X	Shift-load, 3-state outputs	432
4-Bit	395			X	Expandable shift, 3-state outputs	497
5-Bit	96	X		X	Shift right, parallel load	156
8-Bit	91	X		X	Serial in-serial out	139
8-Bit	164	X		X	Serial in-parallel	271
8-Bit	165	X			Parallel in-serial out	274
8-Bit	166	X			Parallel in-serial out	278
8-Bit	299			X	Parallel, 3-state input / output	439
8-Bit	323			X	Master Reset LS299 with Synchronous Reset	444
8-Bit	198	X			Parallel & Serial in-parallel & serial out	362
8-Bit	199	X			Universal, reversible, shift-load	366
Dual 8-Bit	—	—	— 8277 —	—	Dual, Serial in-serial out	579

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Arithmetic Units

8282	4-Bit BCD Arithmetic Unit	586
82S83	44-Bit BCD Adder	590

Counters

8280	BCD Decade Counter/Storage Element	581
8281	4-Bit Binary Counter/Storage Element	581
8290	Presetable High Speed Decade Counter	594
82S90	Presetable High Speed Decade Counter	594
8291	Presetable High Speed Decade Counter	594
82S91	Presetable High Speed Decade Counter	594
8292	Presetable Low Power Decade Counter	600
8293	Presetable Low Power Binary Counter	600

Decoders Display Drivers

8250	Binary-to-Octal Decoder	557
82S50	Binary-to-Octal Decoder	557
8251	BCD-to-Decimal Decoder	557
82S51	BCD-to-Decimal Decoder	557
8252	BCD-to-Decimal Decoder	557
82S52	BCD-to-Decimal Decoder	557

Generator/Checker

8262	8-Bit Parity Generator/Checker	560
82S62	8-Bit Parity Generator/Checker	560

Multiplexers

8230	8-Input Digital Multiplexer	544
82S30	8-Input Digital Multiplexer	544
8231	8-Input Digital Multiplexer	544
82S31	8-Input Digital Multiplexer	544
8232	8-Input Digital Multiplexer	544
82S32	8-Input Digital Multiplexer	544
8233	2-Input 4-Bit Digital Multiplexer	547
82S33	2-Input 4-Bit Digital Multiplexer	547
8234	2-Input 4-Bit Digital Multiplexer	547
82S34	2-Input 4-Bit Digital Multiplexer	547
8263	2-Input 4-Bit Digital Multiplexer	563
8264	2-Input 4-Bit Digital Multiplexer	563
8266	2-Input 4-Bit Digital Multiplexer	566
82S66	2-Input 4-Bit Digital Multiplexer	566
8267	2-Input 4-Bit Digital Multiplexer	566
82S67	2-Input 4-Bit Digital Multiplexer	566

Parity Functions

8241	Quad Exclusive-OR/NOR Gate	550
82S41	Quad Exclusive-OR/NOR Gate	550
8242	Quad Exclusive-OR/NOR Gate	550
82S42	Quad Exclusive-OR/NOR Gate	550

Registers/Latches

8200	Buffer/Register	541
8201	Buffer/Register	541
8202	Buffer/Register	541
8203	Buffer/Register	541
8270	4-Bit Shift Register	569

INDEX BY FUNCTION (Cont'd)

8200 SERIES

Registers/Latches (Cont'd)

82S70	4-Bit Shift Register	569
8271	4-Bit Shift Register	569
82S71	4-Bit Shift Register	569
8273	10-Bit Serial-In Parallel-Out Shift Register	573
8274	10-Bit Parallel-In Serial-Out Shift Register	576
8277	Dual 8-Bit Shift Register	579

Scaler

8243	8-Position Scaler	553
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SECTION 2

Product Information

PRODUCT INFORMATION

INTRODUCTION

The TTL Logic devices described in this data manual differ widely in function, complexity and performance, but their electrical input and output characteristics are very similar and are defined and tested to guarantee compatibility. The data sheets that make up this book cover four major categories of TTL circuits and a series of TTL compatible interface products.

The oldest TTL product category is the gold doped double diffused type which is made up of the 54/7400, the 8200 and the 9300 families of devices. These families reflect the same performance ranges and differ only in functions and pin configuration. The 54H/74H00 family is a high performance version of the 54/74 series which uses the gold doped structure, but has higher power and faster speeds.

The remaining two categories of product are fabricated with a non-saturating Schottky clamped transistor technique. The 54S/74S00 and 82S00 families of TTL products are very high performance, high power devices. These two families differ in types of functions offered, and input LOW level loading. They otherwise represent the same speed-power ranges. The newest and most popular TTL category is the 54LS/74LS Low Power Schottky family. These products feature the performance of the 54/74 family at about 1/4 the power.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages and currents as shown below.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	54/74, 8200, 9300	54H/74H	54S/74S, 82S00	54LS/74LS
V _{CC} Supply voltage, continuous (Note a)	7.0V	7.0V	7.0V	7.0V
Input voltage, continuous (Notes a & b)	-0.5V to +5.5V	-0.5V to +5.5V	-0.5V to +5.5V	-0.5V to 15V(b)
Input current, continuous	-30mA to +5mA	-15mA to +5mA	-30mA to 5mA	-30mA to +1mA
Voltage applied to HIGH outputs (Note a)	-0.5V to V _{CC}	-0.5V to 7.0V	-0.5V to 7.0V	-0.5V to V _{CC}
Voltage applied to "off" Open Collector outputs (Notes a & c)	-0.5V to 7.0V	-0.5V to 7.0V	-0.5V to 7.0V	-0.5V to 7.0V
Current into LOW standard output, continuous	30mA	40mA	40mA	15mA
Current into LOW Buffer output, continuous	80mA	100mA	100mA	50mA
Operating free air temperature range	-55°C to +125°C			
Storage temperature range	-65°C to +150°C			

NOTES

- Voltages are referenced to device ground terminal.
- The following LS device inputs are limited to 5.5V input breakdown: All inputs of LS181, Clock inputs of LS90, LS92, LS93, LS196, LS197, LS290, LS293, LS390, LS393 and LS490.
- Some open collector devices are specially processed to handle higher output voltages of from 15V to 30V. The Absolute Maximum voltage for these devices is 10% over the specified V_{OUT} test condition.

OPERATING TEMPERATURE AND VOLTAGE RANGES

The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 volts. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250mV) over an ambient temperature range of 0°C to 70°C. The 8200, 82S00 and 9300 Commercial grade parts are guaranteed to operate over a 0°C to 75°C ambient temperature range.

The Military grade parts are guaranteed to perform with a ±10% supply tolerance (±500mV) over an ambient temperature range of -55°C to +125°C. The 8200 Military grade supply voltage tolerance is limited to ±5% (±250mV).

The actual junction temperature can be calculated by multiplying the power dissipation of the device with the thermal resistance of the package and adding it to the measured ambient temperature T_A or package (case) temperature T_C. The thermal resistance for the various packages in which the TTL products are offered is specified with the Package Information in Section 9 of this manual.

GENERAL TTL CIRCUIT CHARACTERISTICS

All TTL products are derived from a common NAND logic structure. The NAND circuit is actually five subcircuits as shown in Figure 1 and each performs a separate function. The input circuit (1) is an AND gate usually fabricated with a multi-emitter transistor which characterizes TTL technology. Many Schottky processed circuits have been designed with PNP or diode inputs in order to optimize the speed/power performance of the circuits.

The phase splitter (2) provides the inversion

NAND Gate Example

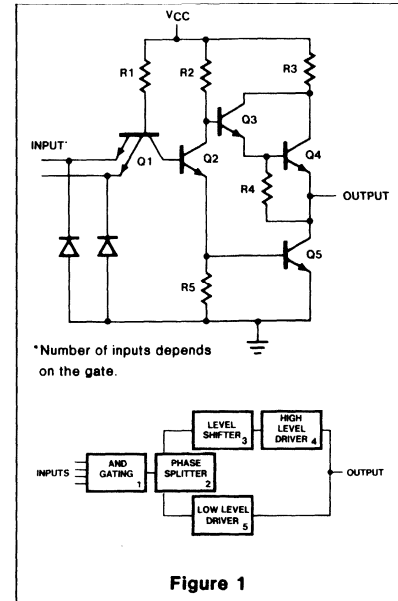


Figure 1

and amplification in the circuit. It determines whether the outputs are active level HIGH or active level LOW. The level shifter (3) provides noise immunity between the HIGH and LOW output levels, and minimizes the possibility of having both HIGH level driver (4) and LOW level driver (5) on simultaneously.

The level shifter (3) and HIGH level driver (4) combine to form an emitter follower circuit that tracks the voltage at the collector of the phase splitter. This circuit is usually designed to drive very heavy capacitive loads so that the initial rise time of the output is determined primarily by the rise time at the

TTL INPUT CONFIGURATIONS

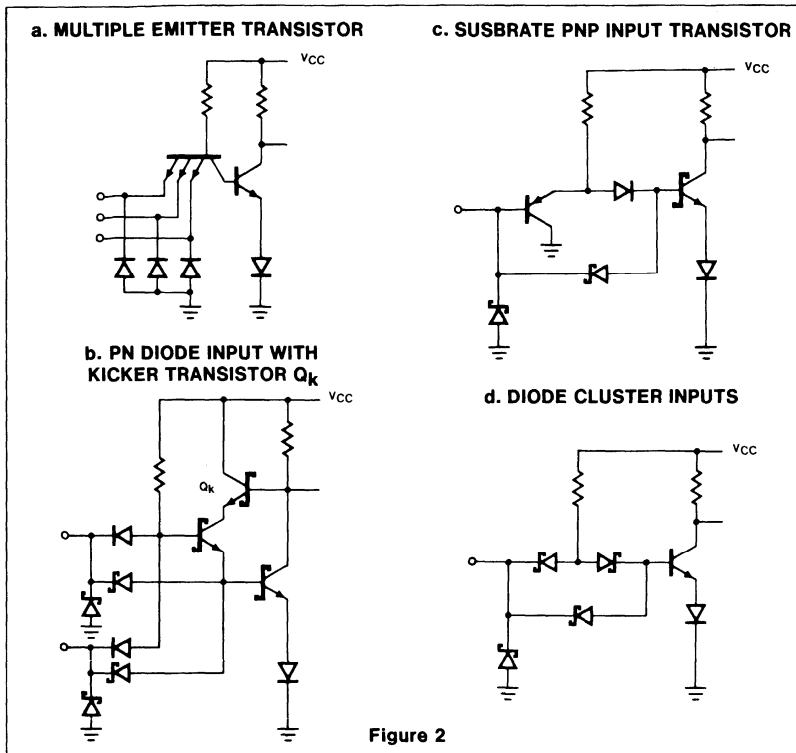


Figure 2

phase splitter collector. The LOW level driver (5) is usually a saturating transistor for the gold doped process devices, or a Schottky diode clamped transistor for the Schottky processed devices. These output transistors are designed to sink the rated fan-out current which characterizes the various TTL families.

Input Circuits

The input circuits as described above are basically AND gate configurations designed with multiple-emitter NPN transistors (MET), substrate PNP transistors, or various junction and Schottky diodes as shown in Figure 2. All of the circuit configurations have very high impedance in the HIGH state. When the input voltage is above the circuit threshold voltage, all of the inputs act like reversed biased diodes. The MET transistors are actually operated in the inverse mode, but the gain is so low there is very little current flowing into the devices.

The LOW level input impedance of the MET and diode inputs is determined by the internal pull-up resistor. This resistor is nominally 4KΩ for the 54/74, 8200, and 9300 inputs, it is 2KΩ for the 54H/74H and 54S/74S inputs, and it is 16KΩ to 20KΩ for the 54LS/74LS inputs. The 82S00 devices have substrate PNP inputs which exhibit very high imped-

ance at both HIGH and LOW input logic levels. This PNP input structure is also used some 54LS/74LS buffer products to minimize the input load factor and produce better output drive and performance.

The inputs to all Signetics TTL devices have clamp diodes to ground to minimize negative ringing effects. These diodes are designed to operate in the ac mode and cannot handle heavy dc currents for long periods.

Output Circuits

The output circuit configurations used for the TTL products in this manual are shown in Figure 3. The basic advantages and disadvantages of each configuration is given for reference. The different circuits are used to optimize the functional and performance requirements of the various devices, and are not necessarily restricted to individual TTL families. The pull-down circuit (not shown) on the base of the LOW level driver is usually a resistor which provides a means of turning off the output transistor. The majority of the 54S/74S, 82S00, and 54LS/74LS devices use a resistor-transistor network which acts to square-up the V_{IN} - V_{OUT} transfer characteristics of the device.

A resistive pull up can be added to any TTL output circuit increasing V_{OH} to almost

V_{CC} , but only circuits "c," "d," and "e" can be pulled higher than V_{CC} , e.g., to +7.0V for driving MOS circuits. Configurations "a" and "b" have a diode associated with the resistor at the output which clamps the output one diode drop above V_{CC} . This is an important consideration in large systems where sections might be powered down ($V_{CC} = 0$). In this state, the outputs of circuits "a" and "b" represent a very low impedance at a fairly low voltage (< 1.0V), while the outputs of circuits "c", "d", and "e" represent a high impedance and thus a logic HIGH, more appropriate for isolation from the rest of the system.

The output impedance of a typical TTL device in both the LOW and HIGH state is shown in Figure 4. In the LOW state, the output impedance is determined by a saturated transistor (about 8Ω to 10Ω). However, at very high sinking current, especially at low temperature, the output device is not able to stay in saturation and the output impedance rises as shown.

When switching from the LOW to the HIGH state, the totem-pole output structure provides a low output impedance capable of rapidly charging capacitive loads. However, charge and discharge currents must also flow through the V_{CC} and ground distribution networks. The V_{CC} and ground lines should therefore be short and adequately decoupled.

3-State Outputs

Many new buffers and registers have 3-state outputs designed for "busing". This type of output electrically performs as a totem-pole output with the additional feature that the output may be disabled, neither sinking nor sourcing current. The 3-state outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-state output should be active at any time.

DESIGN CONSIDERATIONS

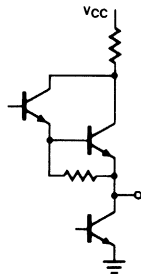
The properties of high speed TTL logic circuits dictate that some care be used in the design and layout of a system. Some general "design considerations" are included in this section. This is not intended to be a thorough guideline for designing TTL systems, but a reference for some of the constraints and techniques to be considered when designing the system.

Clamp Diode Effect on Negative Input Voltages

All Signetics TTL circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes

TTL OUTPUT CONFIGURATIONS

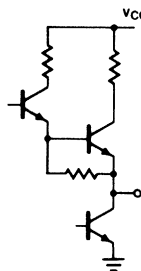
a. DARLINGTON



ADVANTAGE:
 High ac drive capability
 $V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$
 Small size (transistors share one common isolation)

DISADVANTAGE:
 Output cannot be pulled higher than one diode drop above V_{CC}

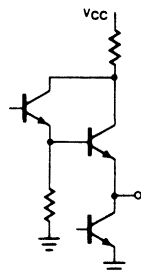
b. 2-STAGE EMITTER FOLLOWER ("DARLINGTON SPLIT")



ADVANTAGE:
 High ac drive capability
 $V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$

DISADVANTAGE:
 Larger than circuit A
 Output cannot be pulled higher than one diode drop above V_{CC}

c. DARLINGTON WITH RESISTOR TO GROUND



ADVANTAGE:
 High ac drive capability
 Lower $V_{OH} = (V_{CC} - 2 V_{BE})$ increases speed
 Outputs can be pulled higher than V_{CC}

DISADVANTAGE:
 Higher dissipation
 Lower noise immunity in the HIGH state

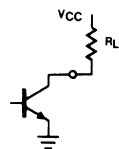
d. TRANSISTOR-DIODE



ADVANTAGE:
 Lowest power consumption
 Small size
 Outputs can be pulled higher than V_{CC}

DISADVANTAGE:
 Less ac drive capability

e. OPEN COLLECTOR



ADVANTAGE:
 Bussable, allows collector ANDing (Wired-OR)

DISADVANTAGE:
 High output impedance in the HIGH state
 Slow, especially with capacitive loading
 Requires additional resistor

Figure 3

TYPICAL INPUT/OUTPUT CHARACTERISTICS

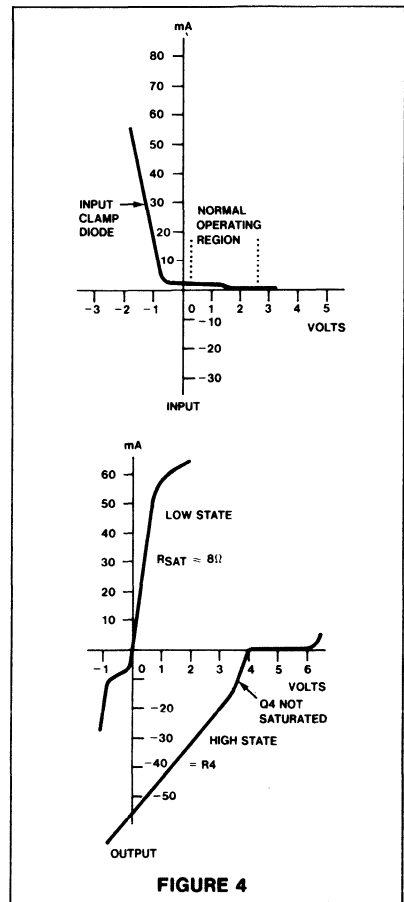


FIGURE 4

should not be used to clamp negative dc voltages or long duration negative pulses especially for 54LS/74LS product. If the input voltage of an LS device is taken more than 0.5 volts negative (referenced to the device ground terminal) for more than 0.5 micro-seconds, it is possible to activate a parasitic circuit component which can cause the HIGH level output of that gate to degrade sufficiently to cause a logic error.

Disposition of Unused Inputs

Electrically open inputs degrade ac noise immunity as well as the switching speed of a circuit. To optimize performance, each input must be connected to a low impedance source. Unused active HIGH NOR or OR inputs must be returned to ground or a LOW level output. Unused active HIGH NAND or AND inputs should be maintained at a voltage greater than 2.7V, but not exceeding the Absolute Maximum Rating. This eliminates the distributed capacitance associated with the floating input, bond wire, and

PRODUCT INFORMATION

package lead, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect the unused active LOW inputs of the TTL devices to ground. The active HIGH inputs should be tied through a resistor of from 1k to 10kohm to V_{CC} . The unused active HIGH LS inputs can be tied directly to V_{CC} , as long as the leads are very short and the supply is adequately decoupled.
2. Connect the unused HIGH input to the output of an unused gate that is forced HIGH.
3. Tie unused NAND or AND inputs (multi-emitter inputs) of non LS devices to a used input of the same gate, provided the HIGH level fan out of the driving circuit is not exceeded. Note that the LOW level fan out is not increased by this connection because the inputs share a common base pull-up resistor.

NOTE

For 54LS/74LS devices do *not* connect multiple inputs of a common gate together. This would increase the input coupling capacitance and reduce the ac noise immunity.

Unused Gates

It is recommended that the outputs of unused gates be forced HIGH by tying a NAND gate input or all NOR gate inputs to ground. This lowers the power dissipation and supplies a logic HIGH at the gate output which can be used at unused inputs to other gates.

Extenders

For maximum speed, TTL extender gates or discrete diodes should be placed as close as possible to the gate being extended. This practice minimizes capacitance at the sensitive extension points.

Increasing Fan Out

To increase fan out, inputs and outputs of gates on the same package may be paralleled. It is advisable to limit the gates being paralleled to those in a single package to avoid large transient supply currents due to different switching times of the gates. This is not detrimental to the devices, but could cause logic problems if the gates are being used as clock drivers.

Isolation Diodes

NEVER REVERSE THE V_{CC} AND GROUND POTENTIALS. Catastrophic failure can occur if more than 100mA is conducted through a forward biased substrate (isolation) diode.

Input Loading and Output Drive Characteristics

The logic levels of all the TTL products are fully compatible with each other. However,

the input loading and output drive characteristics of each of these families is different and must be taken into consideration when mixing the TTL families in a system. Table I shows the relative drive capabilities of each family for the Commercial temperature and voltage ranges. For Military ranges the 74LS and 74L drive capabilities must be cut in half. You will note that the 74LS Buffers have three times the drive capability of the standard 74LS devices; in fact, they can drive more loads than any other non-buffer TTL device.

Mixing TTL Families

Most TTL families are intended to be used together, but this cannot be done indiscriminately. Each family of TTL devices has unique input and output characteristics optimized to get the desired speed or power features. Fast devices like 54S/74S and 54H/74H are designed with relatively low input and output impedances. The speed of these devices is determined primarily by fast rise and fall times internally as well as at the input and output nodes. These fast transitions cause noise of various types in the system. Power and ground line noise is generated by the large currents needed to charge and discharge the circuit and load capacitances during the switching transitions. Signal line noise is generated by the fast output transitions and the relatively low output impedances, which tend to increase reflections.

The noise generated by these 54S/74S and 54H/74H can only be tolerated in systems designed with very short signal leads, elaborate ground planes, and good, well decoupled power distribution networks. Mixing the slower TTL families like 54/74 and 54LS/74LS with the higher speed families is also possible but must be done with caution. The slower speed families are more susceptible to induced noise than the higher speed families due to their higher input and

output impedances. The low power schottky 54LS/74LS family is especially sensitive to induced noise and must be isolated as much as possible from the 54S/74S or 54H/74H devices. Separate or isolated power and ground systems are recommended, and the LS input signal lines should **not** run adjacent to lines driven by 54S/74S or 545H/74H devices.

Mixing 54/74 and 54LS/74LS is less restrictive, and the overall system design need not be so elaborate. Standard two sided PC boards can be used with good, well decoupled power and ground grid systems. The signal transitions are slower and therefore generate less noise. However, good high speed design techniques are still required, especially when working with counters, registers, or other devices with memory.

Clock Pulse Requirements

Most TTL flip-flop circuits are master-slave devices which makes their clock inputs level sensitive. This is an improvement over ac coupled clock inputs, but it does not make the devices fully insensitive to clock edge rates. The dc level at which the data in the master (input section) is transferred to the slave (output section) is the normal threshold voltage for the devices. For most Signetics TTL devices this level is 1.4V at 25°C, and it changes at a rate of about $-4mV/°C$.

When the clock input reaches the threshold voltage, the internal gates and the changing outputs start to dump current into the ground lead of the device. If there are enough internal gates or loaded outputs changing at the same time, the chip ground reference level (and therefore the clock input reference level) can rise by as much as 500mV. This ground noise is the algebraic sum of the internal and external ground plane noise. If the clock input of a positive edge triggered device is at or near the threshold of the

DRIVING DEVICE	NUMBER OF LOADS DRIVEN						
	74LS	74	74H	74L	74S	8200 AND 9300	82S00
74LS	20	5	4	40	4	5	20
*74LS Buffers	60	15	12	120	12	15	60
74	40	10	8	80	8	10	40
74 Buffers	60	30	24	120	24	30	120
74H	50	12	10	100	10	12	50
74H Buffers	75	37	30	150	30	37	150
74L	9	2	1	20	1	2	9
74S	50	12	10	100	10	12	50
74S Buffers	150	37	30	150	30	37	150
8200 & 9300	40	10	8	80	8	10	40
82S00	50	12	10	100	10	12	50

*The 74LS Buffers include 3-State outputs except LS253 & LS670

PRODUCT INFORMATION

device during the ground noise transient period, it is quite possible for the internal device to receive multiple clock pulses.

For this reason the rise time on positive edge triggered devices should be less than the nominal clock to output delay time measured between the 0.8V and 2.0V levels of the clock driver. This edge rate is obtainable from almost any Signetics TTL device of the same family, as long as it is driving no more than rated fan-out and no more than 12 to 16 inches of line. When clock pulses are distributed on lines over 16 inches long, all of the clock inputs should be clustered at the receiving end of the line to avoid reflection problems at the driving end.

Special Note

Some of the recent Signetics counters and registers have been designed with a special clock buffer that includes a small amount of hysteresis to minimize clock edge rate and noise problems. The LS160A, LS161A, LS162A, LS163A, LS364, and LS374 all have the special clock buffers to increase their tolerance of slow positive clock edges and heavy ground noise.

TTL OUTPUTS TIED TOGETHER

The only TTL outputs that are designed to be tied together are open collector and 3-state outputs. Standard TTL outputs should not be tied together unless their logic levels will always be the same; either all HIGH or all LOW. When connecting open collector or 3-state outputs together some general guidelines must be observed:

Open Collector

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active HIGH level. Only special high voltage buffers can be tied to a higher voltage than V_{CC} . The minimum and maximum size of the pull-up resistor is determined as follows:

$$R(\text{Min}) = \frac{V_{CC}(\text{Max}) - V_{OL}}{I_{OL} - N_2(I_{IL})}$$

$$R(\text{Max}) = \frac{V_{CC}(\text{Min}) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee of OR-tied elements.

$N_2(I_{IL})$ = Cumulative maximum input LOW current for all inputs tied to OR-tie connection.

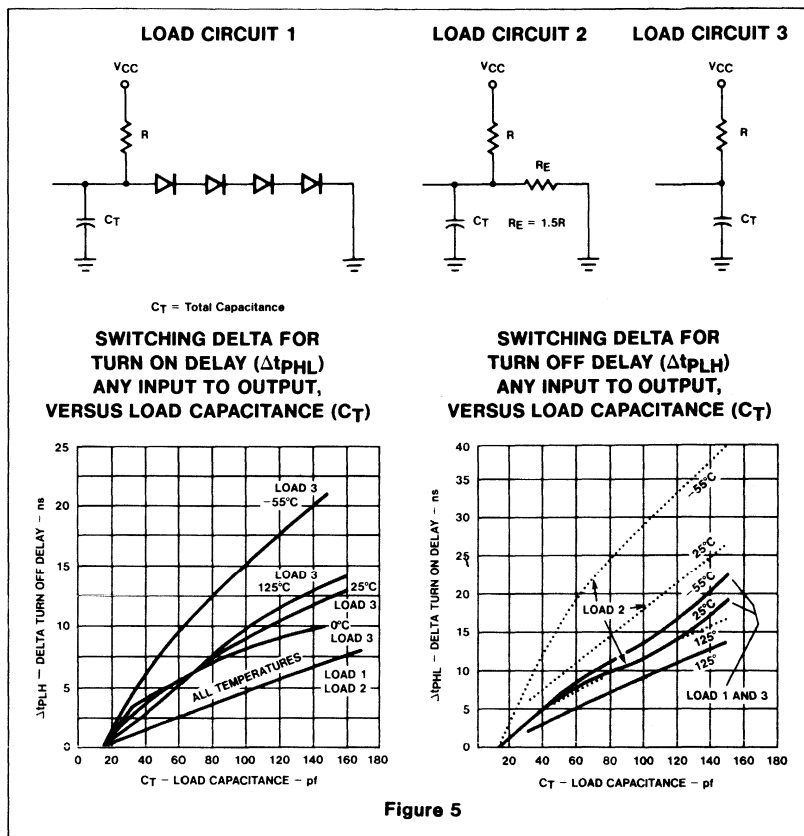


Figure 5

$N_1(I_{OH})$ = Cumulative maximum output HIGH leakage current for all outputs tied to OR-tie connection.

$N_2(I_{IH})$ = Cumulative maximum input HIGH leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the HIGH level, the $R(\text{Max})$ must be decreased enough to provide the required $(V_{OH}/R(\text{pull-down}))$ current.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in Load Circuit 1, Figure 5. Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor Load Circuits 2 and 3 give progressively slower propagation delays.

3-STATE OUTPUTS

3-State Outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-state output should be active at any time. This gener-

ally requires that the Output Enable signals be non-overlapping. When TTL decoders are used to enable 3-state outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally be guaranteed when the address is changing.

Since most 3-state Output Enable signals are active LOW, shift registers or edge triggered storage registers provide good Output Enable buffers. Shift registers with one circulating LOW bit, like the "164" or "194" are ideal for sequential enable signals. The "174" or "273" can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from LOW-to-HIGH faster than from HIGH-to-LOW, the selection of one device at a time is assured.

POWER SUPPLY DECOUPLING

Power supply capacitance decoupling is required for any TTL system. Generally, $0.01\mu\text{F}$ per synchronously driven gate and at least $0.1\mu\text{F}$ for each 20 gates is required regardless of synchronization. Counters and

PRODUCT INFORMATION

shift registers are especially susceptible to power and ground line noise. They should be decoupled with a $0.1\mu\text{F}$ capacitor for each eight internal flip-flops, or one capacitor for each two devices put as close as possible to the devices. Buffers and line drivers should be heavily decoupled at the driver power pins, due to the large current transients needed to charge and discharge the lines.

On-Board Regulation

In most digital systems, there is a large current requirement, and the current supplied usually comes from a main supply. TTL logic tends to generate current spikes during switching due to the overlap in conduction of both upper and lower transistors, thus creating V_{CC} noise. An on-board regulator would not only regulate the power supplied to the circuits on-board, but also would isolate the noise otherwise propagated to the rest of the system. Systems designed using this technique would not need tight regulation on the main power supply.

LINE DRIVING AND RECEIVING

Open wire connections between TTL circuits should not be bundled, tied, or routed together. Instead, point-to-point wiring should be used, preferably above a ground plane which reduces coupling between conductors.

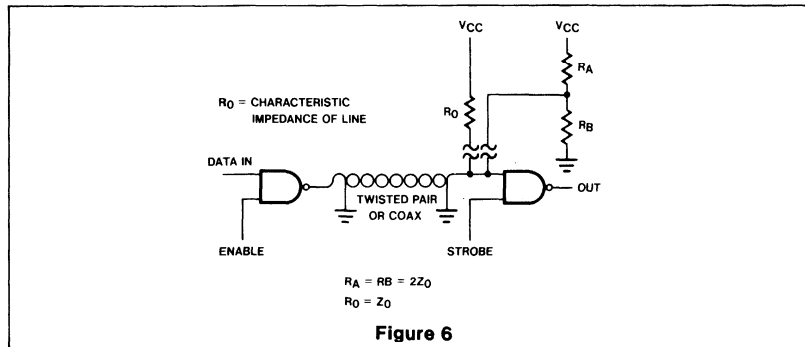
Single line wire interconnections should not exceed two feet; for wires longer than 15 inches, a ground plane is essential to pro-

vide adequate system performance. Over 2-foot twisted pairs or coaxial cable should be used. The characteristic impedance of an open wire over a ground plane is about 150Ω , while for twisted pairs of #26 wire the impedance is about 120Ω . For added protection against crosstalk, coaxial cables can be used but coaxial cables having very low characteristic impedances are difficult to drive. For best performance, coaxial cables with a characteristic impedance R_0 of 100Ω should be used. Resistive pull ups at the receiving end can be used to increase noise margins. If reflection effects are unacceptable, the line must be terminated in its characteristic impedance. One method is shown in Figure 6 where the output of the line is tied to V_{CC} through a resistor equiv-

alent to the characteristic impedance of the line. Therefore R_0 is fairly small, and the driving gate must sink the current through it in addition to the current from the inputs being driven. Terminating the line in a voltage divider with two resistors, each twice the line impedance, reduces the extra sink current by 50%. It is preferable to dedicate gates solely for line driving if the line length is in excess of five feet.

For additional noise immunity when driving long lines, the 8830 and 8820 dual differential line driver and line receiver may be used. These devices drive a twisted pair of wires differentially, permit easy termination of lines, and provide $+15\text{V}$ common mode noise rejection.

TTL DRIVING TWISTED PAIR



DEFINITION OF TERMS AND SYMBOLS

DC SYMBOLS AND DEFINITIONS

Voltages - All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i.e., -10V is greater than -1.0V).

V_{CC}	Supply voltage: The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
$V_{CD}(\text{Max})$	Input clamp diode voltage: The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.
V_{IH}	Input HIGH voltage: The range of input voltages recognized by the device as a logic HIGH.
$V_{IH}(\text{Min})$	Minimum input HIGH voltage: This value is the guaranteed input HIGH threshold for the device. The minimum allowed input HIGH in a logic system.
V_{IL}	Input LOW voltage: The range of input voltages recognized by the device as a logic LOW.
$V_{IL}(\text{Max})$	Maximum input LOW voltage: This value is the guaranteed input LOW threshold for the device. The maximum allowed input LOW in a logic system.
V_M	Measurement voltage: The reference voltage level on ac waveforms for determining ac performance. Usually specified as 1.5V for most TTL families, but 1.3V for the Low Power Schottky 54LS/74LS family.
$V_{OH}(\text{Min})$	Output HIGH voltage: The minimum guaranteed HIGH voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.
$V_{OL}(\text{Max})$	Output LOW voltage: The maximum guaranteed LOW voltage at an output terminal sinking the specified load current I_{OL} .
V_{T+}	Positive-going threshold voltage: The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below $V_{T-}(\text{Min})$.
V_{T-}	Negative-going threshold voltage: The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above $V_{T+}(\text{Max})$.

Currents—Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC}	Supply current: The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.
I_I	Input leakage current: The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.
I_{IH}	Input HIGH current: The current flowing into an input when a specified HIGH level voltage is applied to that input.
I_{IL}	Input LOW current: The current flowing out of an input when a specified LOW level voltage is applied to that input.
I_{OH}	Output HIGH current: The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.
I_{OL}	Output LOW current: The current flowing into an output which is in the LOW state.
I_{OS}	Output short-circuit current: The current flowing out of an output which is in the HIGH state when that output is short circuit to ground.
I_{OZH}	Output off current HIGH: The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
I_{OZL}	Output off current LOW: The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

DEFINITION OF TERMS AND SYMBOLS

AC SWITCHING PARAMETERS AND DEFINITIONS

f_{MAX}	The maximum clock frequency: The maximum input frequency at a clock input for predictable performance. Above this frequency the device may cease to function.	t_{PZL}	Output enable time to a LOW level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "off" state to the LOW level.
t_{PLH}	Propagation delay time: The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.	t_h	Hold time: The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.
t_{PHL}	Propagation delay time: The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.	t_s	Setup time: The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_{PHZ}	Output disable time from HIGH level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the HIGH level to a high impedance "off" state.	t_w	Pulse width: The time between the specified reference points on the leading and trailing edges of a pulse.
t_{PLZ}	Output disable time from LOW level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the LOW level to a high impedance "off" state.	t_{rec}	Recovery time: The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.
t_{PZH}	Output enable time to a HIGH level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "off" state to the HIGH level.		

SECTION 3
54/74 Series
Data Sheets

**54/7400
54H/74H00
54S/74S00
54LS/74LS00**

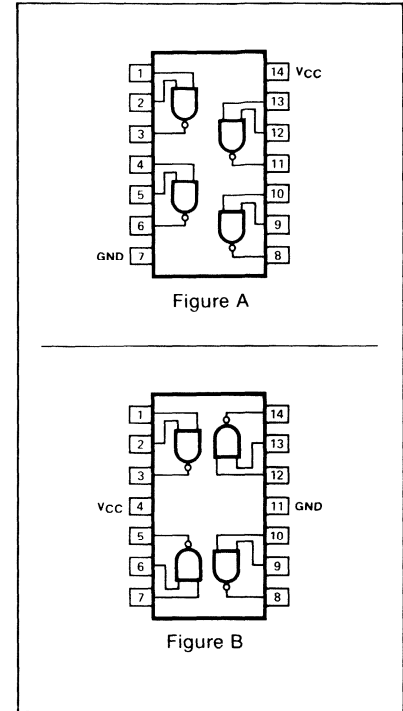
ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
		Plastic DIP	Fig. A Fig. A	N7400N N74S00N	• N74H00N • N74LS00N
Ceramic DIP	Fig. A Fig. A	N7400F N74S00F	• N74H00F • N74LS00F	S5400F S54S00F	• S54H00F • S54LS00F
Flatpak	Fig. B Fig. A			S5400W S54S00W	• S54H00W • S54LS00W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)	-400	-500	-1000	-400
	I_{OL} (mA)	16	20	20	4/8 ^(a)

PIN CONFIGURATIONS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			8.0		16.8		16	1.6	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			12		40		36	4.4	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$			
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	Waveform 1			22		10		4.5	15	ns
t_{PHL}	Propagation delay	Waveform 1			15		10		5.0	15	ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7401
54H/74H01
54LS/74LS01**

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. C	N7401N • N74LS01N N74H01N	
Ceramic DIP	Fig. A Fig. C	N7401F • N74LS01F N74H01F	S5401F • S54LS01F S54H01F
Flatpak	Fig. B Fig. A		S5401W • S54H01W S54LS01W

PIN CONFIGURATIONS

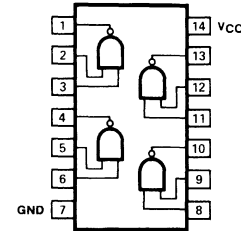


Figure A

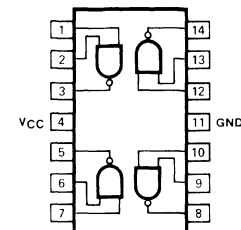


Figure B

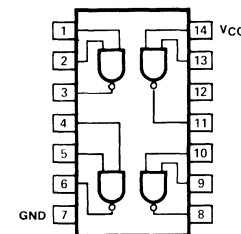


Figure C

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50		20
	I_{IL} (mA)	-1.6	-2.0		-0.36
Outputs	I_{OH} (μA)	+250	+250		+100
	I_{OL} (mA)	16	20		4/8 (a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			8.0		10			1.6	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			22		40			4.4	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$				$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$			
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	Waveform 1			45 (c)		15			32	ns
t_{PHL}	Propagation delay	Waveform 1			15		12			28	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. $R_L = 4k \Omega$ for t_{PLH} .

54/7402
54S/74S02
54LS/74LS02

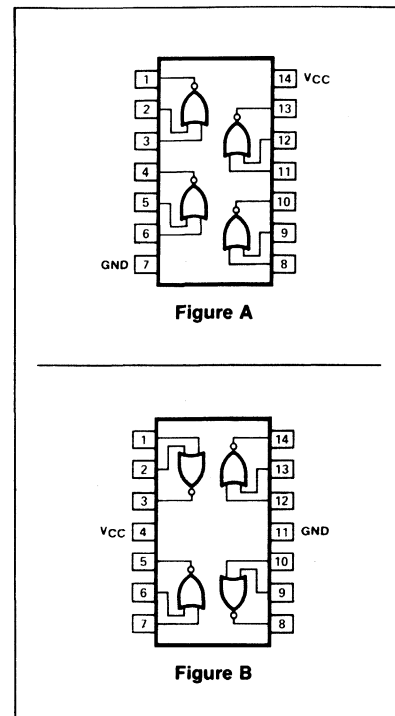
ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7402N • N74S02N N74LS02N	
Ceramic DIP	Fig. A Fig. A	N7402F • N74S02F N74LS02F	S5402F • S54S02F S54LS02F
Flatpak	Fig. B Fig. A		S5402W S54S02W • S54LS02W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40		50	20
	I_{IL} (mA)	-1.6		-2.0	-0.36
Outputs	I_{OH} (μA)	-400		-1000	-400
	I_{OL} (mA)	16		20	$4/8^{(a)}$

PIN CONFIGURATIONS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$		16				29		3.2	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} = (c)$		27				45		5.4	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$				$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		15				5.5		15	ns
t_{PHL} Propagation delay	Waveform 1		15				5.5		15	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. $V_{IN} = 0V$ for one input and $\geq 4.5V$ for other input on each gate.

**54/7403
54S/74S03
54LS/74LS03**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $-70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7403N • N74S03N N74LS03N	
Ceramic DIP	Fig. A Fig. A	N7403F • N74S03F N74LS03F	S5403F • S54S03F S54LS03F
Flatpak	Fig. A Fig. A		S5403W S54S03W • S54LS03W

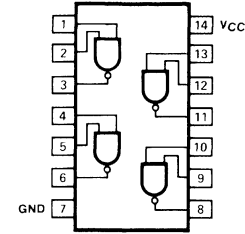


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40		50	20
	I_{IL} (mA)	-1.6		-2.0	-0.36
Outputs	I_{OH} (μA)	+250		+250	+100
	I_{OL} (mA)	16		20	4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		8.0				13.2		1.6	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		22				36		4.4	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$				$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		45 ^(c)				7.5		32	ns
t_{PHL} Propagation delay	Waveform 1		15				7.0		28	ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. $R_L = 4k\Omega$ for t_{PLH} .

54/7404
54H/74H04
54S/74S04
54LS/74LS04

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A Fig. A	N7404N N74S04N	• N74H04N • N74LS04N		
Ceramic DIP	Fig. A Fig. A	N7404F N74S04F	• N74H04F • N74LS04F	S5404F S54S04F	• S54H04F • S54LS04F
Flatpak	Fig. B Fig. A			S5404W S54S04W	• S54H04W • S54LS04W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)	-400	-500	-1000	-400
	I_{OL} (mA)	16	20	20	4/8 ^(a)

PIN CONFIGURATIONS

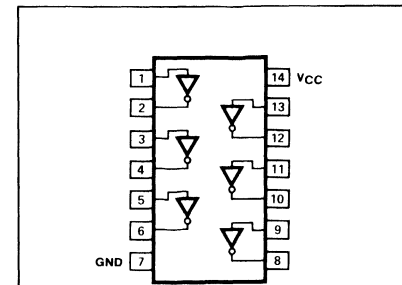


Figure A

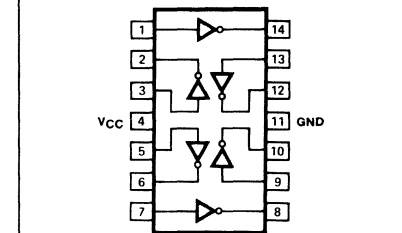


Figure B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		12		26		24		2.5	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		33		58		54		6.6	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		22		10		4.5		15	ns
t_{PHL} Propagation delay	Waveform 1		15		10		5.0		15	ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7405
54H/74H05
54S/74S05
54LS/74LS05**

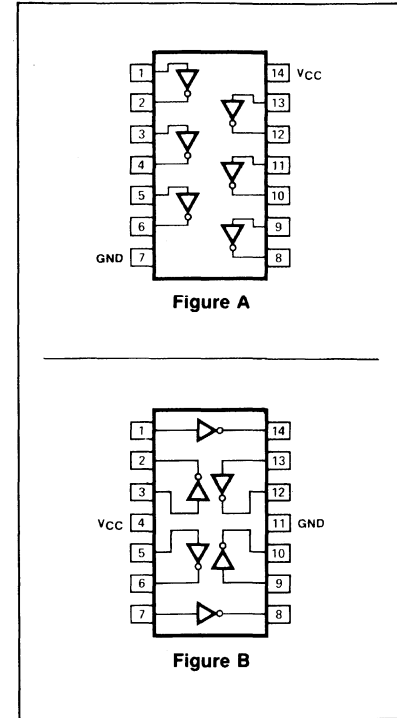
ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A Fig. A	N7405N N74S05N	• N74H05N • N74LS05N		
Ceramic DIP	Fig. A Fig. A	N7405F N74S05F	• N74H05F • N74LS05F	S5405F S54S05F	• S54H05F • S54LS05F
Flatpak	Fig. B Fig. A			S5405W S54S05W	• S54H05W • S54LS05W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)	+250	+250	+250	+100
	I_{OL} (mA)	16	20	20	4/8 ^(a)

PIN CONFIGURATIONS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			12		26		19.8	2.4	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			33		58		54	6.6	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$			
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	Waveform 1			55 ^(c)		15		7.5	32	ns
t_{PHL}	Propagation delay	Waveform 1			15		12		7.0	28	ns

NOTE

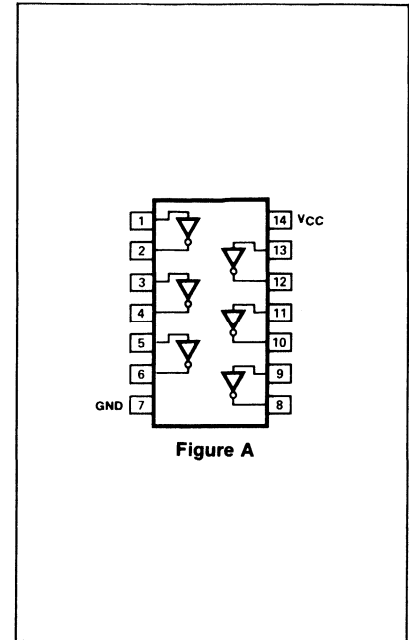
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. $R_L = 4k\Omega$ for t_{PLH} .

54/7406

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7406N	
Ceramic DIP	Fig. A	N7406F	S5406F
Flatpak	Fig. A		S5406W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			
	I_{IL} (mA)	-1.6			
Outputs	I_{OH} (μA)	250			
	I_{OL} (mA)	30/40 ^(a)			

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$, $I_{OL} = 16\text{mA}$		0.4							V
	$V_{IN} = 2.0V$	$I_{OL} = 30\text{mA Mil}$		0.7						V
		$I_{OL} = 40\text{mA Com}$		0.7						V
I_{OH} Output HIGH current	$V_{CC} = \text{Min}$, $V_{IN} = 0.8V$ $V_{OUT} = 30V$		250							μA
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		42							mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		38							mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 110\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		15							ns
t_{PHL} Propagation delay	Waveform 1		23							ns

NOTES

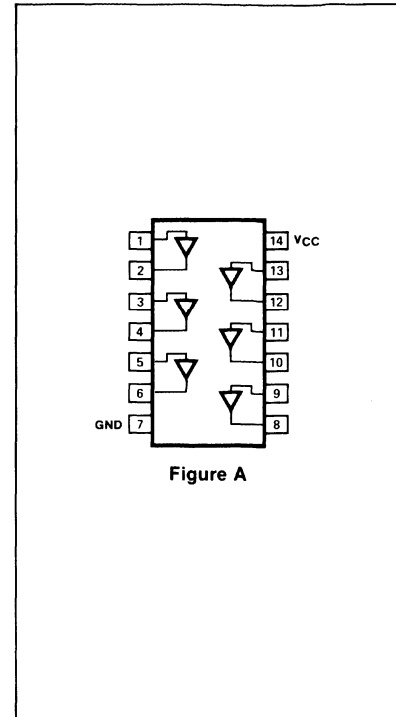
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7407

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7407N	
Ceramic DIP	Fig. A	N7407F	S5407F
Flatpak	Fig. A		S5407W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			
	I_{IL} (mA)	-1.6			
Outputs	I_{OH} (μA)	250			
	I_{OL} (mA)	30/40 (a)			

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$		0.4							V
	$V_{IN} = 2.0V$	$I_{OL} = 16mA$		0.7						V
		$I_{OL} = 30mA$ Mil $I_{OL} = 40mA$ Com		0.7						V
I_{OH} Output HIGH current	$V_{CC} = \text{Min}$, $V_{IN} = 2.0V$ $V_{OUT} = 30V$		250							μA
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		41							mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		30							mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 pF$ $R_L = 110\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 2		15							ns
t_{PHL} Propagation delay	Waveform 2		23							ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7408
54H/74H08
54S/74S08
54LS/74LS08

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	Fig. A Fig. A	N7408N • N74H08N N74S08N • N74LS08N	
Ceramic DIP	Fig. A Fig. A	N7408F • N74H08F N74S08F • N74LS08F	S5408F • S54H08F S54S08F • S54LS08F
Flatpak	Fig. B Fig. A		S54H08W S5408W/S54S08W/S54LS08W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)	-800	-500	-1000	-400
	I_{OL} (mA)	16	20	20	4/8 ^(a)

PIN CONFIGURATIONS

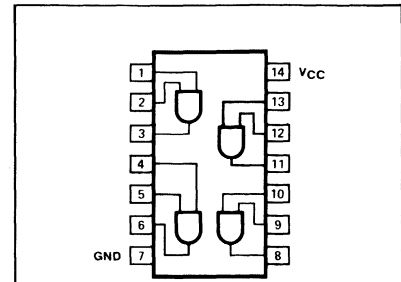


Figure A

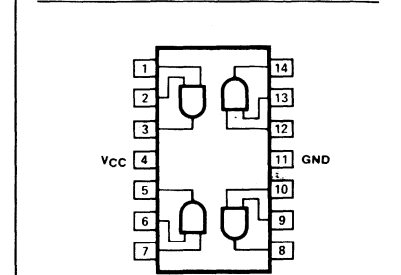


Figure B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current $V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		21		40		32		4.8	mA
I_{CCL}	Supply current $V_{CC} = \text{Max}, V_{IN} = 0V$		33		64		57		8.8	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay Waveform 2		27		12		7.0		15	ns
t_{PHL}	Propagation delay Waveform 2		19		12		7.5		20	ns

NOTES

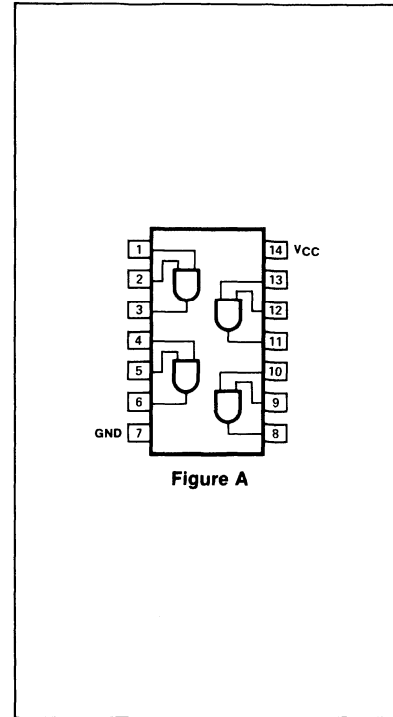
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7409
54S/74S09
54LS/74LS09**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7409N • N74S09N N74LS09N	
Ceramic DIP	Fig. A Fig. A	N7409F • N74S09F N74LS09F	S5409F • S54S09F S54LS09F
Flatpak	Fig. A Fig. A		S5409W • S54S09W S54LS09W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40		50	20
	I_{IL} (mA)	-1.6		-2.0	-0.36
Outputs	I_{OH} (μA)	-800		-1000	-400
	I_{OL} (mA)	16		20	$4/8^{(a)}$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			21				32	4.8	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			33				57	8.8	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		$C_L = 15pF$ $R_L = 400\Omega$				$C_L = 15pF$ $R_L = 280\Omega$		$C_L = 15pF$ $R_L = 2k\Omega$			
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	Waveform 2			32				10	35	ns
t_{PHL}	Propagation delay	Waveform 2			24				10	35	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7410
54H/74H10
54S/74S10
54LS/74LS10

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $-70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7410N • N74H10N N74S10N • N74LS10N	
Ceramic DIP	Fig. A Fig. A	N7410F • N74H10F N74S10F • N74LS10F	S5410F • S54H10F S54S10F • S54LS10F
Flatpak	Fig. B Fig. A		S5410W • S54H10W S54S10W • S54LS10W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)	-400	-500	-1000	-400
	I_{OL} (mA)	16	20	20	4/8 ^(a)

PIN CONFIGURATIONS

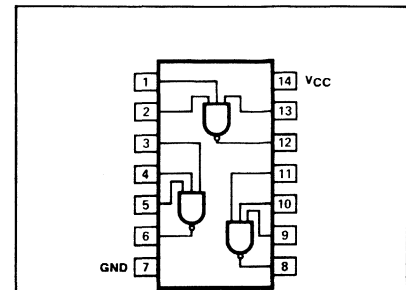


Figure A

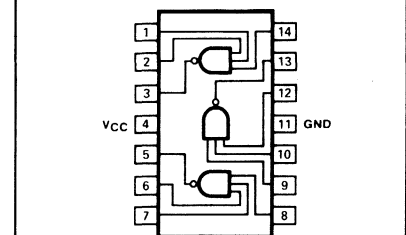


Figure B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			6.0		12.6		12	1.2	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			16.5		30		27	3.3	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$			
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	Waveform 1			22		10		4.5	15	ns
t_{PHL}	Propagation delay	Waveform 1			15		10		5.0	15	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7411
54H/74H11
54S/74S11
54LS/74LS11

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7411N • N74H11N N74S11N • N74LS11N	
Ceramic DIP	Fig. A Fig. A	N7411F • N74H11F N74S11F • N74LS11F	S5411F • S54H11F S54S11F • S54LS11F
Flatpak	Fig. B Fig. A		S5411W • S54H11W S54S11W • S54LS11W

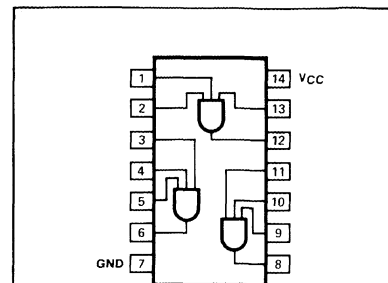


Figure A

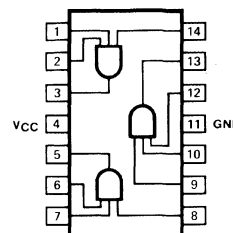


Figure B

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)	-800	-500	-1000	-400
	I_{OL} (mA)	16	20	20	4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current $V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		12		30		24		3.6	mA
I_{CCL}	Supply current $V_{CC} = \text{Max}, V_{IN} = 0V$		20		48		42		6.6	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay Waveform 2		27		12		7.0		15	ns
t_{PHL}	Propagation delay Waveform 2		19		12		7.5		20	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7412
54LS/74LS12**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7412N	• N74LS12N		
Ceramic DIP	Fig. A	N7412F	• N74LS12F	S5412F	• S54LS12F
Flatpak	Fig. A			S5412W	• S54LS12W

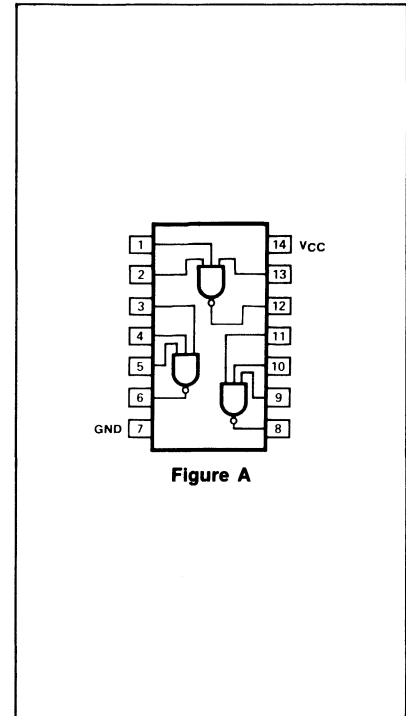


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.36
Outputs	I_{OH} (μA)	-800			-400
	I_{OL} (mA)	16			4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$		6.0				1.4		mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		16.5				3.3		mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$						$C_L = 15pF$ $R_L = 2k\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		45 ^(c)				32		ns
t_{PHL}	Propagation delay	Waveform 1		15				28		ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. $R_L = 4k\Omega$ for t_{PLH} .

54/7413
54LS/74LS13

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7413N	• N74LS13N		
Ceramic DIP	Fig. A	N7413F	• N74LS13F	S5413F	• S54LS13F
Flatpak	Fig. A			S5413W	• S54LS13W

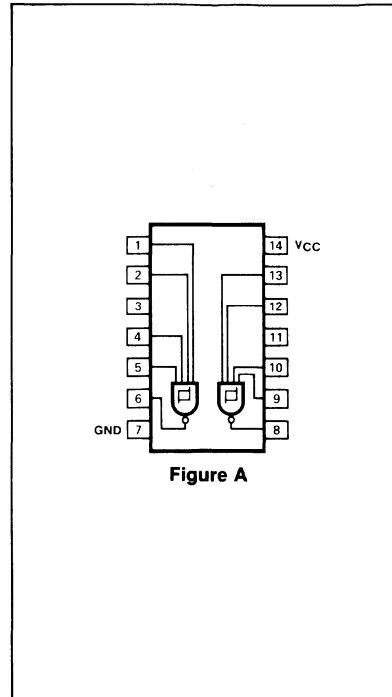


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.4
Outputs	I_{OH} (μA)	-800			-400
	I_{OL} (mA)	16			4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT		
		Min	Max	Min	Max	Min	Max	Min	Max			
V_{T+}	Positive going threshold	$V_{CC} = 5V$		1.5	2.0					1.5	1.9	V
V_{T-}	Negative going threshold	$V_{CC} = 5V$		0.6	1.1					0.6	1.1	V
ΔV_T	Hysteresis	$V_{CC} = 5V$		0.4						0.4		V
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			23						6.0	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			32						7.0	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$						$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Figure H		27					22	ns
t_{PHL}			22					27	ns	

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

TYPICAL CHARACTERISTICS

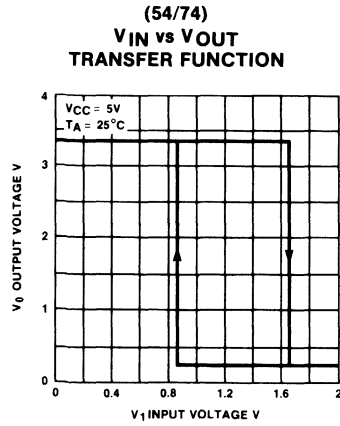


Figure B

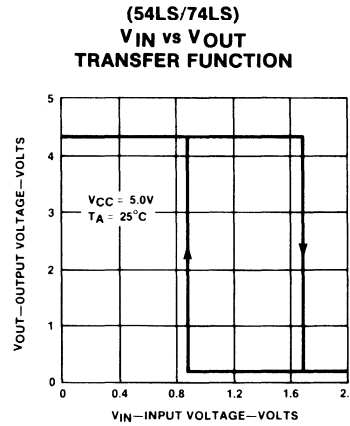


Figure E

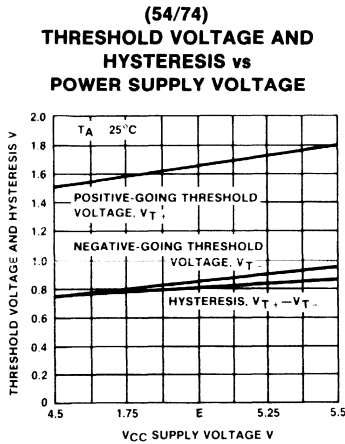


Figure C

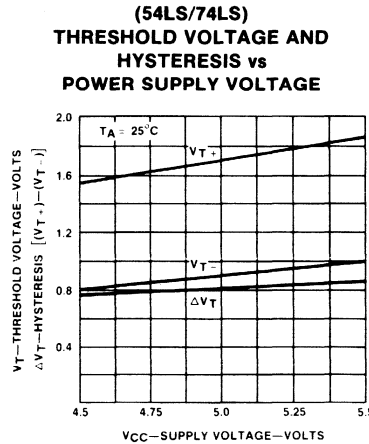


Figure F

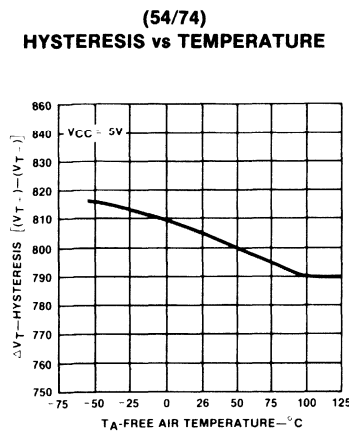


Figure D

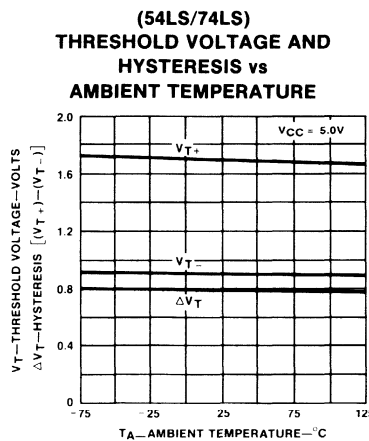


Figure G

FUNCTIONAL DESCRIPTION

The "13" contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition they have greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+} (Max), the gate will respond in the transitions of the other input as shown in Figure H.

AC WAVEFORMS

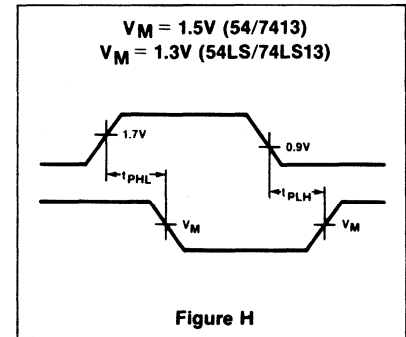


Figure H

54/7414
54LS/74LS14

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7414N	• N74LS14N		
Ceramic DIP	Fig. A	N7414F	• N74LS14F	S5414F	• S54LS14F
Flatpak	Fig. A			S5414W	• S54LS14W

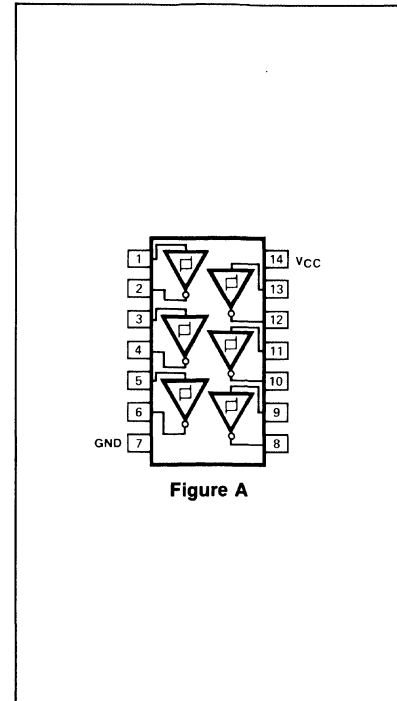


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.2			-0.4
Outputs	I_{OH} (μA)	-800			-400
	I_{OL} (mA)	16			4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{T+}	Positive-going threshold	$V_{CC} = 5V$		1.5	2.0				1.5	1.9	V
V_{T-}	Negative-going threshold	$V_{CC} = 5V$		0.6	1.1				0.6	1.1	V
ΔV_T	Hysteresis	$V_{CC} = 5V$		0.4					0.4		V
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			36					16	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			60					21	mA

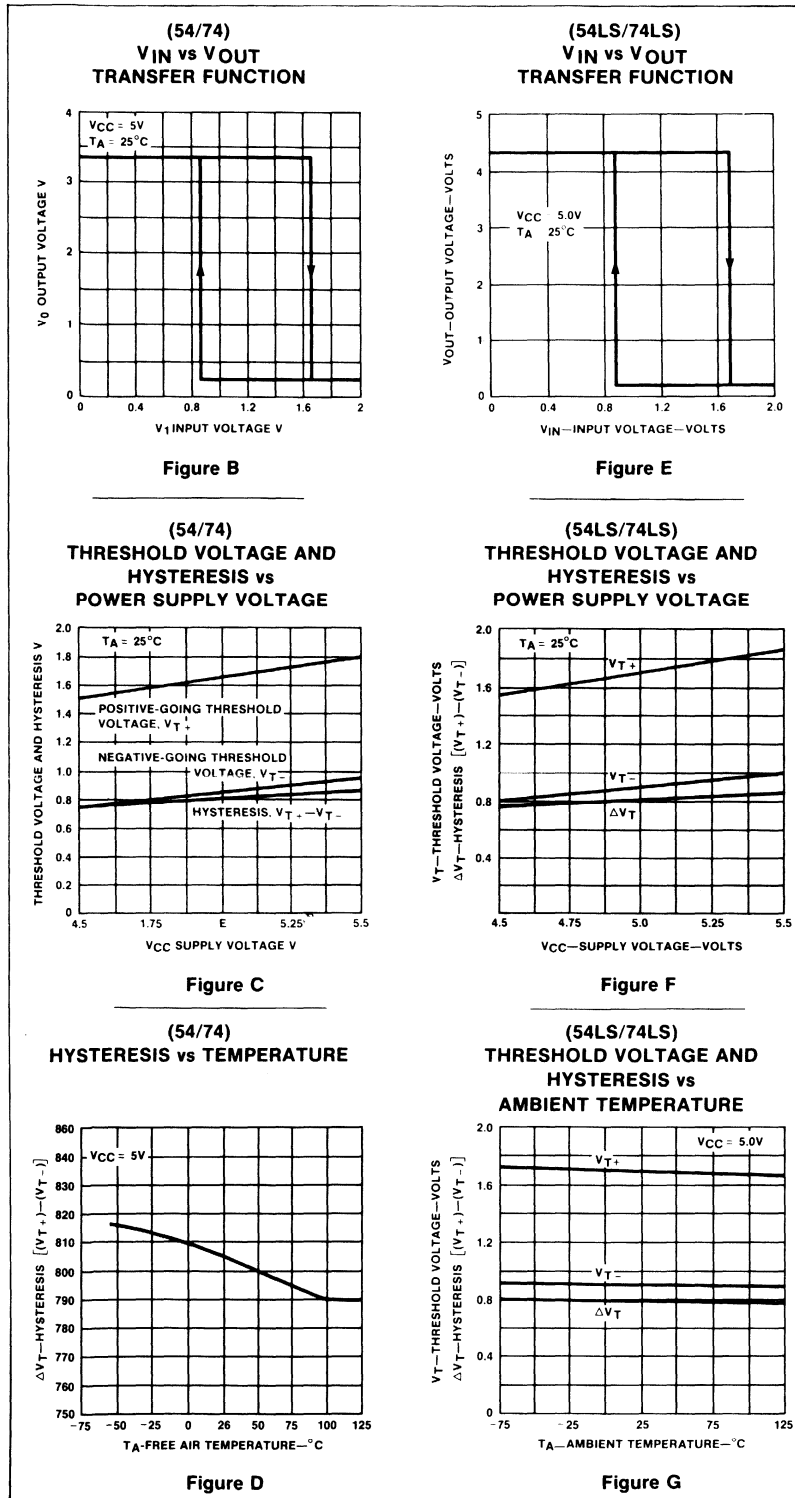
AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$						$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Figure H		22					22	ns
t_{PHL}				22					22	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

TYPICAL CHARACTERISTICS

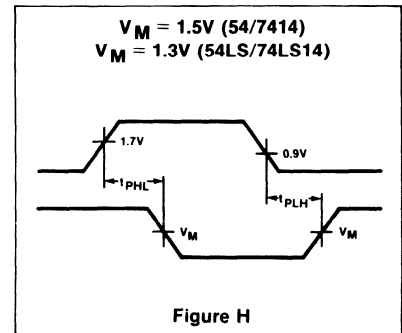


FUNCTIONAL DESCRIPTION

The "14" contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

AC WAVEFORMS



54S/74S15
54LS/74LS15

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74S15N • N74LS15N	
Ceramic DIP	Fig. A	N74S15F • N74LS15F	S54S15F • S54LS15F
Flatpak	Fig. A		S54S15W • S54LS15W

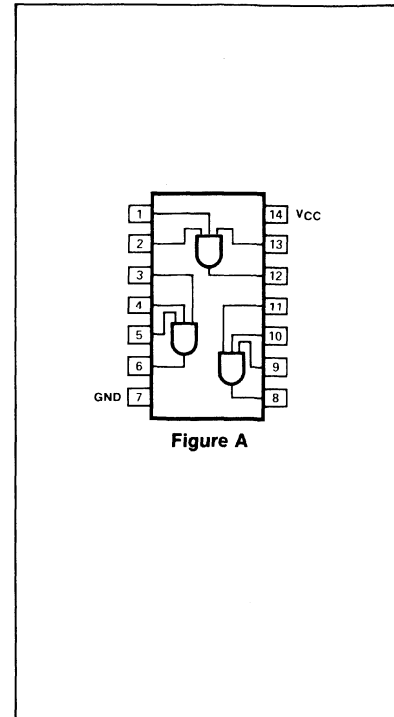


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)			50	20
	I_{IL} (mA)			-2.0	-0.36
Outputs	I_{OH} (μA)			+250	+100
	I_{OL} (mA)			20	4/8 (a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$						19.5	3.6	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$						42	6.6	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
						$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 2					8.5		35	ns
t_{PHL}	Propagation delay	Waveform 2					9.0		35	ns

NOTE

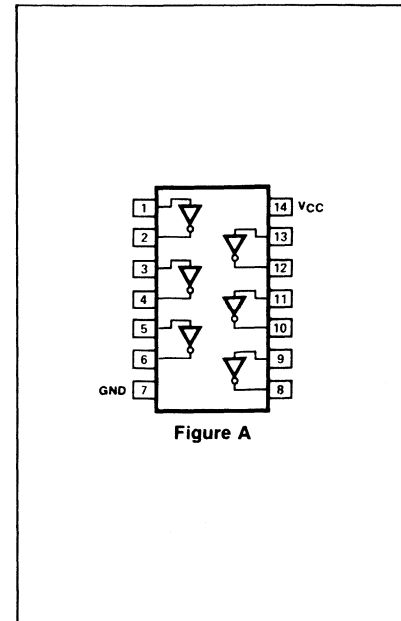
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7416

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7416N	
Ceramic DIP	Fig. A	N7416F	S5416F
Flatpak	Fig. A		S5416W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			
	I_{IL} (mA)	-1.6			
Outputs	I_{OH} (μA)	250			
	I_{OL} (mA)	30/40 ^(a)			

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$, $I_{OL} = 16\text{mA}$		0.4							V
	$V_{IN} = 2.0V$, $I_{OL} = 30\text{mA Mil}$		0.7							V
	$I_{OL} = 40\text{mA Com}$		0.7							V
I_{OH} Output HIGH current	$V_{CC} = \text{Min}$, $V_{IN} = 0.8V$ $V_{OUT} = 15V$		250							μA
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		42							mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		38							mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 110\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		15							ns
t_{PHL} Propagation delay	Waveform 1		23							ns

NOTES

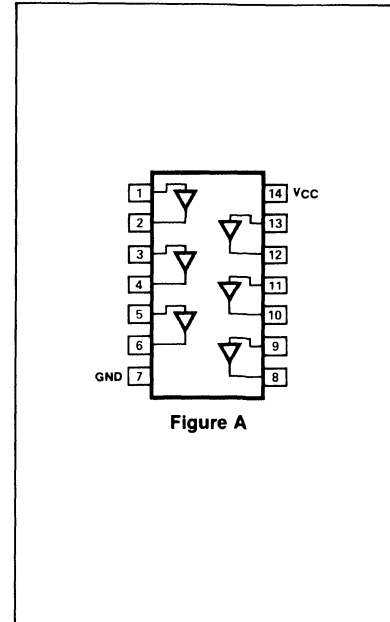
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7417

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7417N	
Ceramic DIP	Fig. A	N7417F	S5417F
Flatpak	Fig. A		S5417W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			
	I_{IL} (mA)	-1.6			
Outputs	I_{OH} (μA)	250			
	I_{OL} (mA)	30/40 ^(a)			

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}, V_{IN} = 0.8V$	$I_{OL} = 16mA$		0.4						V
		$I_{OL} = 30mA$ Mil		0.7						V
		$I_{OL} = 40mA$ Com		0.7						V
I_{OH} Output HIGH current	$V_{CC} = \text{Min}, V_{IN} = 2.0V$ $V_{OUT} = 15V$	250								μA
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$	41								mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$	30								mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 110\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 2	15								ns
t_{PHL} Propagation delay	Waveform 2	23								ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7420
54H/74H20
54S/74S20
54LS/74LS20

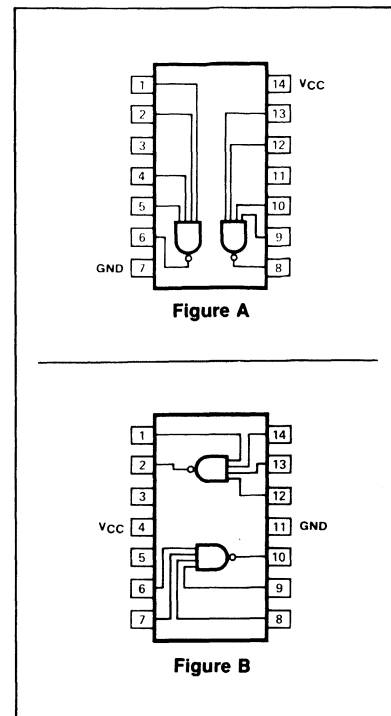
ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A Fig. A	N7420N N74S20N	• N74H20N • N74LS20N		
Ceramic DIP	Fig. A Fig. A	N7420F N74S20F	• N74H20F • N74LS20F	S5420F S54S20F	• S54H20F • S54LS20F
Flatpak	Fig. B Fig. A			S5420W S54S20W	• S54H20W • S54LS20W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)	-400	-500	-1000	-400
	I_{OL} (mA)	16	20	20	4/8 ^(a)

PIN CONFIGURATIONS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			4.0		8.4		8.0	0.8	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			11		20		18	2.2	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		$C_L = 15 pF$ $R_L = 400 \Omega$		$C_L = 25 pF$ $R_L = 280 \Omega$		$C_L = 15 pF$ $R_L = 280 \Omega$		$C_L = 15 pF$ $R_L = 2k \Omega$			
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay	Waveform 1			22		10		4.5	15	ns
t_{PHL}	Propagation delay	Waveform 1			15		10		5.0	15	ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7421
54H/74H21
54LS/74LS21

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7421N • N74H21N N74LS21N	
Ceramic DIP	Fig. A Fig. A	N7421F • N74H21F N74LS21F	S5421F • S54H21F S54LS21F
Flatpak	Fig. B Fig. A		S5421W • S54H21W S54LS21W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50		20
	I_{IL} (mA)	-1.6	-2.0		-0.36
Outputs	I_{OH} (μA)	-800	-500		-400
	I_{OL} (mA)	16	20		$4/8^{(a)}$

PIN CONFIGURATIONS

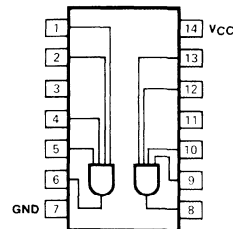


Figure A

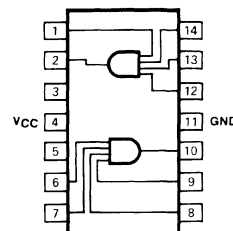


Figure B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		8.0		20				2.4	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$		13		32				4.4	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$				$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 2		27		12				15	ns
t_{PHL} Propagation delay	Waveform 2		19		12				20	ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54H/74H22
54S/74S22
54LS/74LS22

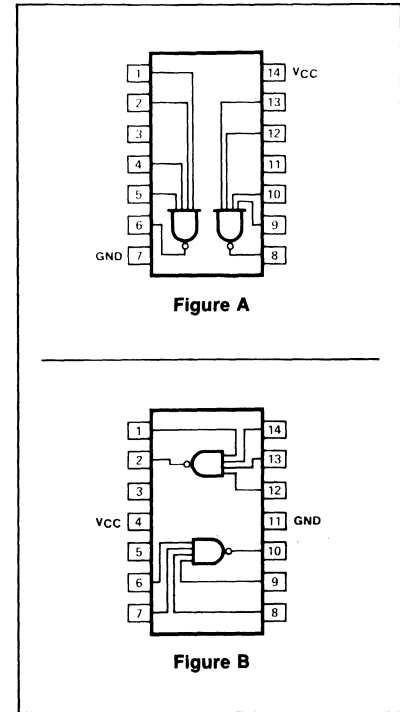
ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N74H22N N74S22N • N74LS22N	
Ceramic DIP	Fig. A Fig. A	N74H22F N74S22F • N74LS22F	S54H22F S54S22F • S54LS22F
Flatpak	Fig. B Fig. A		S54H22W S54S22W • S54LS22W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)		50	50	20
	I_{IL} (mA)		-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)		+250	+250	+100
	I_{OL} (mA)		20	20	4/8 ^(a)

PIN CONFIGURATIONS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$				5.0		6.6		0.8	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$				20		18		2.2	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

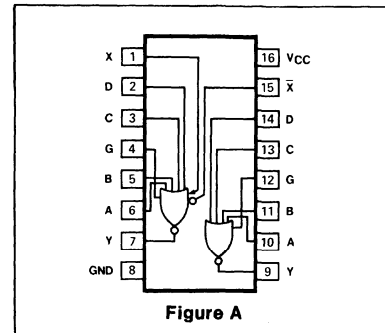
PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$	$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$	$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$				
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1				15		7.5		32	ns
t_{PHL} Propagation delay	Waveform 1				12		7.0		28	ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7423

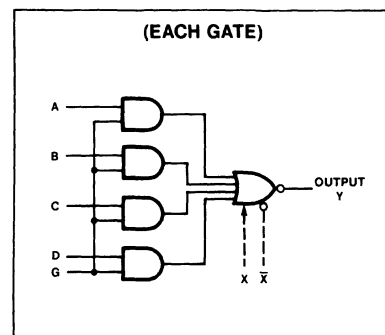
PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7423N	
Ceramic DIP	Fig. A	N7423F	S5423F
Flatpak	Fig. A		S5423W

LOGIC DIAGRAM



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			
	I_{IL} (mA)	-1.6			
Outputs	I_{OH} (μA)	-800			
	I_{OL} (mA)	16			

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{IH}	Input HIGH current for Strobe input $V_{CC} = \text{Max}, V_{IN} = 2.4V$		160							μA
I_{IL}	Input LOW current for Strobe input $V_{CC} = \text{Max}, V_{IN} = 0.4V$		-6.4							mA
I_{CCH}	Supply current $V_{CC} = \text{Max}, V_{IN} = 0V$		16							mA
I_{CCL}	Supply current $V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		19							mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1		22 15							ns ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

DC CHARACTERISTICS using expander inputs, $V_{CC} = 4.5V$, $T_A = -55^\circ C$

PARAMETER	TEST CONDITIONS	5423								UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$I_{\bar{X}}$ Expander current	$V_{\bar{X}X} = 0.4V, I_{OL} = 16mA$		-3.5							mA
	$V_X = 1.4V, I_{\bar{X}} = 0, I_{OL} = 0$									mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor	$I_X + I_{\bar{X}} = 410\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 16mA$		1.1							V
	$I_X + I_{\bar{X}} = 700\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 20mA$									V
V_{OH} Output HIGH voltage	$I_X = 150\mu A, I_{\bar{X}} = -150\mu A$ $I_{OH} = -400\mu A$	2.4								V
	$I_X = 320\mu A, I_{\bar{X}} = -320\mu A$ $I_{OH} = -500\mu A$									V
V_{OL} Output LOW voltage	$I_X + I_{\bar{X}} = 300\mu A$ $R_{\bar{X}X} = 114\Omega, I_{OL} = 16mA$		0.4							V
	$I_X + I_{\bar{X}} = 470\mu A$ $R_{\bar{X}X} = 68\Omega, I_{OL} = 20mA$									V

DC CHARACTERISTICS using expander inputs, $V_{CC} = 4.75V$, $T_A = 0^\circ C$

PARAMETER	TEST CONDITIONS	7423								UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_X Expander current	$V_{\bar{X}X} = 0.4V, I_{OL} = 16mA$		-3.5							mA
	$V_X = 1.4V, I_X = 0, I_{OL} = 0$									mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor	$I_X + I_{\bar{X}} = 620\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 16mA$		1.0							V
	$I_X + I_{\bar{X}} = 1.1mA$ $R_{\bar{X}X} = 0, I_{OL} = 20mA$									V
V_{OH} Output HIGH voltage	$I_X = 270\mu A, I_{\bar{X}} = -270\mu A$ $I_{OH} = 400\mu A$	2.4								V
	$I_X = 570\mu A, I_{\bar{X}} = 570\mu A$ $I_{OH} = 500\mu A$									V
V_{OL} Output LOW voltage	$I_X + I_{\bar{X}} = 430\mu A$ $R_{\bar{X}X} = 105\Omega, I_{OL} = 16mA$		0.4							V
	$I_X + I_{\bar{X}} = 600\mu A$ $R_{\bar{X}X} = 63\Omega, I_{OL} = 20mA$									V

54/7425

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7425N	
Ceramic DIP	Fig. A	N7425F	S5425F
Flatpak	Fig. A		S5425W

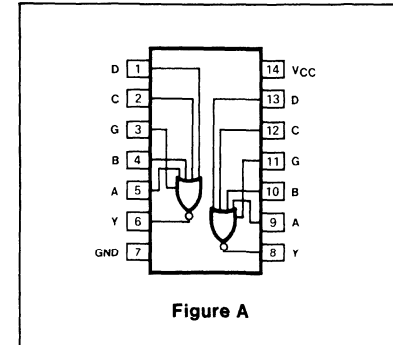
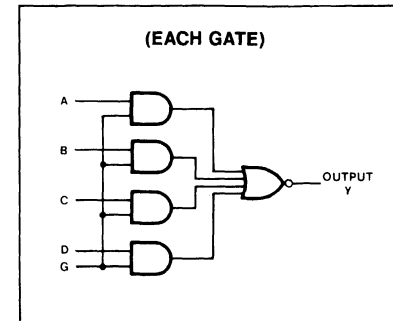


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
G Inputs	I_{IH} (μA)	160			
	I_{IL} (mA)	-6.4			
Other inputs	I_{IH} (μA)	40			
	I_{IL} (mA)	-1.6			
Outputs	I_{OH} (μA)	-800			
	I_{OL} (mA)	16			

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$		16							mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		19							mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		22 15							ns ns

NOTES

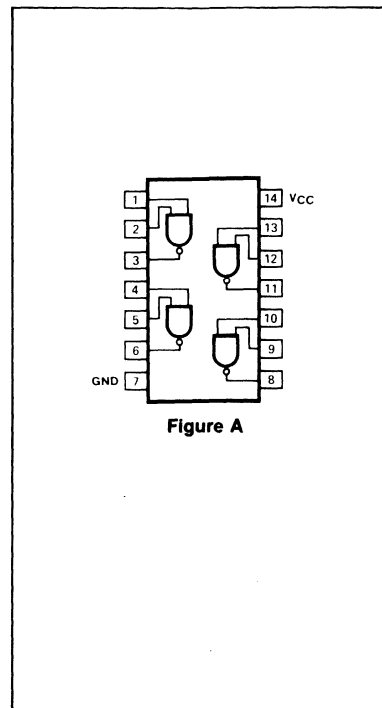
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7426
54LS/74LS26**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7426N • N74LS26N	
Ceramic DIP	Fig. A	N7426F • N74LS26F	S5426F • S54LS26F
Flatpak	Fig. A		S54LS26W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.4
Outputs	I_{OH} (μA)	+50			+50
	I_{OL} (mA)	16			4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{OH} Output HIGH current	$V_{CC} = \text{Min}$ $V_{IN} = V_{IL}$ $V_{OUT} = 12V$		50						50	μA
	$V_{OUT} = 15V$		1.0						1.0	mA
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		8.0						1.6	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		22						4.4	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 pF$ $R_L = 1k\Omega$						$C_L = 15 pF$ $R_L = 2k\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		24						32	ns
t_{PHL} Propagation delay	Waveform 1		17						28	ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7427
54LS/74LS27

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7427N	•	N74LS27N	
Ceramic DIP	Fig. A	N7427F	•	N74LS27F	S5427F • S54LS27F
Flatpak	Fig. A				S5427W • S54LS27W

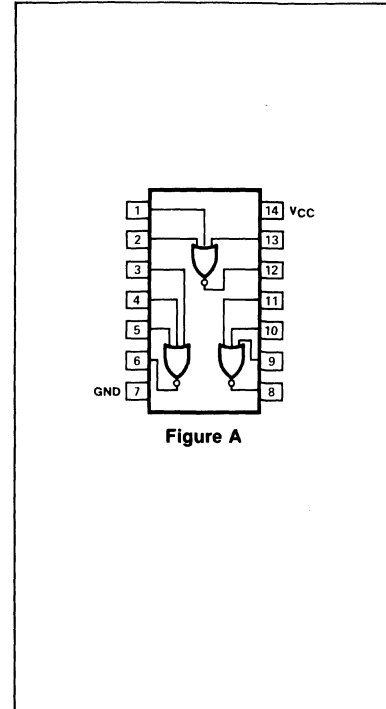


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.36
Outputs	I_{OH} (μA)	-800			-400
	I_{OL} (mA)	16			4/8 (a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$							4.0	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			26				6.8	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$						$C_L = 15 \text{ pF}$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1			15				15	ns
t_{PHL}	Propagation delay	Waveform 1			11				15	ns

NOTES

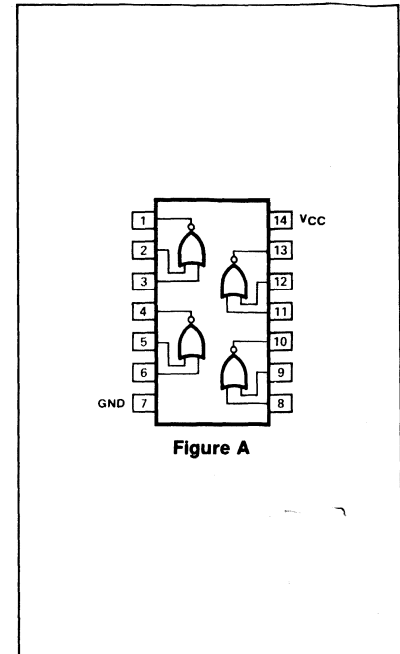
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7428
54LS/74LS28**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7428N	• N74LS28N		
Ceramic DIP	Fig. A	N7428F	• N74LS28F	S5428F	• S54LS28F
Flatpak	Fig. A			S5428W	• S54LS28W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.4
Outputs	I_{OH} (μA)	-2400			-1200
	I_{OL} (mA)	48			12/24 (a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{OS}	Output short circuit current $V_{CC} = \text{Max}, V_{OUT} = 0V$	-70	-180					-30	-100	mA
I_{CCH}	Supply current $V_{CC} = \text{Max}, V_{IN} = 0V$		21						3.6	mA
I_{CCL}	Supply current $V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		57						13.8	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$R_L = 133\Omega$						$C_L = 45pF$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay Waveform 1		9.0 (c)						24	ns
t_{PHL}			12 (c)						24	ns
t_{PLH}	Propagation delay Waveform 1		15 (d)							ns
t_{PHL}			18 (d)							ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. $C_L = 50pF$ for 54/7428
- d. $C_L = 150pF$ for 54/7428

54/7430
54H/74H30
54LS/74LS30

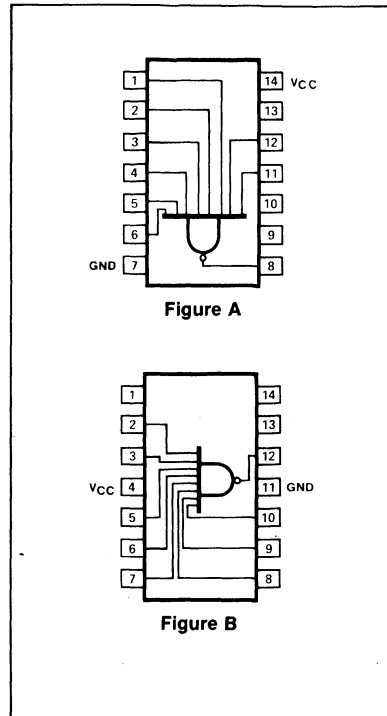
ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	Fig. A Fig. A	N7430N • N74H30N N74LS30N	
Ceramic DIP	Fig. A Fig. A	N7430F • N74H30F N74LS30F	S5430F • S54H30F S54LS30F
Flatpak	Fig. B Fig. A		S5430W • S54H30W S54LS30W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50		20
	I_{IL} (mA)	-1.6	-2.0		-0.4
Outputs	I_{OH} (μA)	-400	-500		-400
	I_{OL} (mA)	16	20		$4/8^{(a)}$

PIN CONFIGURATIONS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			2.0		4.2		0.5	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			6.0		10		1.1	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 pF$ $R_L = 400 \Omega$		$C_L = 15 pF$ $R_L = 280 \Omega$				$C_L = 15 pF$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1			22		10		15	ns
t_{PHL}	Propagation delay	Waveform 1			15		12		20	ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7432
54S/74S32
54LS/74LS32**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7432N • N74S32N N74LS32N	
Ceramic DIP	Fig. A Fig. A	N7432F • N74S32F N74LS32F	S5432F • S54S32F S54LS32F
Flatpak	Fig. A Fig. A		S5432W • S54S32W S54LS32W

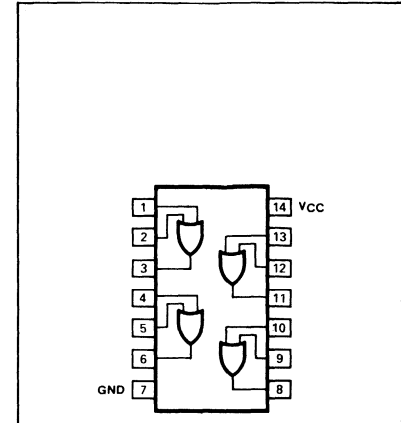


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40		50	20
	I_{IL} (mA)	-1.6		-2.0	-0.36
Outputs	I_{OH} (μA)	-800		-1000	-400
	I_{OL} (mA)	16		20	4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			22			32	6.2	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			38			68	9.8	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$				$C_L = 15 \text{ pF}$ $R_L = 280 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 2K \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 2			15			7.0	22	ns
t_{PHL}	Propagation delay	Waveform 2			22			7.0	22	ns

NOTE

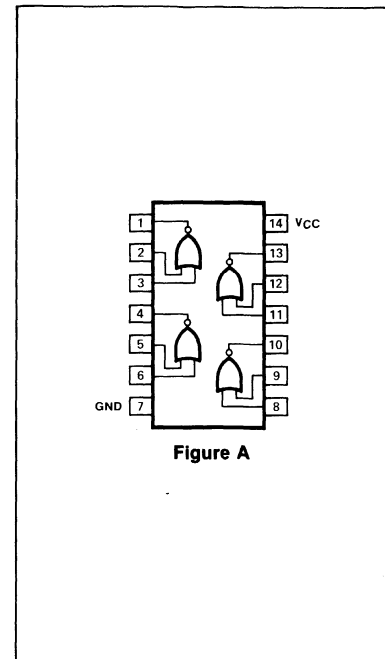
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7433
54LS/74LS33**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$	
Plastic DIP	Fig. A	N7433N	• N74LS33		
Ceramic DIP	Fig. A	N7433F	• N74LS33F	S5433F	• S54LS33F
Flatpak	Fig. A			S5433W	• S54LS33W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.4
Outputs	I_{OH} (μA)	250			250
	I_{OL} (mA)	48			12/24 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$		21				3.6		mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		57				13.8		mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$R_L = 133\Omega$						$C_L = 45pF$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	15 ^(c)						32	ns
t_{PHL}			18 ^(c)						28	ns
t_{PLH}	Propagation delay	Waveform 1	22 ^(d)							ns
t_{PHL}			24 ^(d)							ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. $C_L = 50pF$ for 54/7433.
- d. $C_L = 150pF$ for 54/7433.

**54/7437
54S/74S37
54LS/74LS37**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A Fig. A	N7437N	• N74S37N N74LS37N		
Ceramic DIP	Fig. A Fig. A	N7437F	• N74S37F N74LS37F	S5437F • S54S37F S54LS37F	
Flatpak	Fig. A Fig. A			S4537W • S54S37W S54LS37W	

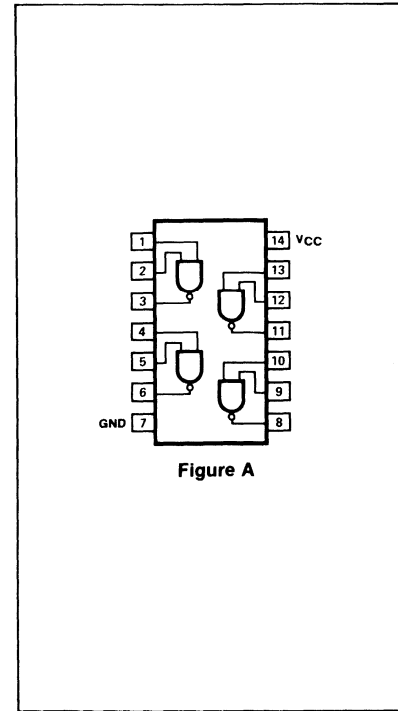


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40		100	20
	I_{IL} (mA)	-1.6		-4.0	-0.4
Outputs	I_{OH} (μA)	-1200		-3000	-1200
	I_{OL} (mA)	48		60	12/24 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$, Mil $V_{OUT} = 0V$ Com	-20	-70			-50	-225	-30	-100	mA
		-18	-70			-50	-225	-30	-100	
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		15.5				36		2.0	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		54				80		12.0	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 45pF$ $R_L = 133\Omega$				$C_L = 50pF$ $R_L = 93\Omega$		$C_L = 45pF$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		22				6.5		24	ns
t_{PHL} Propagation delay	Waveform 1		15				6.5		24	ns

NOTES

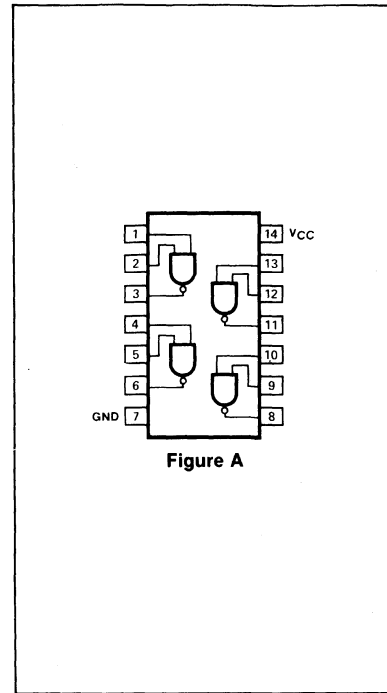
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7438
54S/74S38
54LS/74LS38**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7438N • N74S38N N74LS38N	
Ceramic DIP	Fig. A Fig. A	N7438F • N74S38F N74LS38F	S5438F • S54S38F S54LS38F
Flatpak	Fig. A Fig. A		S5438W • S54S38W S54LS38W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40		100	20
	I_{IL} (mA)	-1.6		-4.0	-0.4
Outputs	I_{OH} (μA)	250		250	250
	I_{OL} (mA)	48		60	12/24 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0$			8.5			36	2.0	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5$			54			80	12	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 45pF$ $R_L = 667\Omega$				$C_L = 50pF$ $R_L = 93\Omega$		$C_L = 45pF$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1			22			6.5	32	ns
t_{PHL}	Propagation delay	Waveform 1			18			6.5	28	ns

NOTES

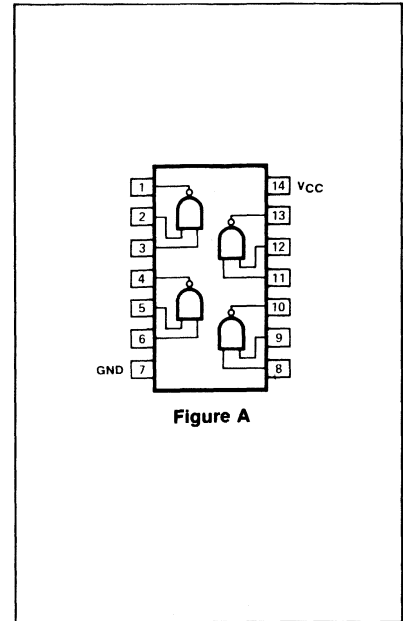
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7439

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7439N	
Ceramic DIP	Fig. A	N7439F	S5439F
Flatpak			



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			
	I_{IL} (mA)	-1.6			
Outputs	I_{OH} (μA)	250			
	I_{OL} (mA)	48			

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			8.5					mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			54					mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 133pF$ $R_L = 45\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1			22					ns
t_{PHL}	Propagation delay	Waveform 1			18					ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7440
54H/74H40
54S/74S40
54LS/74LS40

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $-70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7440N • N74H40N N74S40N • N74LS40N	
Ceramic DIP	Fig. A Fig. A	N7440F • N74H40F N74S40F • N74LS40F	S5440F • S54H40F S54S40F • S54LS40F
Flatpak	Fig. B Fig. A		S5440W • S54H40W S54S40W • S54LS40W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	100	100	20
	I_{IL} (mA)	-1.6	-4.0	-4.0	-0.4
Outputs	I_{OH} (μA)	-1200	-1500	-3000	1200
	I_{OL} (mA)	48	60	60	12/24 ^(a)

PIN CONFIGURATIONS

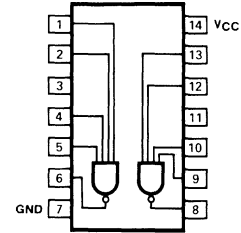


Figure A

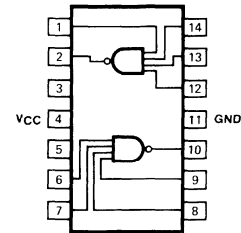


Figure B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$, Mil	-20	-70	-40	-125	-50	-225	-30	-100	mA
	$V_{OUT} = 0V$, Com	-18	-70	-40	-125	-50	-225	-30	-100	mA
I_{CCH} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		8.0		16		18		1.0	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		27		40		44		6.0	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 133\Omega$		$C_L = 25pF$ $R_L = 93\Omega$		$C_L = 50pF$ $R_L = 93\Omega$		$C_L = 45pF$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		22		12		6.5		24	ns
t_{PHL} Propagation delay	Waveform 1		15		12		6.5		24	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

**54/7442
54LS/74LS42**

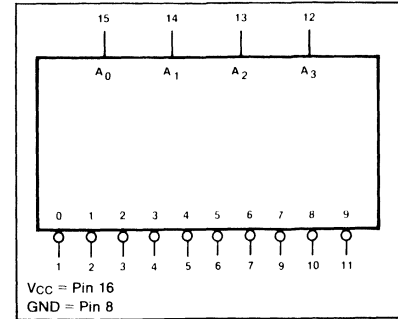
DESCRIPTION

The "42" is a multipurpose decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs.

FEATURES

- Mutually exclusive outputs
- 1-of-8 Demultiplexing capability
- Outputs disabled for input codes above nine

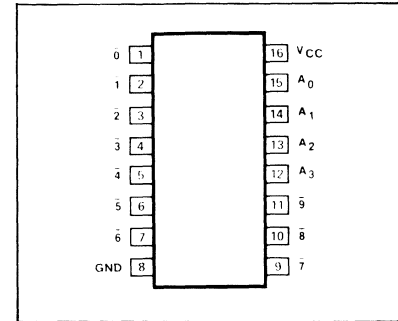
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	N7442N • N74LS42N	
Ceramic DIP	N7442F • N74LS42F	S5442F • S54LS42F
Flatpak		S5442W • S54LS42W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
$A_0 - A_3$	Address inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
$\bar{0} - \bar{9}$	Active LOW outputs	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8 (a)

NOTE

a. Slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "42" decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the "42" ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

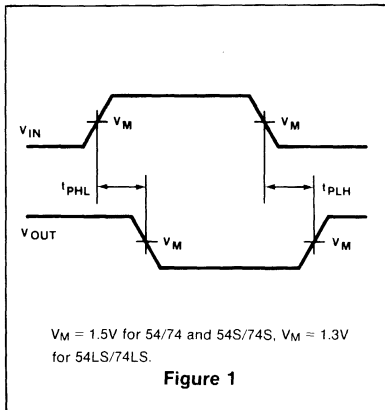
The most significant input, A₃, produces a useful inhibit function when the "42" is used as a one-of-eight decoder. The A₃ input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

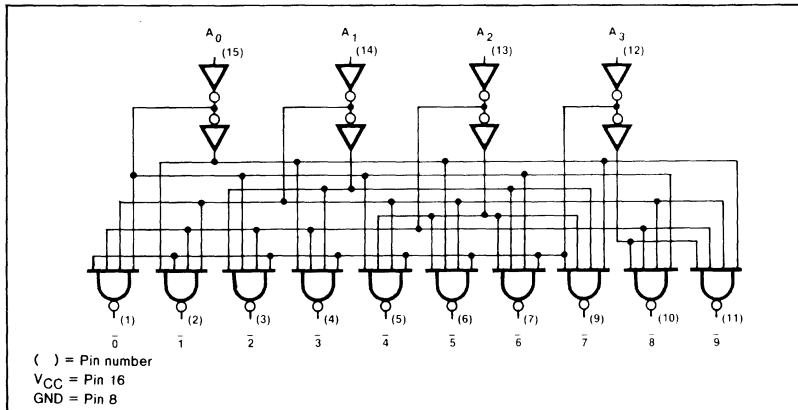
A ₃	A ₂	A ₁	A ₀	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	H	H
L	H	L	H	L	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	L	H	H	H
L	H	H	H	L	H	H	H	L	H	L	H	H	H
L	H	L	L	L	H	H	H	H	H	H	L	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H	H
L	H	H	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	L	H	H	H	H	H	H	H	L	H
H	L	L	H	L	H	H	H	H	H	H	H	L	H
H	L	H	L	L	H	H	H	H	H	H	H	L	H
H	L	H	H	L	H	H	H	H	H	H	H	L	H
H	L	L	L	L	H	H	H	H	H	H	H	L	H
H	L	L	H	L	H	H	H	H	H	H	H	L	H
H	L	H	L	L	H	H	H	H	H	H	H	L	H
H	L	H	H	L	H	H	H	H	H	H	H	L	H
H	H	L	L	L	H	H	H	H	H	H	H	L	H
H	H	L	H	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	H	L	H	H	H	H	H	H	H	L	H
H	H	L	L	L	H	H	H	H	H	H	H	L	H
H	H	L	H	L	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	L	H
H	H	H	H	L	H	H	H	H	H	H	H	L	H

H = HIGH voltage levels
L = LOW voltage levels

AC WAVEFORMS



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE ^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current	V _{CC} = Max		Mil	41		13	mA
				Com	56		13	

AC SET-UP REQUIREMENTS T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation delay	Figure 1					30	ns
t _{PHL}	Address to output						30	

NOTES

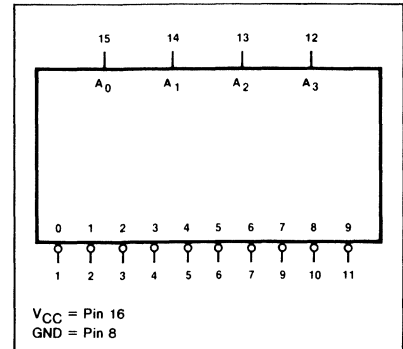
b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

54/7443

DESCRIPTION

The "43" is a TTL MSI array utilized in decoding and logic conversion applications. The "43" decodes excess-3 code numbers to 1-of-10 outputs.

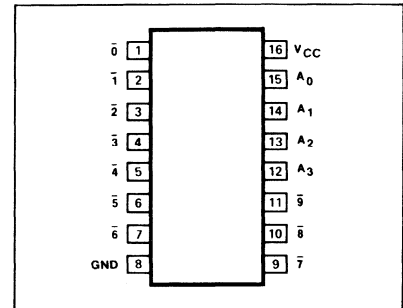
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N7443N	
Ceramic DIP	N7443F	S5443F
Flatpak		S5443W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION	54/74	54S/74S	54LS/74LS
$A_0 - A_3$	Address inputs I_{IH} (μA) I_{IL} (mA)	40 -1.6		
$\bar{0} - \bar{9}$	Active LOW inputs I_{OH} (μA) I_{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "43" is an Excess-3 to 1-of-10 decoder that accepts excess-3 coded inputs (binary range three through 12) and generates ten mutually-exclusive active LOW outputs.

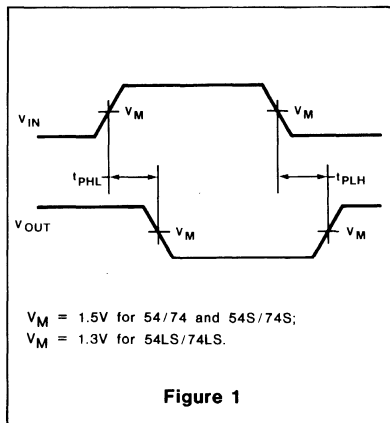
The excess-3 code is used in decimal arithmetic because of its self-complementing feature (the bit-wise complement of a number is also the nine's complement) which simplifies subtraction.

TRUTH TABLE

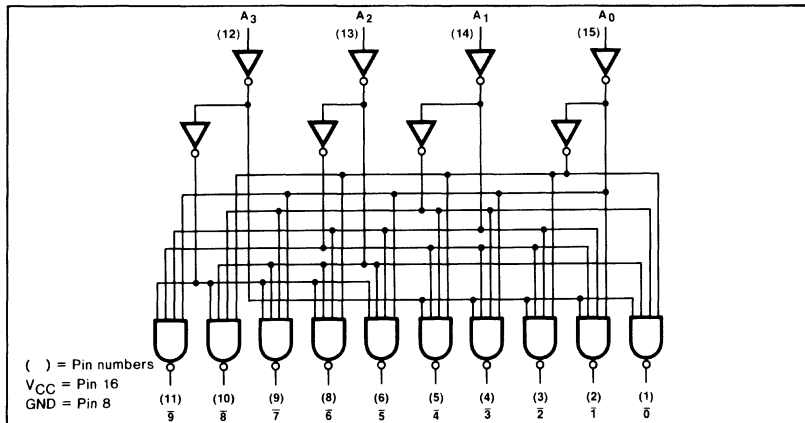
INPUTS				OUTPUTS									
A ₃	A ₂	A ₁	A ₀	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	H	H	H	L	H	H	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H	H	H
L	H	H	H	H	H	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	H	L	H	H
H	L	H	H	H	H	H	H	H	H	H	H	L	H
H	H	L	L	H	H	H	H	H	H	H	H	H	L
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage level
L = LOW voltage level

AC WAVEFORM



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil	41					mA
		Com	56					mA

AC CHARACTERISTICS: $T_A = 25^\circ C$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Figure 1		35					ns
t_{PHL} Address to output			35					ns

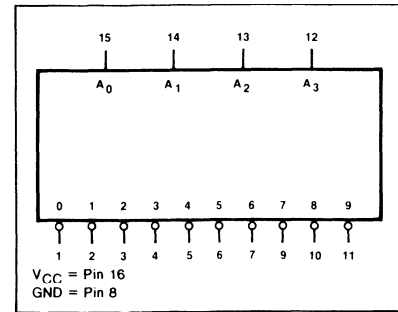
NOTE
b. For family dc Characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

54/7444

DESCRIPTION

The "44" is a TTL MSI array utilized in decoding and logic conversion applications. The "44" decodes excess-three-gray code to 1-of-10 outputs.

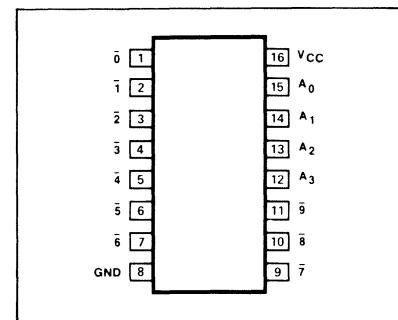
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ\text{C}$ to $+70^\circ\text{C}$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
Plastic DIP	N7444N	
Ceramic DIP	N7444F	S5444F
Flatpak		S5444W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_0-A_3	Address inputs	I_{IH} (μA)	40		
		I_{IL} (mA)	-1.6		
$\bar{0}-\bar{9}$	Active LOW outputs	I_{OH} (μA)	-800		
		I_{OL} (mA)	16		

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil	41					mA
		Com	56					mA

NOTES

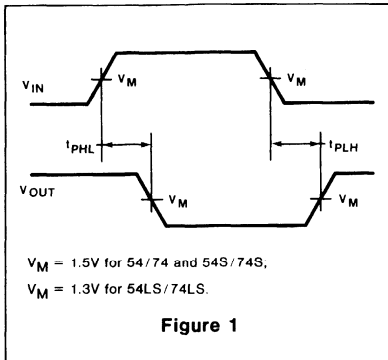
- a. The slashed numbers indicate different parametric values for Military / Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

FUNCTIONAL DESCRIPTION

The "44" is an Excess-3-Gray code to 1-of-10 decoder that accepts excess-3 Gray coded inputs and generates ten mutually exclusive active LOW outputs.

The excess-3 Gray code is used in decimal position encoders, since it retains the characteristics of a Gray code (only one bit changes between adjacent states) even on the change between nine and zero.

AC WAVEFORM

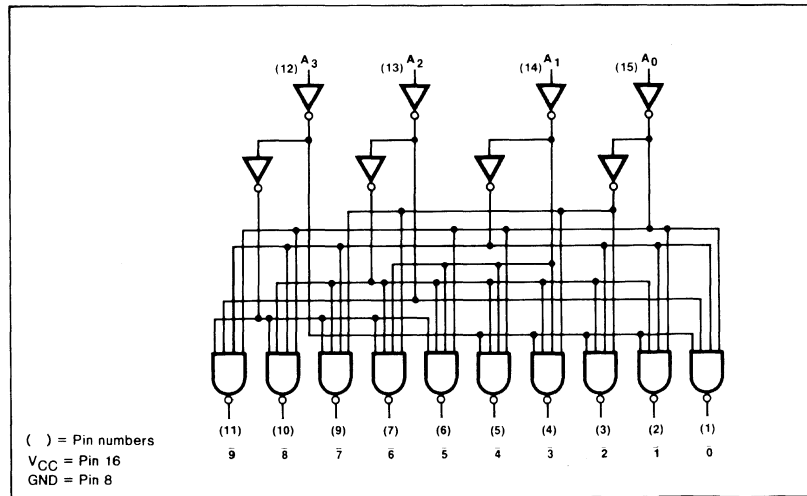


TRUTH TABLE

INPUTS				OUTPUTS									
A ₃	A ₂	A ₁	A ₀	0	1	2	3	4	5	6	7	8	9
L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	H	L	H	H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage level.
 L = LOW voltage level.

LOGIC DIAGRAM



AC CHARACTERISTICS: $T_A = 25^\circ C$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Figure 1		35					ns
t_{PHL} Address to output			35					ns

54/7445

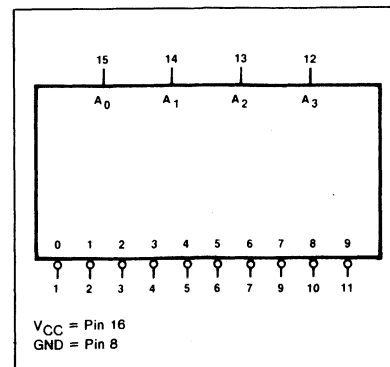
DESCRIPTION:

The "45" is a TTL MSI array. It features standard TTL inputs and high voltage, high current (80mA) outputs. The "45" minimum output breakdown is 30 volts.

FEATURES

- 80mA output sink capability
- 30V output breakdown voltage
- Ideally suited as lamp or solenoid driver
- See "42" for standard TTL output version
- See "145" for "LS" version

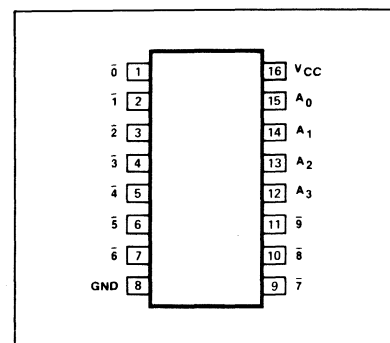
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ\text{C}$ to $+70^\circ\text{C}$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
Plastic DIP	N7445N	
Ceramic DIP	N7445F	S5445F
Flatpak		S5445W

PIN CONFIGURATION

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_0 to A_3	Address inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
$\bar{0}$ to $\bar{9}$	Active LOW outputs	I_{OH} (μA) I_{OL} (mA)	+250 80		

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$ $I_{OL} = 80\text{mA}$ $I_{OL} = 20\text{mA}$		0.9					V
			0.4					V
I_{OH} Output HIGH current	$V_{CC} = \text{Min}$, $V_{OUT} = 30\text{V}$		250					μA
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil	62					mA
		Com	70					mA

NOTES

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

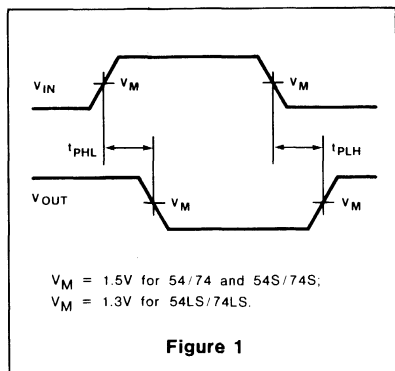
FUNCTIONAL DESCRIPTION

The "45" decoder accepts BCD inputs on the A₀ to A₃ address lines and generates ten mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are off. This device can therefore be used as a 1-of-8 decoder with A₃ used as an active LOW enable.

The "45" can sink 20mA while maintaining the standardized guaranteed output LOW voltage (V_{OL}) of 0.4V, but it can sink up to 80mA with a guaranteed V_{OL} of less than 0.9V.

The "45" features an output breakdown voltage of 30V and is ideally suited as a lamp and solenoid driver.

AC WAVEFORMS

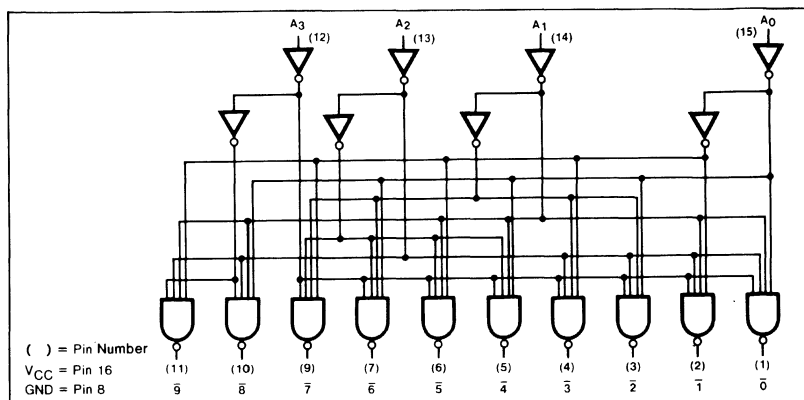


TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

LOGIC DIAGRAM



AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 100Ω						
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay	Figure 1		50					ns
t _{PHL} Address to output			50					ns

54/7446A
54/7447A

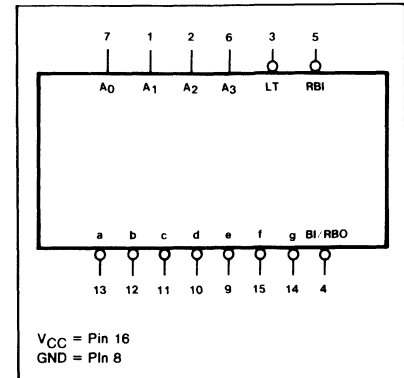
DESCRIPTION

The "46" and "47" are BCD to 7-Segment Decoder/Drivers with open collector outputs. They accept 4-bit BCD data and provide seven active LOW decoded outputs to drive 7-segment incandescent displays directly. Their 40mA output sink current capability makes them useful for driving multiplexed common anode LED displays. Both devices feature overriding lamp test (all segments "on") and ripple blanking for leading and trailing zeroes.

FEATURES

- 40mA output current sink per segment
- 30V segment voltage on 54/7446A
- 15V segment voltage on 54/7447A
- Overriding lamp test
- Ripple Blanking for leading and trailing zeroes

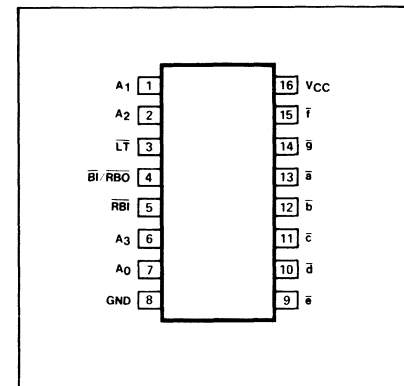
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N7446AN	
	N7447AN	
Ceramic DIP	N7446AF	S5446AF
	N7447AF	S5447AF
Flatpak		

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A ₀ -A ₃	BCD Address inputs	I _{IH} (μA)	40		
		I _{IL} (mA)	-1.6		
\overline{LT}	Lamp Test (active LOW) input	I _{IH} (μA)	40		
		I _{IL} (mA)	-1.6		
\overline{RBI}	Ripple Blanking (active LOW) input	I _{IH} (μA)	40		
		I _{IL} (mA)	-1.6		
$\overline{BI}/\overline{RBO}$	Blanking (active LOW) input	I _{IH} (μA)	N.A.		
		I _{IL} (mA)	-4.0		
$\overline{BI}/\overline{RBO}$	Ripple Blanking (active LOW) output	I _{OH} (μA)	-200		
		I _{OL} (mA)	8.0		
$\overline{a}-\overline{g}$	Seven-segment (active LOW) outputs	I _{OH} (μA)	+250		
		I _{OL} (mA)	40		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "46A" and "47A" 7-segment decoders accept a 4-bit BCD code input and produce the appropriate outputs for selection of segments in a 7-segment matrix display used for representing the decimal numbers "0-9." The seven outputs (\bar{a} , \bar{b} , \bar{c} , \bar{d} , \bar{e} , \bar{f} , \bar{g}) of the decoder select the corresponding segments in the matrix shown in Figure A. The numeric designations chosen to represent the decimal numbers are shown in Figure B, together with the resulting displays for input code configurations in excess of binary "9."

The "46A" and "47A" have provisions for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability, 0070.0500 would be displayed as 70.05. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{BI}/\overline{RBO}$) of a decoder to the Ripple Blanking Input (\overline{RBI}) of the next lower stage device. The most significant decoder stage should have the \overline{RBI} input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the \overline{RBI} input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{BI}/\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of open collector gates.

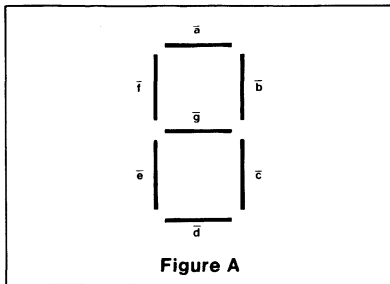


Figure A

NOTE

b. $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input (\overline{BI}) and/or ripple-blanking output (\overline{RBO}). The blanking out (\overline{BI}) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (\overline{RBI}) must be open or at a HIGH level if blanking of a decimal 0 is not desired.

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS						
	LT	\overline{RBI}	A ₃	A ₂	A ₁	A ₀	$\overline{BI}/\overline{RBO}(b)$	\bar{a}	\bar{b}	\bar{c}	\bar{d}	\bar{e}	\bar{f}	\bar{g}
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
$\overline{BI}(b)$	X	X	X	X	X	X	L	H	H	H	H	H	H	H
$\overline{RBI}(b)$	H	L	L	L	L	L	L	H	H	H	H	H	H	H
\overline{LT}	L	X	X	X	X	X	H	L	L	L	L	L	L	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

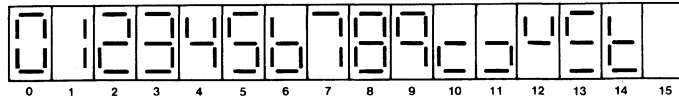
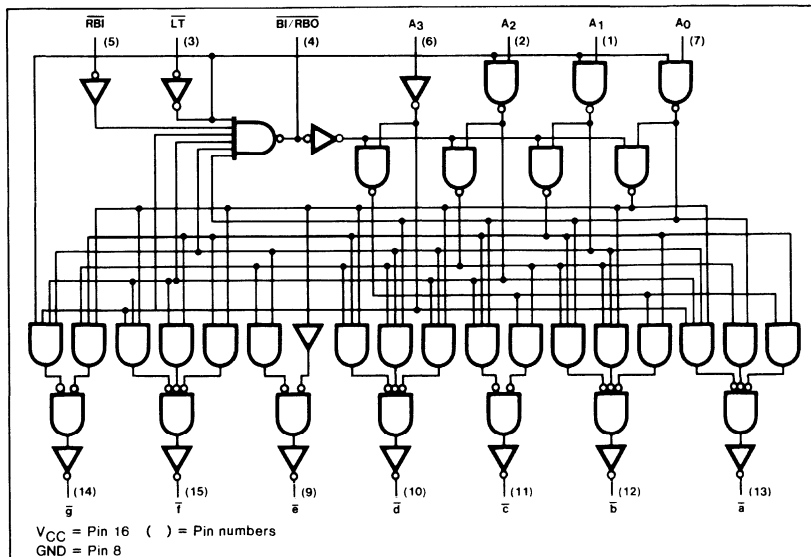


Figure B

LOGIC DIAGRAM



V_{CC} = Pin 16 () = Pin numbers
GND = Pin 8

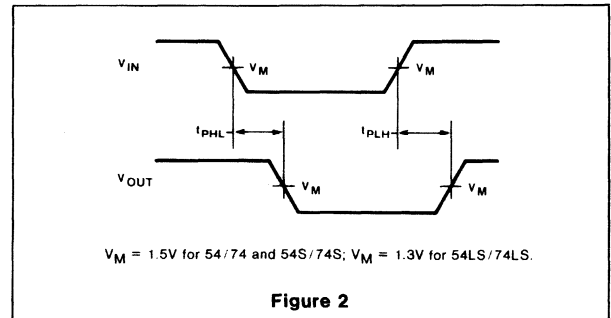
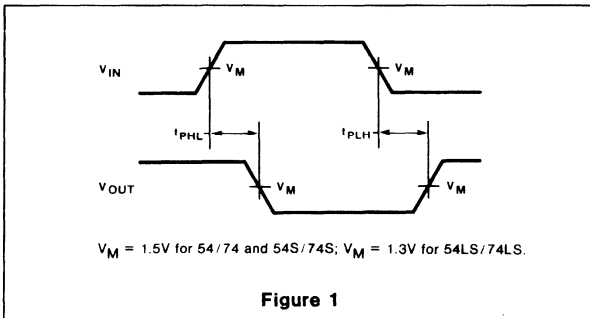
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(c)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{OH} Output HIGH current \bar{a} - \bar{g} outputs	V _{CC} = Max	V _{OUT} = 30V 54/7446A		250				μA
		V _{OUT} = 15V 54/7447A		250				μA
V _{OL} Output LOW voltage \bar{a} - \bar{g} outputs	V _{CC} = Max, I _{OL} = 40mA		0.4					V
V _{OL} Output LOW voltage \bar{BI}/\bar{RBO} output	V _{CC} = Min, I _{OL} = 8mA		0.4					V
I _{CC} Supply current	V _{CC} = Max	Mil.	85					mA
		Com.	103					mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 120Ω						
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay any input to any output	Figures 1 and 2		100					ns
t _{PHL}		100					ns	

AC WAVEFORMS



c. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

54/7448

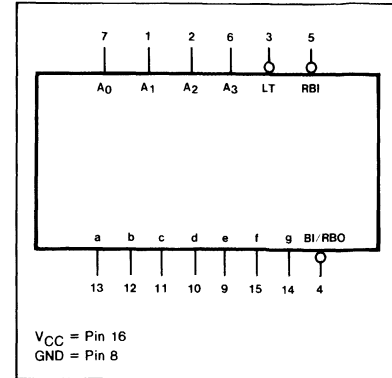
DESCRIPTION

The "48" is a BCD to 7-Segment Decoder. It accepts 4-bit BCD data and provides seven active HIGH decoded outputs to drive 7-segment displays of various types. It is used primarily with high current or high voltage NPN transistors or segment drivers in multiplexed LED, incandescent, electro-luminescent or gas discharge 7-segment display applications. It features overriding lamp test (all segments "on") and ripple blanking for leading and trailing zeroes.

FEATURES

- Active HIGH outputs
- Resistor pull-ups for driving NPN transistors directly
- Overriding lamp test
- Ripple Blanking for leading and trailing zeroes

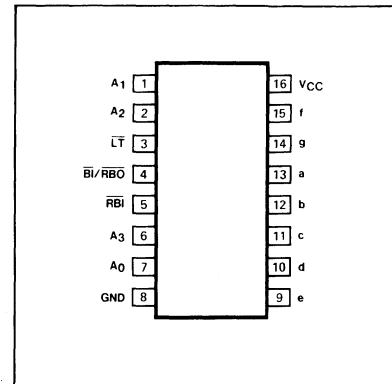
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N7448N	
Ceramic DIP	N7448F	S5448F
Flatpak		

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A ₀ -A ₃	BCD Address inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
\overline{LT}	Lamp Test (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
\overline{RBI}	Ripple Blanking (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
$\overline{BI/RBO}$	Blanking (active LOW) input	I _{IH} (μA) I _{IL} (mA)	N.A. -4.0		
$\overline{BI/RBO}$	Ripple Blanking (active LOW) output	I _{OH} (μA) I _{OL} (mA)	-200 8.0		
a-g	Seven-segment outputs	I _{OH} (μA) I _{OL} (mA)	-400 6.4		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "48" 7-segment decoder accepts a 4-bit BCD code input and produces the appropriate outputs for selection of segments in a 7-segment matrix display used for representing the decimal numbers "0-9." The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure A. The numeric designations chosen to represent the decimal numbers are shown in Figure B together with the resulting displays for input code configurations in excess of binary "9."

The decoder has active HIGH outputs so a buffer transistor may be used directly to provide the high currents required for multiplexed LED displays. If additional base drive current is required external resistors may be added from the supply voltage to the 7-segment outputs of the decoders. The value of this resistor is constrained by the 6.4mA current sinking capability of the output transistors of the circuit.

The "48" has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking

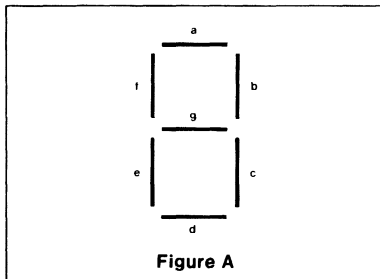


Figure A

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS							OUTPUTS						
	LT	RBI	A ₃	A ₂	A ₁	A ₀	BI/RBO(b)	a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H
5	H	X	L	H	L	H	H	H	L	H	L	L	H	H
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H
9	H	X	H	L	L	H	H	H	H	L	L	L	H	H
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L
BI(b)	X	X	X	X	X	X	L	L	L	L	L	L	L	L
RBI(b)	H	L	L	L	L	L	L	L	L	L	L	L	L	L
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

NUMERICAL DESIGNATIONS—RESULTANT DISPLAYS

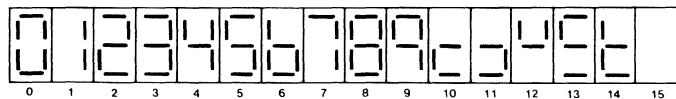
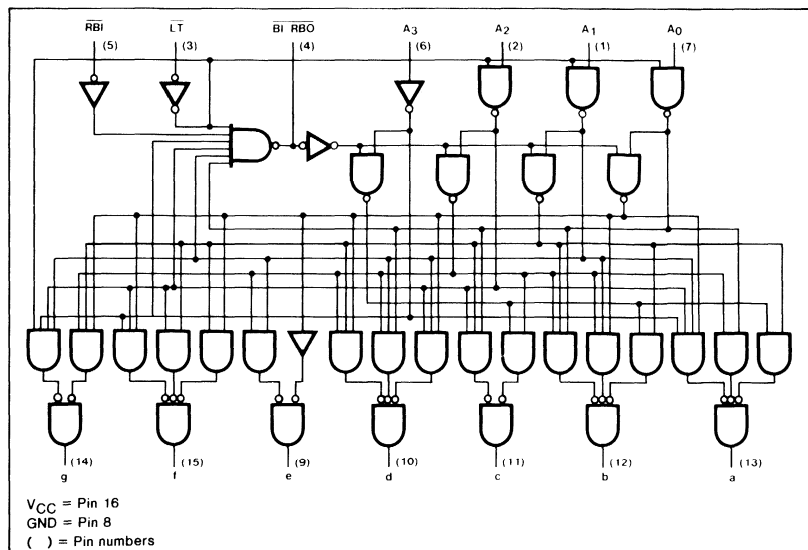


Figure B

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
() = Pin numbers

NOTE

- b. BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired.

Output ($\overline{BI}/\overline{RBO}$) of a decoder to the Ripple Blanking Input (\overline{RBI}) of the next lower stage device. The most significant decoder stage should have the \overline{RBI} input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the \overline{RBI} input of this decoder stage should be left open. A similar procedure for the

fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{BI}/\overline{RBO}$ terminal of the decoder can be OR-tied with

a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency combinations and enables a check to be made on possible display malfunctions. The $\overline{BI}/\overline{RBO}$ terminal of the decoder can be OR-tied with

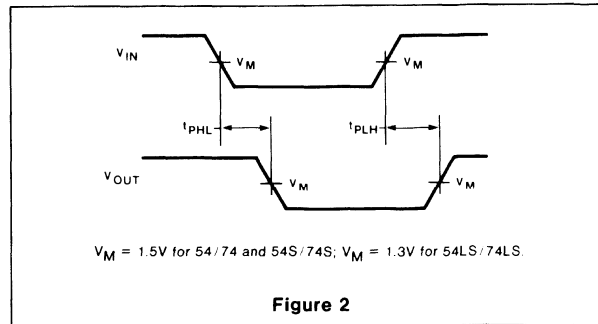
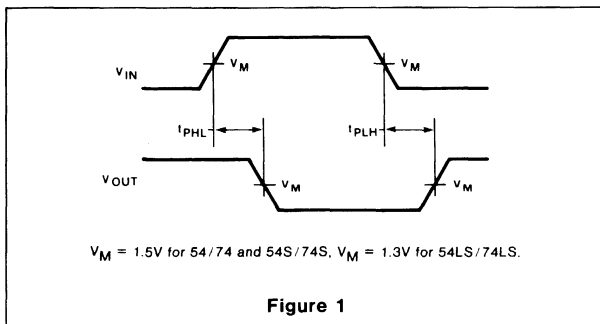
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(c)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{OA} Available output current a-g outputs	$V_{CC} = \text{Min}, V_{OUT} = 0.85V$ outputs HIGH	-1.3						mA
V_{OL} Output LOW voltage a-g outputs	$V_{CC} = \text{Min}, I_{OL} = 6.4mA$		0.4					V
V_{OL} Output LOW voltage $\overline{BI}/\overline{RBO}$ output	$V_{CC} = \text{Min}, I_{OL} = 8mA$		0.4					V
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil	76					mA
		Com.	90					mA

AC CHARACTERISTICS: $T_A = 25^\circ C$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 1k\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay any input to any output	Figures 1 and 2		100					ns
t_{PHL}			100					ns

AC WAVEFORMS



NOTE

c. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications

54/7450
54H/74H50

PIN CONFIGURATIONS

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7450N	• N74H50N		
Ceramic DIP	Fig. A	N7450F	• N74H50F	S5450F	• S54H50F
Flatpak	Fig. B			S5450W	• S54H50W

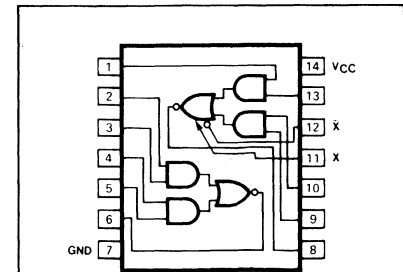


Figure A

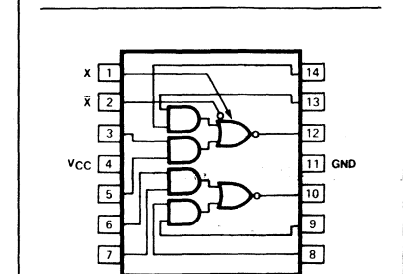


Figure B

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50		
	I_{IL} (mA)	-1.6	-2.0		
Outputs	I_{OH} (μA)	-400	-500		
	I_{OL} (mA)	16	20		

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$		8.0		12.8					mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5$		14		24					mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$		$C_L = 25pF$ $R_L = 280\Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		22 15		11 11					ns ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

DC CHARACTERISTICS (using expander inputs, $V_{CC} = 4.5V$, $T_A = -55^\circ C$)

PARAMETER	TEST CONDITIONS	5450		54H50		Min	Max	Min	Max	UNIT
		Min	Max	Min	Max					
$I_{\bar{X}}$ Expander current	$V_{\bar{X}X} = 0.4V, I_{OL} = 16mA$		-2.9							mA
	$V_X = 1.4V, I_X = 0, I_{OL} = 0$				-5.85					mA
$V_{BE(Q)}$ Base-Emitter voltage of output transistor	$I_X + I_{\bar{X}} = 410\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 16mA$		1.1							V
	$I_X + I_{\bar{X}} = 700\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 20mA$				1.1					V
V_{OH} Output HIGH voltage	$I_X = 150\mu A, I_{\bar{X}} = -150\mu A$ $I_{OH} = -400\mu A$	2.4								V
	$I_X = 320\mu A, I_{\bar{X}} = -320\mu A$ $I_{OH} = -500\mu A$			2.4						V
V_{OL} Output LOW voltage	$I_X + I_{\bar{X}} = 300\mu A$ $R_{\bar{X}X} = 138\Omega, I_{OL} = 16mA$		0.4							V
	$I_X + I_{\bar{X}} = 470\mu A$ $R_{\bar{X}X} = 68\Omega, I_{OL} = 20mA$				0.4					V

DC CHARACTERISTICS (using expander inputs, $V_{CC} = 4.75V$, $T_A = 0^\circ C$)

PARAMETER	TEST CONDITIONS	7450		74H50		Min	Max	Min	Max	UNIT
		Min	Max	Min	Max					
$I_{\bar{X}}$ Expander current	$V_{\bar{X}X} = 0.4V, I_{OL} = 16mA$		-3.1							mA
	$V_X = 1.4V, I_X = 0, I_{OL} = 0$				-6.3					mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor	$I_X + I_{\bar{X}} = 620\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 16mA$		1.0							V
	$I_X + I_{\bar{X}} = 1.1mA$ $R_{\bar{X}X} = 0, I_{OL} = 20mA$				1.0					V
V_{OH} Output HIGH voltage	$I_X = 270\mu A, I_{\bar{X}} = -270\mu A$ $I_{OH} = -400\mu A$	2.4								V
	$I_X = 570\mu A, I_{\bar{X}} = -570\mu A$ $I_{OH} = -500\mu A$			2.4						V
V_{OL} Output LOW voltage	$I_X + I_{\bar{X}} = 430\mu A$ $R_{\bar{X}X} = 130\Omega, I_{OL} = 16mA$		0.4							V
	$I_X + I_{\bar{X}} = 600\mu A$ $R_{\bar{X}X} = 63\Omega, I_{OL} = 20mA$				0.4					V

54/7451
54H/74H51
54S/74S51
54LS/74LS51

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A Fig. A	N7451N N74S51N	• •	N74H51N N74LS51N	
Ceramic DIP	Fig. A Fig. A	N7451F N74S51F	• •	N74H51F N74LS51F	S5451F • S54H51F S54S51F • S54LS51F
Flatpak	Fig. B Fig. A				S5451W • S54H51W S54S51W • S54LS51W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
Outputs	I_{OH} (μA)	-400	-500	-1000	-400
	I_{OL} (mA)	16	20	20	4/8(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$		8.0		12.8		17.8		1.6	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$		14		24		22		2.8	mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$		$C_L = 25pF$ $R_L = 280\Omega$		$C_L = 15pF$ $R_L = 280\Omega$		$C_L = 15pF$ $R_L = 2k\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		22 15		11 11		5.5 5.5		20 20	ns ns

NOTES

- The slashed numbers indicate different values for Military/Commercial temperature ranges respectively.
- For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- Make no external connection to these pins on the 54/7451, 54H/74H51 & 54S/74S51.

PIN CONFIGURATIONS

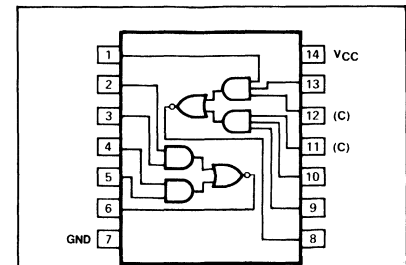


Figure A

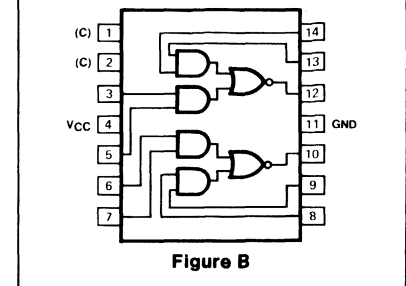


Figure B

54H/74H52

PIN CONFIGURATIONS

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74H52N	
Ceramic DIP	Fig. A	N74H52F	S54H52F
Flatpak	Fig. B		S54H52W

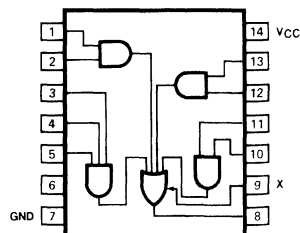


Figure A

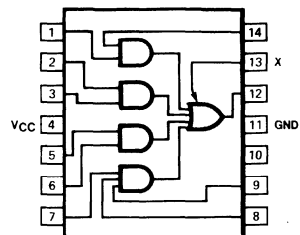


Figure B

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)		50		
	I_{IL} (mA)		-2.0		
Outputs	I_{OH} (μA)		-500		
	I_{OL} (mA)		20		

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_X Expander Current	$V_{CC} = \text{Min}, V_X = 1.0V, I_{OH} = -500\mu A, T_A = -55^\circ C$			-2.7	-4.5					mA
	$T_A = 0^\circ C$			-2.9	-5.35					mA
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}, V_X = 1.0V, T_A = \text{Min}, I_{OH} = -500\mu A$			2.4						V
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}, I_X = -300\mu A, T_A = \text{Max}, I_{OL} = 20mA$				0.4					V
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$				31					mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$				24					mA

AC CHARACTERISTICS: $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				$C_L = 25pF, R_L = 280\Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 2				15 15					

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7453
54H/74H53

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7453N	• N74H53N		
Ceramic DIP	Fig. A	N7453F	• N74H53F	S5453F	• S54H53F
Flatpak	Fig. B			S5453W	• S54H53W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50		
	I_{IL} (mA)	-1.6	-2.0		
Outputs	I_{OH} (μA)	-400	-500		
	I_{OL} (mA)	16	20		

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$			8.0		11			mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$			9.5		14			mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$		$C_L = 25pF$ $R_L = 280\Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1			22 15		11 11			ns ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc Characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. These pins are not internally connected on the 54/7453.

PIN CONFIGURATIONS

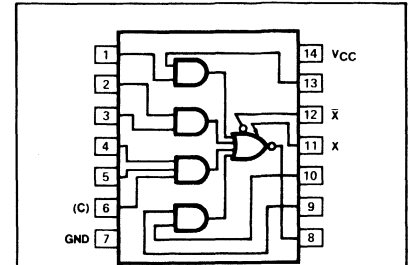


Figure A

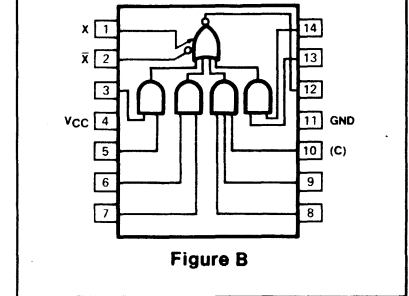


Figure B

DC CHARACTERISTICS using expander inputs, $V_{CC} = 4.5V$, $T_A = -55^\circ C$

PARAMETER	TEST CONDITIONS	5453		54H53		Min	Max	Min	Max	UNIT
		Min	Max	Min	Max					
I_X Expander current	$V_{\bar{X}X} = 0.4V, I_{OL} = 16mA$		-2.9							mA
	$V_X = 1.4V, I_X = 0, I_{OL} = 0$				-5.85					mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor	$I_X + I_{\bar{X}} = -410\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 16mA$		1.1							V
	$I_X + I_{\bar{X}} = 700\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 20mA$				1.1					V
V_{OH} Output HIGH voltage	$I_X = 150\mu A, I_{\bar{X}} = -150\mu A$ $I_{OH} = -400\mu A$	2.4								V
	$I_X = 320\mu A, I_{\bar{X}} = -320\mu A$ $I_{OH} = -500\mu A$			2.4						V
V_{OL} Output LOW voltage	$I_X + I_{\bar{X}} = 300\mu A$ $R_{\bar{X}X} = 138\Omega, I_{OL} = 16mA$		0.4							V
	$I_X + I_{\bar{X}} = 470\mu A$ $R_{\bar{X}X} = 68\Omega, I_{OL} = 20mA$				0.4					V

DC CHARACTERISTICS using expander inputs, $V_{CC} = 4.75V$, $T_A = 0^\circ C$

PARAMETER	TEST CONDITIONS	7453		74H53		Min	Max	Min	Max	UNIT
		Min	Max	Min	Max					
I_X Expander current	$V_{\bar{X}X} = 0.4V, I_{OL} = 16mA$		-3.1							mA
	$V_X = 1.4V, I_X = 0, I_{OL} = 0$				-6.3					mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor	$I_X + I_{\bar{X}} = 620\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 16mA$		1.0							V
	$I_X + I_{\bar{X}} = 1.1mA$ $R_{\bar{X}X} = 0, I_{OL} = 20mA$				1.0					V
V_{OH} Output HIGH voltage	$I_X = 270\mu A, I_{\bar{X}} = -200\mu A$ $I_{OH} = -400\mu A$	2.4								V
	$I_X = 570\mu A, I_{\bar{X}} = -570\mu A$ $I_{OH} = -500\mu A$			2.4						V
V_{OL} Output LOW voltage	$I_X + I_{\bar{X}} = 430\mu A$ $R_{\bar{X}X} = 130\Omega, I_{OL} = 16mA$		0.4							V
	$I_X + I_{\bar{X}} = 600\mu A$ $R_{\bar{X}X} = 63\Omega, I_{OL} = 20mA$				0.4					V

54/7454
54H/74H54
54LS/74LS54

PIN CONFIGURATIONS

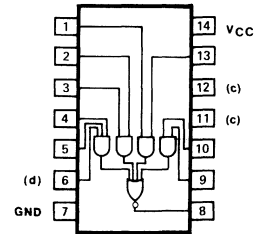


Figure A

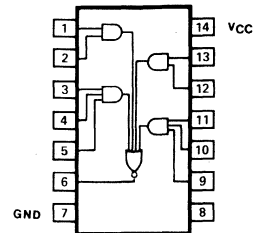


Figure B

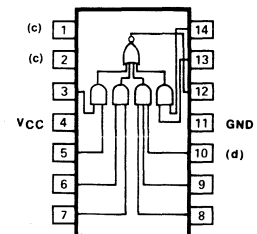


Figure C

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7454N	• N74H54N		
	Fig. B		N74LS54N		
Ceramic DIP	Fig. A	N7454F	• N74H54F	S5454F	• S54H54F
	Fig. B		N74LS54F		S54LS54F
Flatpak	Fig. C			S5454W	• S54H54W
	Fig. B				S54LS54W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50		20
	I_{IL} (mA)	-1.6	-2.0		-0.36
Outputs	I_{OH} (μA)	-400	-500		-400
	I_{OL} (mA)	16	20		4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		8.0		11				1.6	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$, $V_{IN} \geq 4.5V$		9.5		14				2.0	mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 \text{ pF}$ $R_L = 400\Omega$		$C_L = 25 \text{ pF}$ $R_L = 280\Omega$				$C_L = 15 \text{ pF}$ $R_L = 2k\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		22 15		11 11				20 20	ns ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. Make no external connection to these pins on the 54/7454 and 54H/74H54.
- d. These pins are not internally connected on the 54/7454.

54H/74H55
54LS/74LS55
*LS55 is not expandable

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N74H55N N74LS55N	
Ceramic DIP	Fig. A Fig. A	N74H55F N74LS55F	S54H55F S54LS55F
Flatpak	Fig. B Fig. A		S54H55W S54LS55W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)		50		20
	I_{IL} (mA)		-2.0		-0.36
Outputs	I_{OH} (μA)		-500		-400
	I_{OL} (mA)		20		4/8(a)

PIN CONFIGURATIONS

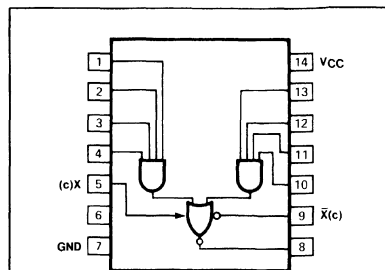


Figure A

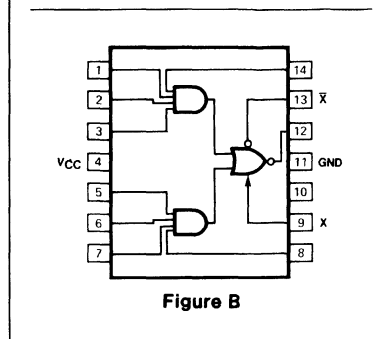


Figure B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$				6.4				0.8	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$				12				1.3	mA

AC CHARACTERISTICS $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				$C_L = 25pF$ $R_L = 280\Omega$				$C_L = 15pF$ $R_L = 2K\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1				11				20	ns ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. Make no external connection to these pins for the 54LS/74LS55.

DC CHARACTERISTICS using expander inputs, $V_{CC} = 4.5V$, $T_A = -55^\circ C$

PARAMETER	TEST CONDITIONS	54H55								UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_X Expander current	$V_{\bar{X}X} = 0.4V, I_{OL} = 16mA$									mA
	$V_X = 1.4V, I_X = 0, I_{OL} = 0$				-5.85					mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor	$I_X + I_{\bar{X}} = 410\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 16mA$									V
	$I_X + I_{\bar{X}} = 700\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 20mA$				1.1					V
V_{OH} Output HIGH voltage	$I_X = 150\mu A, I_{\bar{X}} = -150\mu A$ $I_{OH} = -400\mu A$									V
	$I_X = 320\mu A, I_{\bar{X}} = -320\mu A$ $I_{OH} = -500\mu A$			2.4						V
V_{OL} Output LOW voltage	$I_X + I_{\bar{X}} = 300\mu A$ $R_{\bar{X}X} = 138\Omega, I_{OL} = 16mA$									V
	$I_X + I_{\bar{X}} = 470\mu A$ $R_{\bar{X}X} = 68\Omega, I_{OL} = 20mA$				0.4					V

DC CHARACTERISTICS using expander inputs, $V_{CC} = 4.75V$, $T_A = 0^\circ C$

PARAMETER	TEST CONDITIONS	74H55								UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_X Expander current	$V_{\bar{X}X} = 0.4V, I_{OL} = 16mA$									mA
	$V_X = 1.4V, I_X = 0, I_{OL} = 0$				-6.3					mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor	$I_X + I_{\bar{X}} = 620\mu A$ $R_{\bar{X}X} = 0, I_{OL} = 16mA$									V
	$I_X + I_{\bar{X}} = 1.1mA$ $R_{\bar{X}X} = 0, I_{OL} = 20mA$				1.0					V
V_{OH} Output HIGH voltage	$I_X = 270\mu A, I_{\bar{X}} = -270\mu A$ $I_{OH} = -400\mu A$									V
	$I_X = 570\mu A, I_{\bar{X}} = -570\mu A$ $I_{OH} = -500\mu A$			2.4						V
V_{OL} Output LOW voltage	$I_X + I_{\bar{X}} = 430\mu A$ $R_{\bar{X}X} 130\Omega, I_{OL} = 16mA$									V
	$I_X + I_{\bar{X}} = 600\mu A$ $R_{\bar{X}X} 63\Omega, I_{OL} = 20mA$				0.4					V

54/7460
54H/74H60

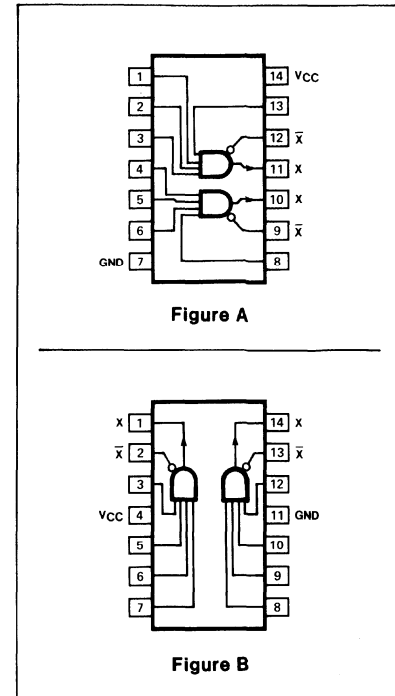
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7460N	• N74H60N		
Ceramic DIP	Fig. A	N74H60F	• N74H60F	S5460F	• S54H60F
Flatpak	Fig. B			S5460W	• S54H60W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40	50		
	I_{IL} (mA)	-1.6	-2.0		
Outputs	I_{OH} (μA)	N/A	N/A		
	I_{OL} (mA)	N/A	N/A		

PIN CONFIGURATIONS



DC CHARACTERISTICS FOR EXPANDER DEVICES(b)

PARAMETER		TEST CONDITIONS						54/74		54H/74H		UNIT
		V_{CC}	V_{IN}	V_X	$V_{\bar{X}}$	$I_{\bar{X}}$	R_X	T_A	Min	Max	Min	
$V_{\bar{X}X}$	Voltage drop across outputs	4.5V	2.0V	1.1V		3.8mA		-55°C	0.4			V
		4.5V	2.0V	1.1V		5.85mA		-55°C			0.4	V
		4.75V	2.0V	1.0V		3.5mA		0°C	0.4			V
		4.75V	2.0V	1.0V		6.3mA		0°C			0.4	V
		5.5V	2.0V	1.0V		7.85mA		125°C			0.4	V
		5.25V	2.0V	1.0V		7.4mA		70°C			0.4	V
$I_{X(on)}$	On-state expander current	4.5V	2.0V	1.1V		0		-55°C	-300		-470	μA
		4.75V	2.0V	1.0V		0		0°C	-430		-600	μA
$I_{\bar{X}(off)}$	Off-state expander current	4.5V	0.8V		4.5V	1.2K		-55°C	150			μA
		4.5V	0.8V		4.5V	575 Ω		-55°C			320	μA
		4.75V	0.8V		4.5V	1.2K		0°C	270			μA
		4.75V	0.8V		4.5V	575 Ω		0°C			570	μA
$I_{CC(on)}$	Supply current	Max	4.5V	0.85V		0		all	2.5		3.5	mA
		Max	0V	0.85V		0		all	4.0		4.5	mA

NOTES

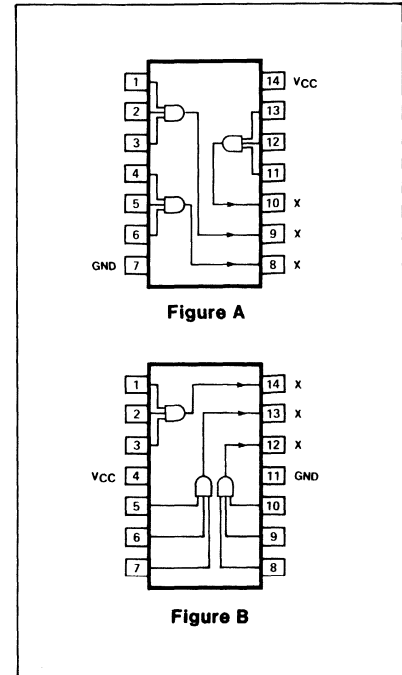
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc Characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54H/74H61

PIN CONFIGURATIONS

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74H61N	
Ceramic DIP	Fig. A	N74H61F	S54H61F
Flatpak	Fig. B		S54H61W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)		50		
	I_{IL} (mA)		-2.0		
Outputs	I_{OH} (μA)		N/A		
	I_{OL} (mA)		N/A		

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{X(on)}$ Output "on" voltage	$V_{CC} = \text{Min}, V_{IN} = 2V$ $I_X = 4.5mA$ $T_A = -55^\circ C$				1.0					V
					1.0					V
$I_{X(off)}$ Output "off" current	$V_{CC} = \text{Min}, V_X = 2.2V$ $T_A = \text{Max}, V_{IN} = 0.8V$				50					μA
$I_{CC(on)}$ Supply current	$V_{CC} = \text{Max}, V_{IN} > 4.5V$				16					mA
$I_{CC(off)}$ Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$				7.0					mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54H/74H62

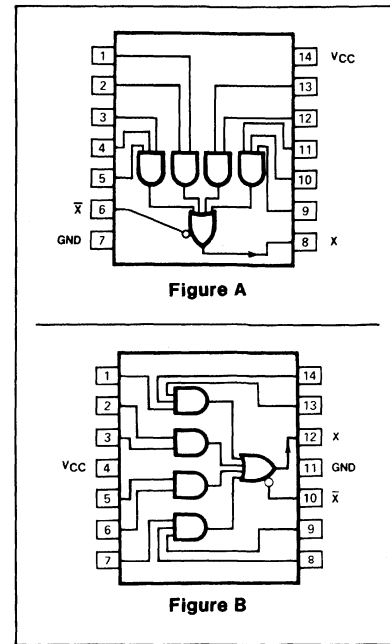
PIN CONFIGURATIONS

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	Fig. A	N74H62N	
Ceramic DIP	Fig. A	N74H62F	S54H62F
Flatpak	Fig. B		S54H62W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I _{IH} (μA)		50		
	I _{IL} (mA)		-2.0		
Outputs	I _{OH} (μA)		N/A		
	I _{OL} (mA)		N/A		



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS							54/74		54H/74H		UNIT
	V _{CC}	V _{IN}	V _X	V _{X̄}	I _{X̄}	R _X	T _A	Min	Max	Min	Max	
V _{X̄X} Voltage drop across outputs	4.5V	2.0V	1.1V		5.85mA		-55°C				0.4	V
	4.75V	2.0V	1.0V		6.3mA		0°C				0.4	V
	5.5V	2.0V	1.0V		7.85mA		125°C				0.4	V
	5.25V	2.0V	1.0V		7.4mA		70°C				0.4	V
I _{X(on)} On-state expander current	4.5V	2.0V	1.1V		0		-55°C			-470		μA
	4.75V	2.0V	1.0V		0		0°C			-600		μA
I _{X̄(off)} Off-state expander current	4.5V	0.8V		4.5V		575Ω	-55°C				320	μA
	4.75V	0.8V		4.5V		575Ω	0°C				570	μA
I _{CC(on)} Supply current I _{CC(off)}	Max	4.5V	0.85V		0		all				7.0	mA
	Max	0V	0.85V		0		all				9.0	mA

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54S/74S64

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74S64N	
Ceramic DIP	Fig. A	N74S64F	S54S64F
Flatpak	Fig. A		S54S64W

PIN CONFIGURATION

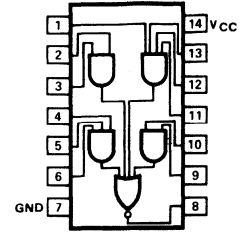


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)			50	
	I_{IL} (mA)			-2.0	
Outputs	I_{OH} (μA)			-1000	
	I_{OL} (mA)			20	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$						12.5		mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$						16		mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1						5.5		ns
t_{PHL}	Propagation delay	Waveform 1						5.5		ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial, temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54S/74S65

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74S65N	
Ceramic DIP	Fig. A	N74S65F	S54S65F
Flatpak	Fig. A		S54S65W

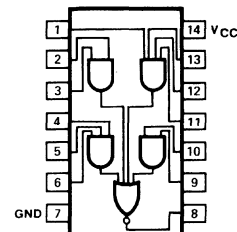


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)			50	
	I_{IL} (mA)			-2.0	
Outputs	I_{OH} (μA)			250	
	I_{OL} (mA)			20	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$							11		mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$							16		mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
						$C_L = 15pF$ $R_L = 280\Omega$				
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1					7.5			ns
t_{PHL}	Propagation delay	Waveform 1					8.5			ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54/7470

DESCRIPTION

The 54/7470 is a positive edge-triggered J-K Flip-Flop featuring direct Set and Reset inputs and complementary outputs Q and \bar{Q} . Information is transferred to the outputs on the LOW-to-HIGH transition of the Clock Pulse. Multiple J and K inputs are provided

to minimize gate requirements in "state decoding" applications.

The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When the Clock is LOW, they override the data inputs forcing the outputs to their steady state level as shown in the Truth Table.

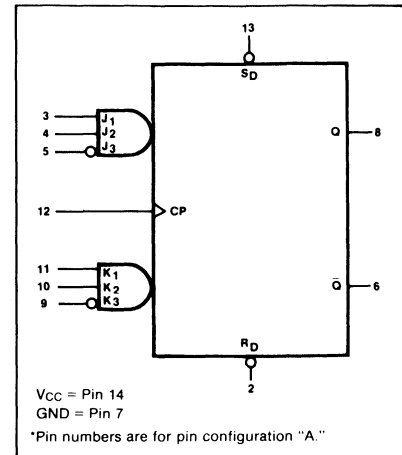
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig A	N7470N	
Ceramic DIP	Fig A	N7470F	S5470F
Flatpak	Fig B		S5470W

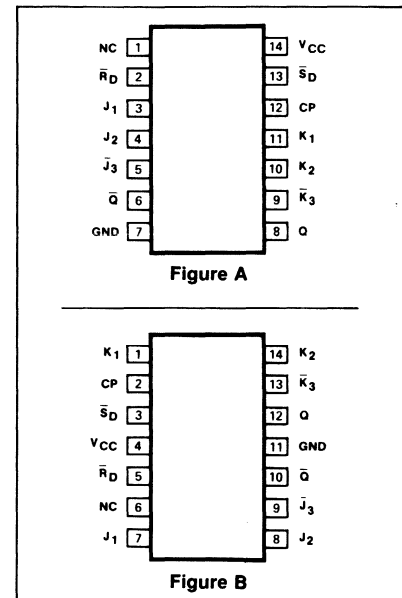
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
CP	Clock input	I_{IH} (μA)	40			
		I_{IL} (mA)	-1.6			
\bar{R}_D	Reset input	I_{IH} (μA)	80			
		I_{IL} (mA)	-3.2			
\bar{S}_D	Set input	I_{IH} (μA)	80			
		I_{IL} (mA)	-3.2			
JK	(Active HIGH) inputs	I_{IH} (μA)	40			
		I_{IL} (mA)	-1.6			
$\bar{J}\bar{K}$	(Active LOW) inputs	I_{IH} (μA)	40			
		I_{IL} (mA)	-1.6			
Q & \bar{Q} Outputs		I_{OH} (μA)	-400			
		I_{OL} (mA)	16			

LOGIC SYMBOL



PIN CONFIGURATION



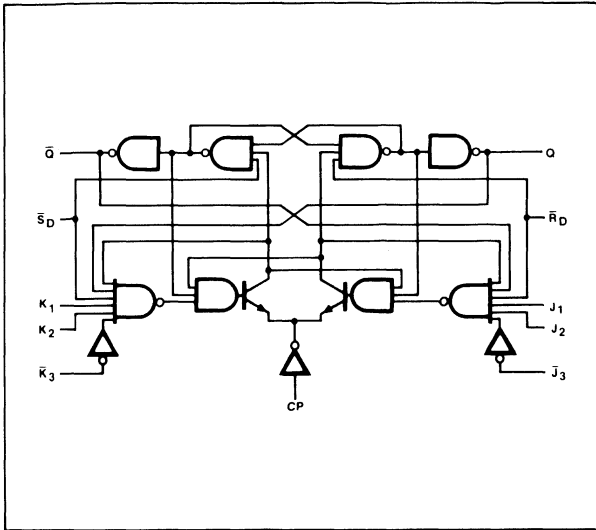
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current	$V_{CC} = \text{Max}, V_{CP} \geq 4.5V$			26					mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS		
	\bar{S}_D	\bar{R}_D	CP	J	K	Q	\bar{Q}
Asynchronous Set	L	H	L	X	X	H	L
Asynchronous Reset (Clear)	H	L	L	X	X	L	H
Undetermined ^(c)	L	L	X	X	X	L	L
Toggle	H	H	↑	h	h	\bar{q}	q
Load "0" (Reset)	H	H	↑	l	h	L	H
Load "1" (Set)	H	H	↑	h	l	H	L
Hold "no change"	H	H	↑	l	l	q	\bar{q}

J = $J_1 \cdot J_2 \cdot J_3$
 K = $K_1 \cdot K_2 \cdot K_3$
 H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW to HIGH Clock transition.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 3		20						MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Output	Waveform 3			50					ns ns
t_{PLH} t_{PHL}	Propagation delay \bar{S}_D or \bar{R}_D to Output	Waveform 5			50					ns ns

AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)	Waveform 3		20						ns
$t_{w(L)}$	Clock pulse width (LOW)	Waveform 3		30						ns
$t_{w(L)}$	Set or Reset pulse width (LOW)	Waveform 5		25						ns
t_s	Setup time J or K to Clock	Waveform 3		20						ns
t_h	Hold time J or K to Clock	Waveform 3		5						ns

NOTE

c. Both outputs will be LOW while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

54H/74H71

DESCRIPTION

The "71" is a positive pulse triggered master slave flip-flop with AND-OR gated JK inputs and direct Set (\bar{S}_D) input. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs should be stable while the Clock is HIGH for conventional operation. J

or K input transitions from HIGH-to-LOW should be avoided while the Clock is HIGH due to "One's catching" feature of this flip-flop.

The Set (\bar{S}_D) is an asynchronous active LOW input. When LOW, the \bar{S}_D overrides the Clock and data inputs forcing the Q output HIGH and the \bar{Q} output LOW.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$
Plastic DIP	Fig A	N74H71N	
Ceramic DIP	Fig A	N74H71F	S54H71F
Flatpak	Fig B		S54H71W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	54/74	54H/74H	54S/74S	54LS/74LS
$\bar{C}P$ Clock input I_{IH} (μA) I_{IL} (mA)		100 -4.0		
\bar{S}_D Set input I_{IH} (μA) I_{IL} (mA)		150 -6.0		
JK Data inputs I_{IH} (μA) I_{IL} (mA)		50 -2.0		
Q & \bar{Q} Outputs I_{OH} (μA) I_{OL} (mA)		-500 20		

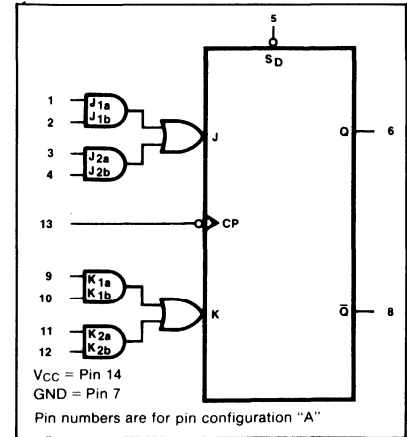
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}, V_{CP} = 0V$				30					mA

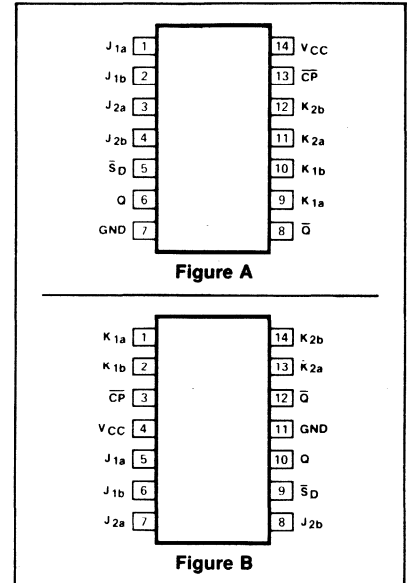
NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

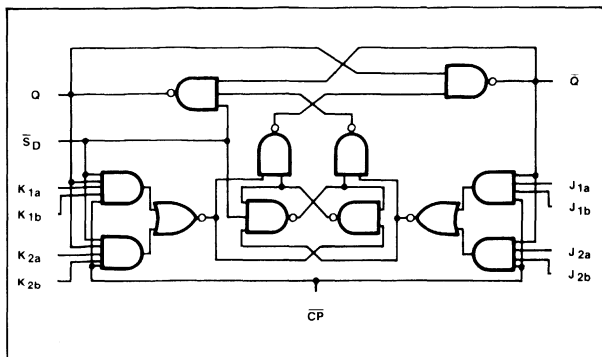
LOGIC SYMBOL



PIN CONFIGURATIONS



LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	$\bar{C}P$	J	K	Q	\bar{Q}
Asynchronous Set	L	X	X	X	H	L
Toggle	H		h	h	\bar{q}	q
Load "1" (Set)	H		h	l	H	L
Hold "no change"	H		l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level prior to LOW-to-HIGH Clock transition. (c)
 l = LOW voltage level prior to LOW-to-HIGH Clock transition. (c)
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition.
 = Positive Clock pulse.

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				$C_L = 25pF$ $R_L = 280\Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum Clock frequency	Waveform 4			25						MHz
t_{PLH} t_{PHL} Propagation delay Clock to Output	Waveform 4				21 27					ns ns
t_{PLH} t_{PHL} Propagation delay Set to Output	Waveform 5				13 24					ns ns

AC SETUP REQUIREMENTS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$ Clock pulse width (HIGH)	Waveform 4			12						ns
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 4			28						ns
$t_{w(L)}$ Set pulse width (LOW)	Waveform 5			16						ns
t_s Setup time J or K to Clock	Waveform 4			(c)						ns
t_h Hold time J or K to Clock	Waveform 4			0						ns

NOTE

c. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

**54/7472
54H/74H72**

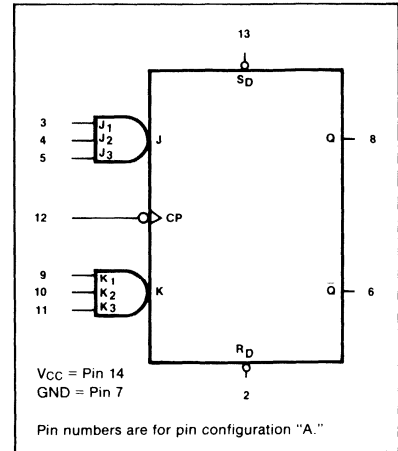
DESCRIPTION

The "72" is a positive pulse triggered master slave Flip-Flop with gated JK inputs and direct Set and Reset inputs. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs should be stable while the Clock is HIGH for conventional operation. J or K

input transitions from HIGH-to-LOW should be avoided while the Clock is HIGH due to "One's catching" feature of this flip-flop.

The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and data inputs forcing the outputs to their steady state level as shown in the Truth Table.

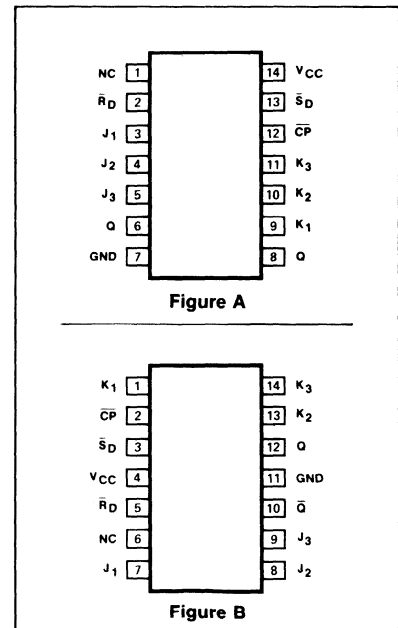
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$	
Plastic DIP	Fig A	N7472N	•	N74H72N	
Ceramic DIP	Fig A	N7472F	•	N74H72F	S5472F • S54H72F
Flatpak	Fig B				S5472W • S54H72W

PIN CONFIGURATIONS



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
$\bar{C}P$ Clock input	I_{IH} (μA)	80	50		
	I_{IL} (mA)	-3.2	-2.0		
\bar{R}_D Reset input	I_{IH} (μA)	80	100		
	I_{IL} (mA)	-3.2	-4.0		
\bar{S}_D Set input	I_{IH} (μA)	80	100		
	I_{IL} (mA)	-3.2	-4.0		
JK Data inputs	I_{IH} (μA)	40	50		
	I_{IL} (mA)	-1.6	-2.0		
Q & \bar{Q} Outputs	I_{OH} (μA)	-400	-500		
	I_{OL} (mA)	16	20		

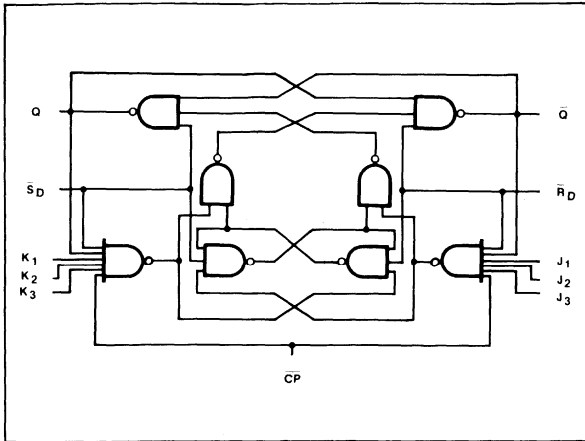
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_{CP} = 0V$		20		25					mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	$\bar{C}P$	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note c)	L	L	X	X	X	H	H
Toggle	H	H	\downarrow	h	h	\bar{q}	q
Load "0" (Reset)	H	H	\downarrow	l	h	L	H
Load "1" (Set)	H	H	\downarrow	h	l	H	L
Hold "no change"	H	H	\downarrow	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level prior to LOW-to-HIGH Clock transition. ^(d)
 l = LOW voltage level prior to LOW-to-HIGH Clock transition. ^(d)
 X = Don't care.
 q = Lower case letters indicate the state of the reference output prior to HIGH to LOW Clock transition.
 \downarrow = Positive Clock pulse.

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$		$C_L = 25pF$ $R_L = 280\Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 4		15		25				MHz
t_{PLH}	Propagation delay	Waveform 4			25		21			ns
t_{PHL}	Clock to Output	Waveform 4			40		27			ns
t_{PLH}	Propagation delay	Waveform 5			25		13			ns
t_{PHL}	\bar{S}_D or \bar{R}_D to Output	Waveform 5			40		24			ns

AC SETUP REQUIREMENTS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)	Waveform 4		20		12				ns
$t_{w(L)}$	Clock pulse width (LOW)	Waveform 4		47		28				ns
$t_{w(L)}$	Set or Reset pulse width (LOW)	Waveform 5		25		16				ns
t_s	Setup time J or K to Clock	Waveform 4		(d)		(d)				ns
t_h	Hold time J or K to Clock	Waveform 4		0		0				ns

NOTES

- c. Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.
- d. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

**54/7473
54H/74H73
54LS/74LS73**

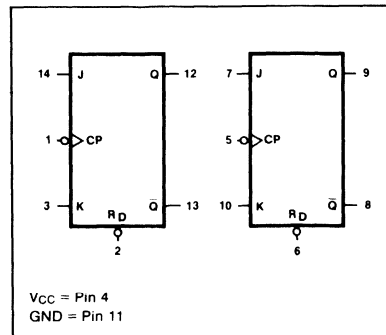
DESCRIPTION

The "73" is a dual Flip-Flop with individual JK, Clock and direct Reset inputs. The 7473 and 74H73 are positive pulse triggered flip-flops. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. For these devices the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS73 is a negative edge triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset (\bar{R}_D) is an asynchronous active LOW input. When LOW, it overrides the Clock and data inputs forcing the Q output LOW and the \bar{Q} output HIGH.

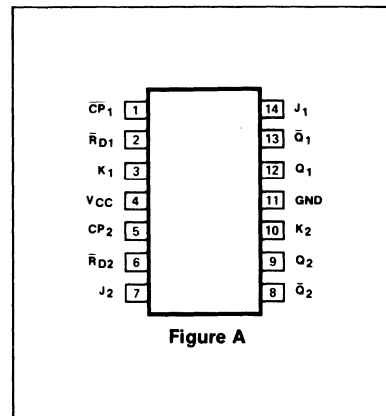
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$	
Plastic DIP	Fig A Fig A	N7473N	• N74H73N	N74LS73N	
Ceramic DIP	Fig A Fig A	N7473F	• N74H73F	S5473F	• S54H73F S54LS73F
Flatpak	Fig A Fig A			S5473W	• S54H73W S54LS73W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP} Clock input	I_{IH} (μA)	80	50		80
	I_{IL} (mA)	-3.2	-2.0		-0.72
\bar{R}_D Reset input	I_{IH} (μA)	80	100		60
	I_{IL} (mA)	-3.2	-4.0		-0.8
JK Data inputs	I_{IH} (μA)	40	50		20
	I_{IL} (mA)	-1.6	-2.0		-0.36
Q & \bar{Q} Outputs	I_{OH} (μA)	-400	-500		-400
	I_{OL} (mA)	16	20		4/8 (a)

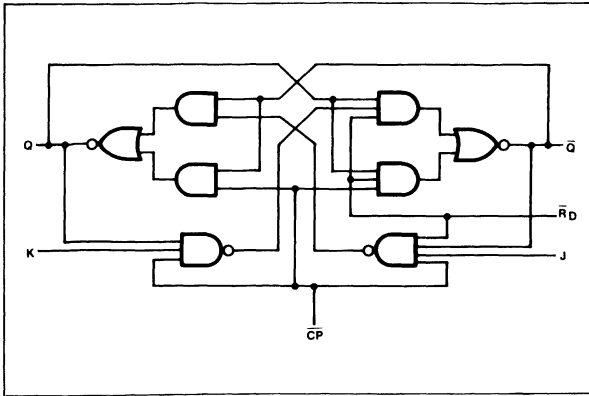
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply Current	$V_{CC} = \text{Max}$, $V_{CP} = 0V$		40		50				8.0	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	R _D	CP (d)	J	K	Q	Q̄
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	⌋	h	h	q̄	q
Load "0" (Reset)	H	⌋	l	h	L	H
Load "1" (Set)	H	⌋	h	l	H	L
Hold "no change"	H	⌋	l	l	q	q̄

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(c)
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(c)
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition.
 ⌋ = Positive Clock pulse.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		C _L = 15pF R _L = 400Ω		C _L = 25pF R _L = 280Ω				C _L = 15pF R _L = 2kΩ			
		Min	Max	Min	Max	Min	Max	Min	Max		
f _{MAX}	Maximum Clock frequency	Waveform 4		15		25				30	MHz
t _{PLH}	Propagation delay	Waveform 4			25		21			20	ns
t _{PHL}	Clock to output	Waveform 4			40		27			30	ns
t _{PLH}	Propagation delay	Waveform 5			25		13			20	ns
t _{PHL}	Reset to output	Waveform 5			40		24			30	ns

AC SET-UP REQUIREMENTS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
t _{w(H)}	Clock pulse width (HIGH)	Waveform 4		20		12				20	ns
t _{w(L)}	Clock pulse width (LOW)	Waveform 4		47		28				13	ns
t _{w(L)}	Reset pulse width (LOW)	Waveform 5		25		16				25	ns
t _s	Setup time J or K to Clock	Waveform 4		(c)		(c)				20	ns
t _h	Hold time J or K to Clock	Waveform 4		0		0				0	ns

NOTES

- c. The J and K inputs of the 7473 and 74H73 must be stable while the Clock is HIGH for conventional operation.
- d. The 74LS73 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.

54/7474
54H/74H74
54S/74S74
54LS/74LS74

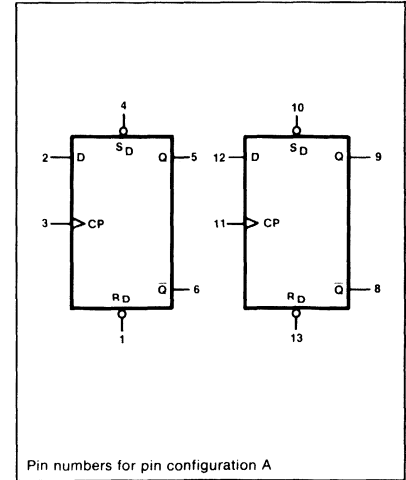
DESCRIPTION

The "74" is a Dual Positive Edge-Triggered D-Type Flip-Flop featuring individual data, clock, set and reset inputs; also complementary Q and \bar{Q} outputs.

Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs and operate independently of the clock input. Information on the data (D) input is transferred to the Q output

on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation. Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N7474N	• N74H74N		
	Fig. A	N74S74N	• N74LS74N		
Ceramic DIP	Fig. A	N7474F	• N74H74F	S5474F	• S54H74F
	Fig. A	N74S74F	• N74LS74F	S54S74F	• S54LS74F
Flatpak	Fig. B			S5474W	• S54H74W
	Fig. A			S54S74W	• S54LS74W

PIN CONFIGURATION

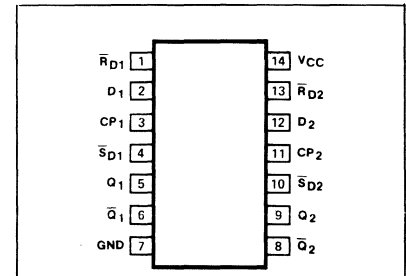


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
D Data Input	I_{IH} (μA)	40	50	50	20
	I_{IL} (mA)	-1.6	-2.0	-2.0	-0.36
CP Clock Input	I_{IH} (μA)	80	100	100	40
	I_{IL} (mA)	-3.2	-4.0	-4.0	-0.8
\bar{S}_D Set Input	I_{IH} (μA)	80	100	100	40
	I_{IL} (mA)	-1.6	-2.0	-4.0	-0.8
\bar{R}_D Reset Input	I_{IH} (μA)	120	150	150	60
	I_{IL} (mA)	-3.2	-4.0	-6.0	-1.15
Q & \bar{Q} Output	I_{OH} (μA)	-400	-500	-1000	-400
	I_{OL} (mA)	16	20	20	4/8 (a)

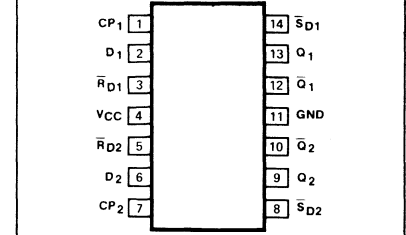


Figure B

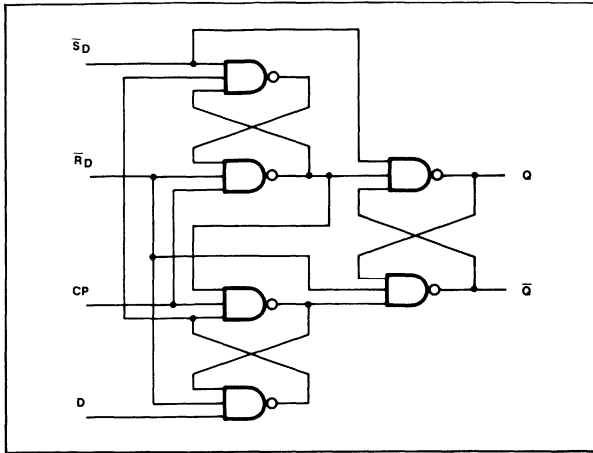
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$		30		42		50		8.0	mA
	$V_{CP} = 0V$		30		50		50		8.0	

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	S _D [̄]	R _D [̄]	CP	D	Q	Q [̄]
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined (c)	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW to HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW to HIGH clock transition.
 X = Don't care.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT		
		C _L = 15 pF R _L = 400 Ω		C _L = 25 pF R _L = 280 Ω		C _L = 15 pF R _L = 280 Ω		C _L = 15 pF R _L = 2k Ω				
		Min	Max	Min	Max	Min	Max	Min	Max			
f _{Max}	Maximum clock frequency	Waveform 3		15		35		75		25		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to output	Waveform 3			25		15		9.0		25	ns
		Waveform 3			40		20		9.0		40	ns
t _{PLH} t _{PHL}	Propagation delay Set or reset to output	Waveform 5			25		20		6.0		25	ns
		Waveform 5 CP = HIGH			40		30		13.5		40	ns
t _{PHL}	Set or reset to output	Waveform 5 CP = LOW			40		30		8.0		40	ns

AC SET UP REQUIREMENTS: T_A = 25°C (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
t _{w(H)}	Clock pulse width (HIGH)	Waveform 3		30		15		6.0		25	ns
t _{w(L)}	Clock pulse width (LOW)	Waveform 3		37		13.5		7.3		15	ns
t _{w(L)}	Set or reset pulse width (LOW)	Waveform 5		30		25		7.0		25	ns
t _{s(H)}	Setup time (HIGH) data to clock	Waveform 3		20		10		3.0		25	ns
t _{s(L)}	Setup time (LOW) data to clock	Waveform 3		20		15		3.0		20	ns
t _h	Hold time data to clock	Waveform 3		5.0		5.0		2.0		5.0	ns

NOTE

c Both outputs will be High while both S_D[̄] and R_D[̄] are LOW, but the output states are unpredictable if S_D[̄] and R_D[̄] go HIGH simultaneously.

54/7475
54LS/74LS75

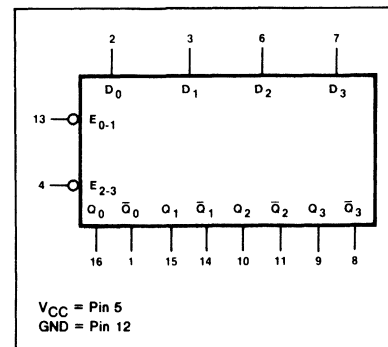
DESCRIPTION

The "75" is a Dual 2-Bit D-Latch with complementary Q and \bar{Q} outputs. Two Enable inputs are provided; each controls two latches. When the Enable (E) is HIGH, information present at a Data (D) input is transferred to the Q and \bar{Q} (inverted) outputs, and the outputs will follow the data input as long as the Enable remains HIGH. The information that is present at the data input one setup time prior to the HIGH-to-LOW Enable transition is stored in the latch until the Enable returns to a HIGH level.

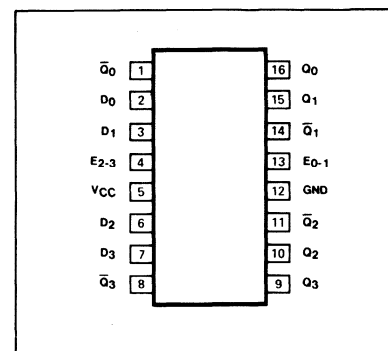
FEATURES

- 4-Bit transparent latch
- Refer to 54LS/74LS375 for V_{CC} and GND on corner pins.

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C		MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C	
Plastic DIP	N7475N	•	N74LS75N	
Ceramic DIP	N7475F	•	N74LS75N	S5475F • S54LS75F
Flatpak				S5475W • S54LS75W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D ₀ -D ₃	Data inputs	I _{IH} (μA) I _{IL} (mA)	80 -3.2		20 -0.4
E ₀₋₁	Enable (active LOW) input, Latches 0, 1	I _{IH} (μA) I _{IL} (mA)	160 -6.4		80 -1.6
E ₂₋₃	Enable (active LOW) input, Latches 2, 3	I _{IH} (μA) I _{IL} (mA)	160 -6.4		80 -1.6
Q ₀ -Q ₃	Latch outputs	I _{OH} (μA) I _{OL} (mA)	-400 16		-400 4/8(a)
\bar{Q}_0 - \bar{Q}_3	Complimentary Latch outputs	I _{OH} (μA) I _{OL} (mA)	-400 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

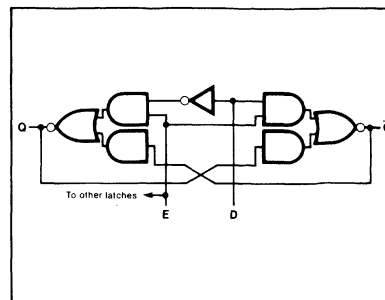
The "75" has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the data inputs as long as E is HIGH. The data on the D inputs one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

**MODE SELECT—
FUNCTION TABLE**

OPERATING MODE	INPUTS		OUTPUTS	
	E	D	Q	\bar{Q}
Data Enabled	H	L	L	H
	H	H	H	L
Data Latched	L	X	q	\bar{q}

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply Current	V _{CC} = Max	Mil	46				12	mA
		Com	53				12	

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay	Figure 1		30				27	ns
t _{PHL} Data to Q output			25				17	
t _{PLH} Propagation delay	Figure 2		40				20	ns
t _{PHL} Data to \bar{Q} output			15				15	
t _{PLH} Propagation delay	Figure 3		30				27	ns
t _{PHL} Enable to Q output			15				25	
t _{PLH} Propagation delay	Figure 3		30				30	ns
t _{PHL} Enable to \bar{Q} output			15				15	

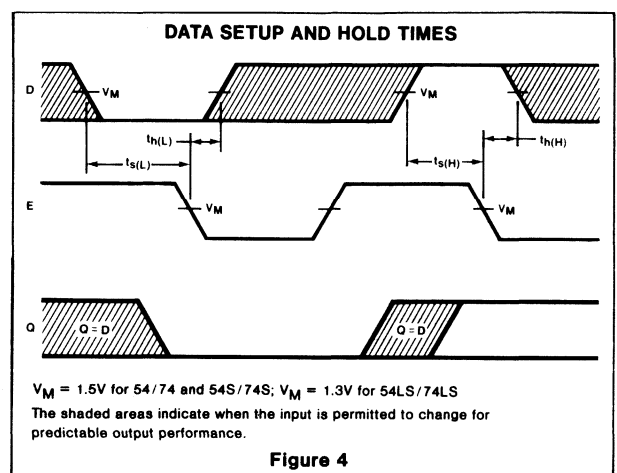
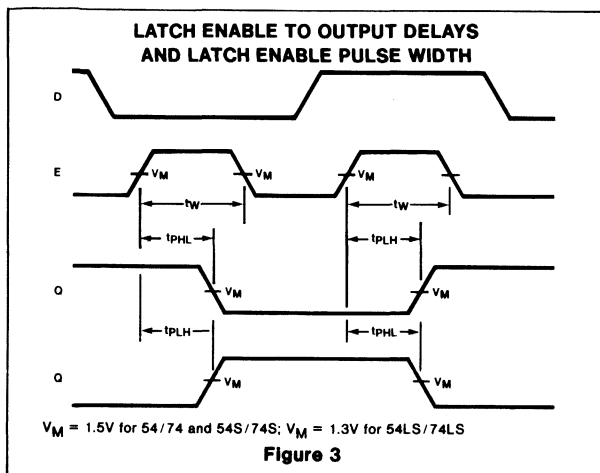
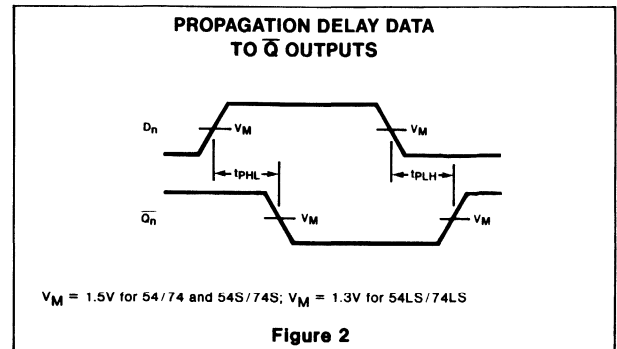
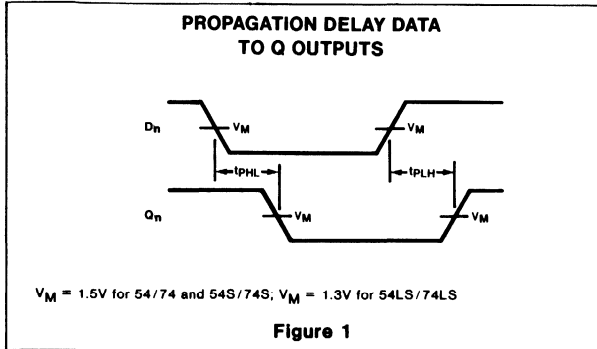
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Enable pulse width	Figure 3	20				20		ns
t _s Setup time Data to Enable	Figure 4	20				20		ns
t _h Hold time Data to Enable	Figure 4	5.0				0		ns

AC WAVEFORMS



**54/7476
54H/74H76
54LS/74LS76**

DESCRIPTION

The "76" is a Dual JK Flip-Flop with individual J, K, Clock, Set and Reset inputs. The 7476 and 74H76 are positive pulse triggered flip-flops. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

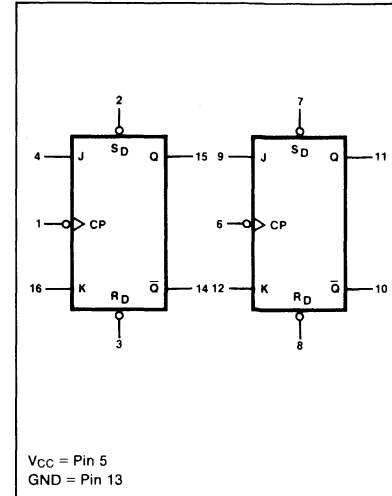
The 74LS76 is a negative edge triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW Clock transition.

The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and data inputs forcing the outputs to the steady state levels as shown in the Truth Table.

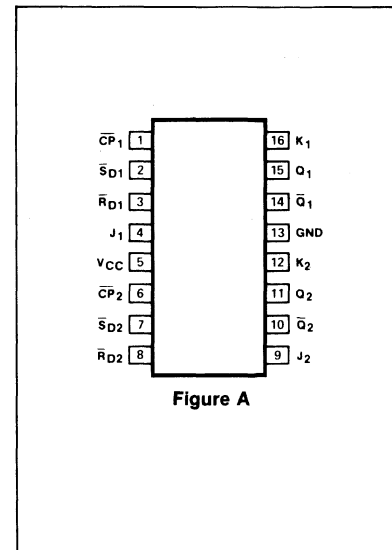
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig A Fig A	N7476N • N74H76N N74LS76N	
Ceramic DIP	Fig A Fig A	N7476F • N74H76F N74LS76F	S5476F • S54H76F S54LS76F
Flatpak	Fig A Fig A		S5476W • S54H76W S54LS76W

LOGIC SYMBOL



PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP} Clock input	I_{IH} (μA)		80	50		80
	I_{IL} (mA)		-3.2	-2.0		-0.8
\bar{R}_D Reset input	I_{IH} (μA)		80	100		60
	I_{IL} (mA)		-3.2	-4.0		-0.8
\bar{S}_D Set input	I_{IH} (μA)		80	100		60
	I_{IL} (mA)		-3.2	-4.0		-0.8
JK Data inputs	I_{IH} (μA)		40	50		20
	I_{IL} (mA)		-1.6	-2.0		-0.4
Q & \bar{Q} Outputs	I_{OH} (μA)		-400	-500		-400
	I_{OL} (mA)		16	20		4/8 ^(a)

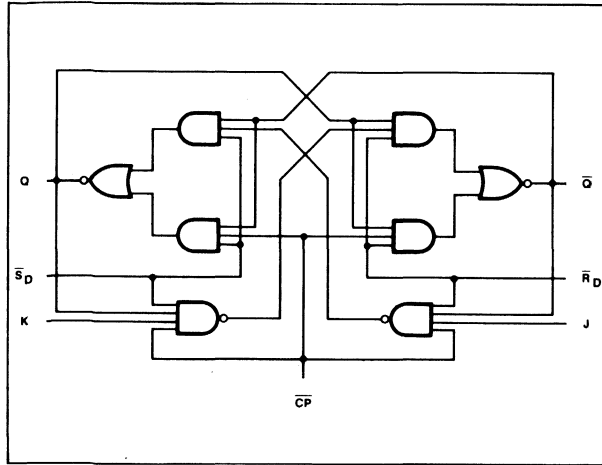
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_{CP} = 0V$		40		50				8.0	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	S _D	R _D	CP (d)	J	K	Q	Q̄
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H		h	h	q̄	q
Load "0" (Reset)	H	H		l	h	L	H
Load "1" (Set)	H	H		h	l	H	L
Hold "no change"	H	H		l	l	q	q̄

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition. ^(e)
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition. ^(e)
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition.
 = Positive Clock pulse.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		C _L = 15 pF R _L = 400 Ω		C _L = 25 pF R _L = 280 Ω				C _L = 15 pF R _L = 2k Ω		
		Min	Max	Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock frequency	Waveform 4	15		25				30	MHz
t _{PLH}	Propagation delay	Waveform 4		25		21			20	ns
t _{PHL}	Clock to Output			40		27			30	
t _{PLH}	Propagation delay	Waveform 5		25		13			20	ns
t _{PHL}	S _D or R _D to Output			40		24			30	

AC SETUP REQUIREMENTS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{w(H)}	Clock pulse width (HIGH)	Waveform 4	20		12				20	ns
t _{w(L)}	Clock pulse width (LOW)	Waveform 4	47		28				13	ns
t _{w(L)}	Set or Reset pulse width (LOW)	Waveform 5	25		16				25	ns
t _s	Setup time J or K to Clock	Waveform 4	(e)		(e)				20	ns
t _h	Hold time J or K to Clock	Waveform 4	0		0				0	ns

NOTES

- c. Both outputs will be HIGH while both S_D and R_D are LOW, but the output states are unpredictable if S_D and R_D go HIGH simultaneously.
- d. The 74LS76 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.
- e. The J and K inputs of the 7476 and 74H76 must be stable while the Clock is HIGH for conventional operation.

**5477
54LS77**

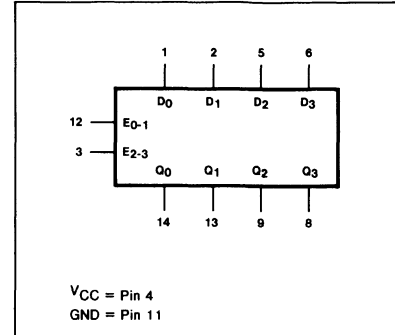
DESCRIPTION

The "77" is a Dual 2-Bit D-Latch offered in a 14-Pin flat pack. Two Enable inputs are provided; each controls two latches. When the Enable (E) is HIGH, information present at a Data (D) input is transferred to the Q outputs, and the outputs will follow the data input as long as the Enable remains HIGH. The information that is present at the data input one setup time prior to the HIGH-to-LOW Enable transition is stored in the latch until the Enable returns to a HIGH level.

FEATURES

- Available in 14-Pin flat pack only
- 4-Bit transparent latch
- Refer to the "75" or "375" for Q & \bar{Q} output version
- Refer to "375" for V_{CC} and GND on corner pins.

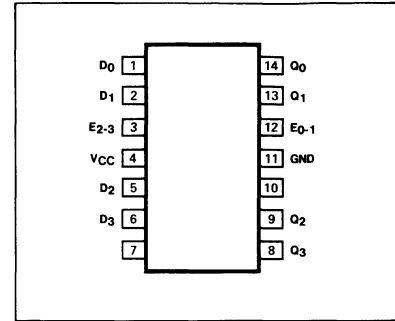
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP		
Ceramic DIP		
Flatpak		S5477W • S54LS77W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D ₀ -D ₃	Data inputs	I _H (μA)	80		20
		I _L (mA)	-3.2		-0.4
E ₀₋₁	Enable (active LOW) input, Latches 0, 1	I _H (μA)	160		80
		I _L (mA)	-6.4		-1.6
E ₂₋₃	Enable (active LOW) input, Latches 2,3	I _H (μA)	160		80
		I _L (mA)	-6.4		-1.6
Q ₀ -Q ₃	Latch outputs	I _{OH} (μA)	-400		-400
		I _{OL} (mA)	16		4.0

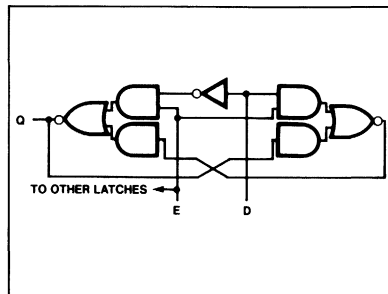
NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "77" has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the data inputs as long as E is HIGH. The data on the D inputs one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

LOGIC DIAGRAM (EACH LATCH)



**MODE SELECT—
FUNCTION TABLE**

OPERATING MODE	INPUTS		OUTPUTS
	E	D	Q
Data Enabled	H	L	L
	H	H	H
Data Latched	L	X	q

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		46				13	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay	Figure 1		30				27	ns
t _{PHL} Data to Q output			25				17	ns
t _{PLH} Propagation delay	Figure 2		30				27	ns
t _{PHL} Enable to Q output			15				25	ns

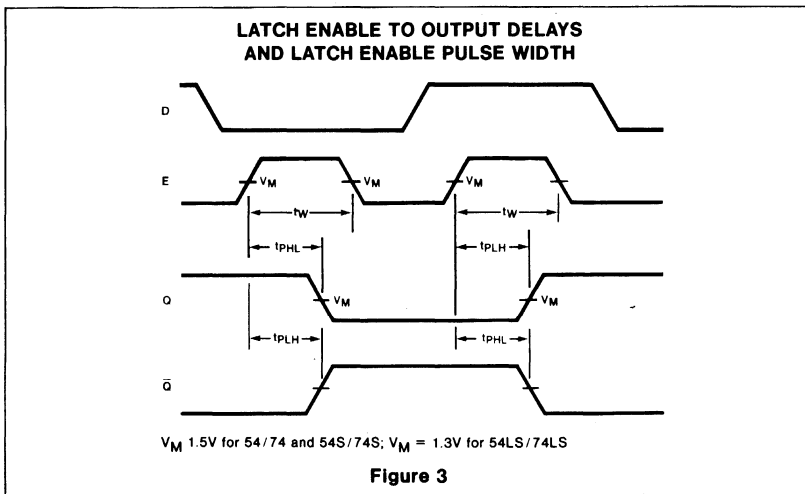
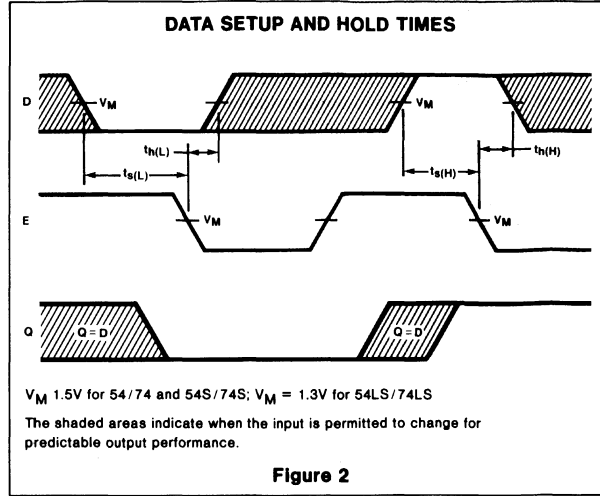
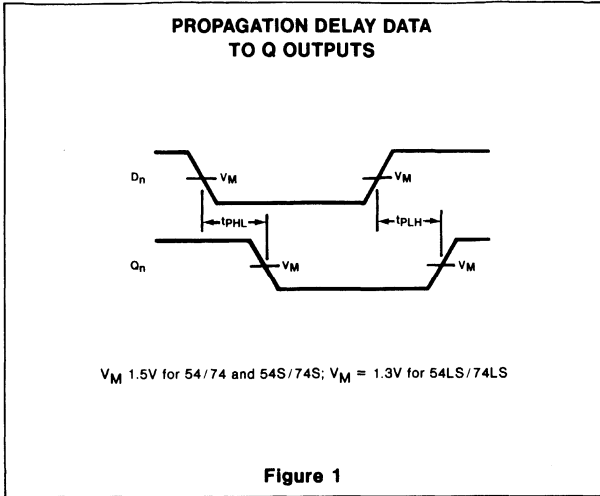
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Enable pulse width	Figure 2	20				20		ns
t _s Setup time Data to Enable	Figure 3	20				20		ns
t _h Hold time Data to Enable	Figure 3	5.0				0		ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54/7480

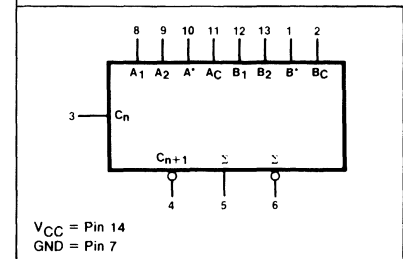
DESCRIPTION

The "80" is a Gated Full Adder useful for parallel or serial addition and for addition of more than two variables. It features gated complementary inputs, complementary sum outputs, and an active LOW carry output.

FEATURES

- Full binary single bit addition
- Gated input for addition of multiple variables
- Fast serial-carry output

LOGIC SYMBOL



PIN CONFIGURATION

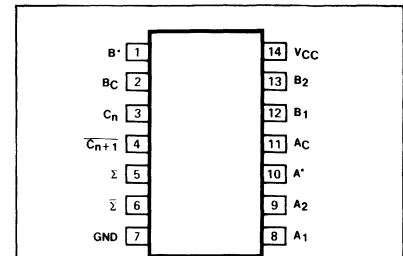


Figure A

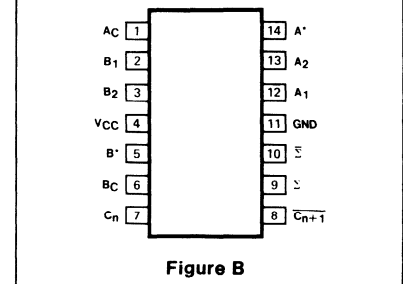


Figure B

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N7480N	
Ceramic DIP	Fig. A	N7480F	S5480F
Flatpak	Fig. B		S5480W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_1, A_2, B_1, B_2	Non-inverting data inputs	I_{IH} (μA) I_{IL} (mA)	15 -1.6		
A', B'	Inverting data inputs	I_{IH} (μA) I_{IL} (mA)	N.A. -2.6		
A_C, B_C	Control inputs	I_{IH} (μA) I_{IL} (mA)	15 -1.6		
C_n	Carry input	I_{IH} (μA) I_{IL} (mA)	200 -8.0		
A', B'	Inverting data outputs	I_{OH} (μA) I_{OL} (mA)	-120 4.8		
Σ & $\bar{\Sigma}$	Sum outputs	I_{OH} (μA) I_{OL} (mA)	-400 16		
\bar{C}_{n+1}	Carry (active LOW) output	I_{OH} (μA) I_{OL} (mA)	-200 8.0		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "80" is a single-bit, high speed, Binary Full Adder with gated complementary inputs, complementary sum (Σ and $\bar{\Sigma}$) outputs and inverted carry output. It is designed for medium and high speed, multiple-bit, parallel-add/serial-carry applications. The circuit utilizes DTL for the gated inputs and high speed, high fan out TTL for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

TRUTH TABLE

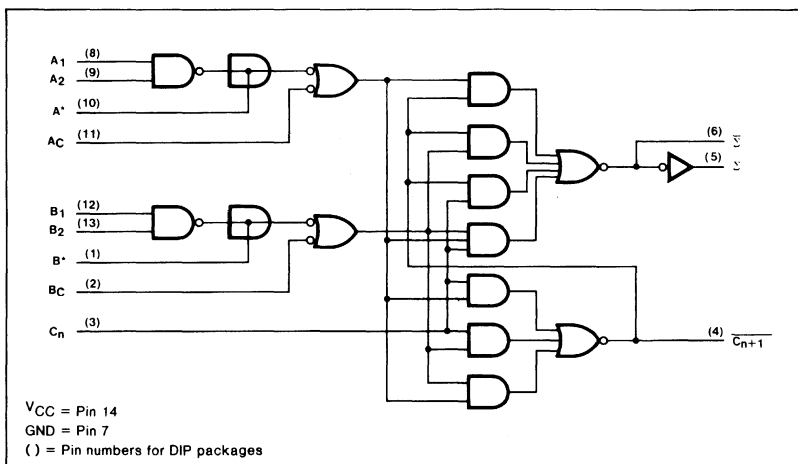
INPUTS			OUTPUTS		
C_n	B	A	\bar{C}_{n+1}	$\bar{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	L	L
H	L	L	H	H	H
H	L	H	L	L	L
H	H	L	L	H	L
H	H	H	L	L	H

H = HIGH voltage level
L = LOW voltage level

NOTES

- b. $A = A^* \cdot A_C$, $B = B^* \cdot B_C$ where $A^* = A_1 \cdot A_2$, $B^* = B_1 \cdot B_2$
- c. When A^* or B^* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
- d. When A_1 and A_2 or B_1 and B_2 are used as inputs, A^* or B^* respectively must be open or used to perform Dot-OR logic.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$, Σ & $\bar{\Sigma}$ outputs	Mil	-20	-57				mA
		Com	-18	-57				mA
	$V_{CC} = \text{Max}$, \bar{C}_{n+1} output	Mil	-20	-70				mA
		Com	-18	-70				mA
		$V_{CC} = \text{Max}$, A^* & B^* outputs		-0.9	-2.9			
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil		31				mA
		Com		35				mA

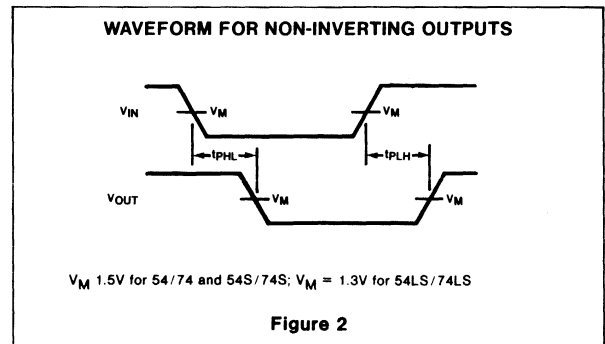
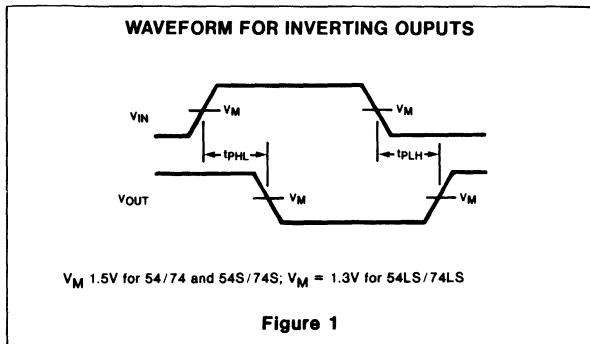
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for test circuits and conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propogation delay C _n to C _{n+1} output Figure 1 C _L = 15pF, R _L = 780Ω		17 12					ns ns
t _{PLH} t _{PHL}	Propogation delay A _C or B _C to C _{n+1} output Figure 2 C _L = 15pF, R _L = 780Ω		25 55					ns ns
t _{PLH} t _{PHL}	Propogation delay A _C or B _C to Σ output Figure 1 C _L = 15pF, R _L = 400Ω		70 80					ns ns
t _{PLH} t _{PHL}	Propogation delay A _C or B _C to Σ̄ output Figure 2 C _L = 15pF, R _L = 400Ω		55 75					ns ns
t _{PLH} t _{PHL}	Propogation delay A ₁ or A ₂ to A* output Figure 1 C _L = 15pF		65 25					ns ns
t _{PLH} t _{PHL}	Propogation delay B ₁ or B ₂ to B* output Figure 1 C _L = 15pF		65 25					ns ns

AC WAVEFORMS



54/7483
54LS/74LS83A

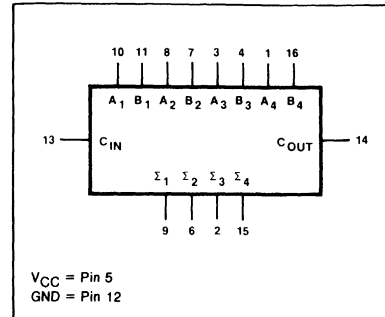
DESCRIPTION

The "83" is a high speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A₁-A₄, B₁-B₄) and a Carry input (C_{IN}). The sum of the two 4-bit words is combined with the carry input and presented at the four Sum outputs (Σ₁-Σ₄) and the Carry output (C_{OUT}). It operates with either HIGH or LOW operands (positive or negative logic).

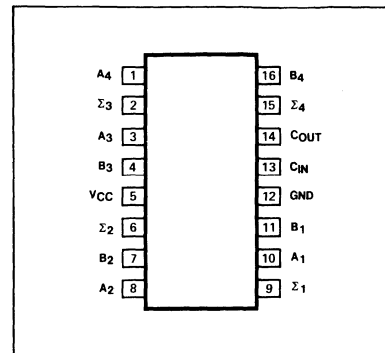
FEATURES

- High speed 4-bit binary addition
- Cascadeable in 4-bit increments
- LS83A has fast internal carry lookahead
- See "283" for corner power pin version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	V _{CC} =5V ± 5%; T _A =0°C to +70°C		V _{CC} =5V ± 10%; T _A =-55°C to +125°C	
Plastic DIP	N7483N	•	N74LS83AN	
Ceramic DIP	N7483F	•	N74LS83AF	S5483F • S54LS83AF
Flatpak				S5483W • S54LS83AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A ₁ , B ₁ , A ₃ , B ₃	Operand inputs	I _{IH} (μA)	80		40
		I _{IL} (mA)	-3.2		-0.8
A ₂ , B ₂ , A ₄ , B ₄	Operand inputs	I _{IH} (μA)	40		40
		I _{IL} (mA)	-1.6		-0.8
C _{IN}	Carry input	I _{IH} (μA)	80		20
		I _{IL} (mA)	-3.2		-0.4
Σ ₁ -Σ ₄	Sum outputs	I _{OH} (μA)	-800		-400
		I _{OL} (mA)	16		4/8(a)
C _{OUT}	Carry output	I _{OH} (μA)	-400		-400
		I _{OL} (mA)	8.0		4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "83" adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs (Σ_1 - Σ_4) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus

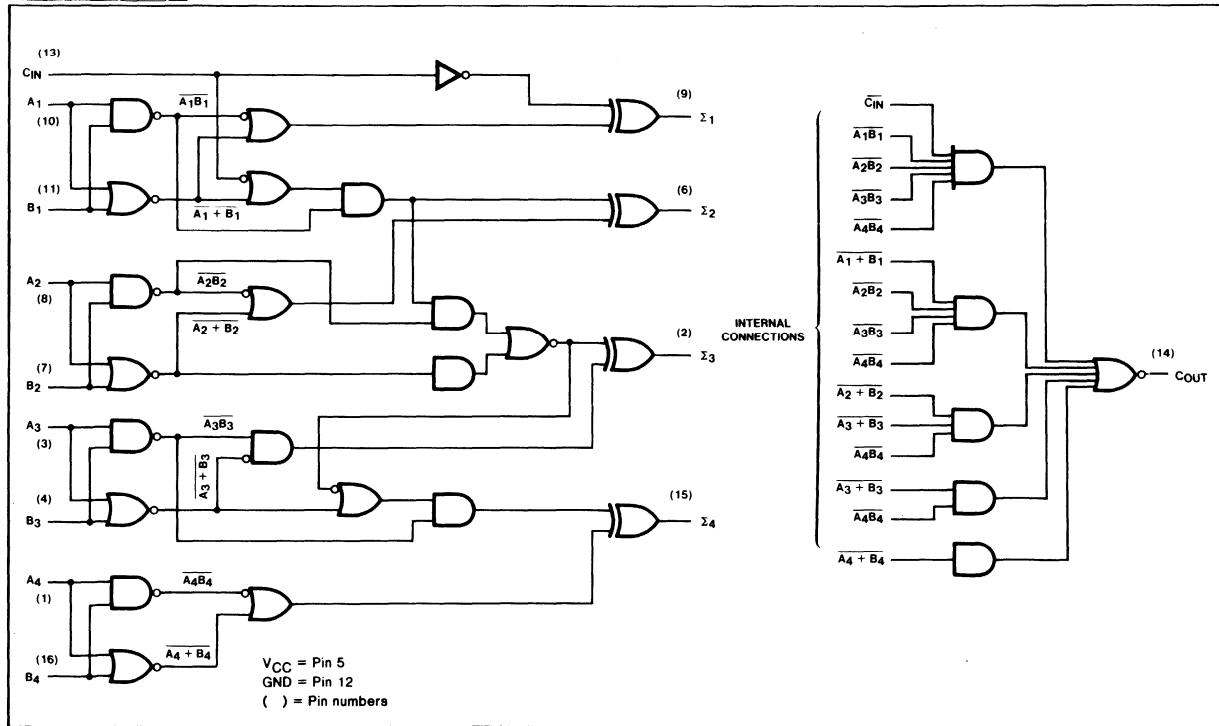
Due to the symmetry of the binary add function the "83" can be used with either all active HIGH operands (positive logic) or with all active LOW operands (negative logic)-see Table "A". With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN} , A_1 , B_1 , can arbitrarily be assigned to pins 10, 11, 13, etc.

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

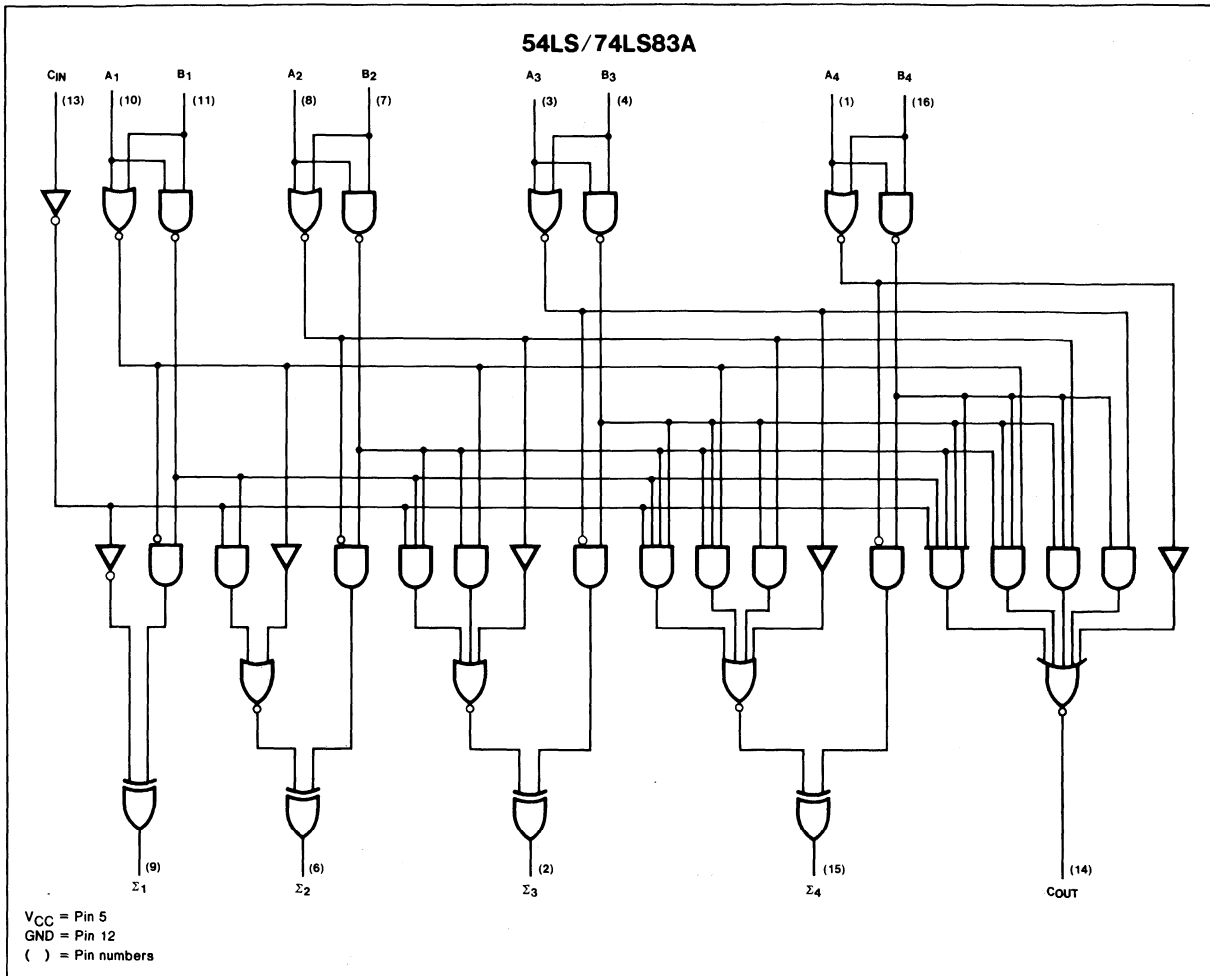
(10+9=19)
(carry+5+6=12)

Table "A"

LOGIC DIAGRAM



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max		
I _{OS} Short circuit current for C _{OUT} only	V _{CC} = Max	Mil	-20	-70			-15	-100	mA
		Com	-18	-70			-15	-100	mA
I _{CC} Supply Current	V _{CC} = Max	V _{IN} = 0V		79				39	mA
		V _{IN} = 4.5V		79				34	mA

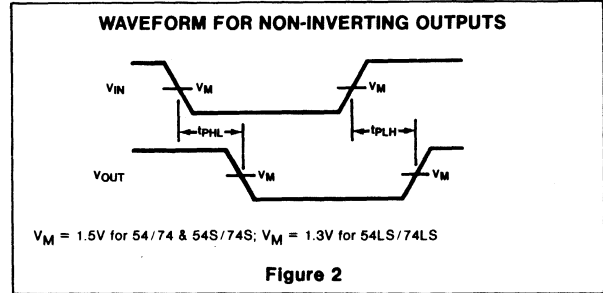
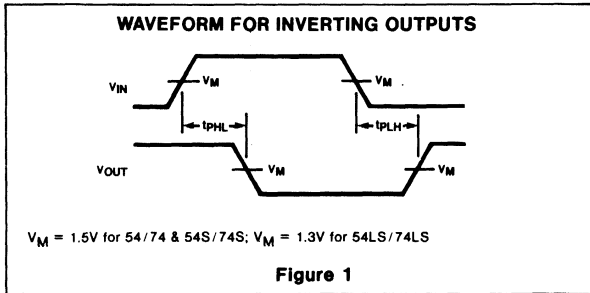
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 50\text{pF}$ $R_L = 400\Omega$				$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} C_{IN} to Σ_1	Figures 1 & 2		34				24	ns
t_{PLH} Propagation delay t_{PHL} C_{IN} to Σ_2	Figures 1 & 2		35				24	ns
t_{PLH} Propagation delay t_{PHL} C_{IN} to Σ_3	Figures 1 & 2		50				24	ns
t_{PLH} Propagation delay t_{PHL} C_{IN} to Σ_4	Figures 1 & 2		50				24	ns
t_{PLH} Propagation delay t_{PHL} A_i or B_i to Σ_i	Figures 1 & 2		40				24	ns
t_{PLH} Propagation delay t_{PHL} C_{IN} to C_{OUT}	Figure 2		20				17	ns
t_{PLH} Propagation delay t_{PHL} A_i or B_i to C_{OUT}	Figures 1 & 2		22				17	ns

AC WAVEFORMS



**54/7485
54S/74S85
54LS/74LS85**

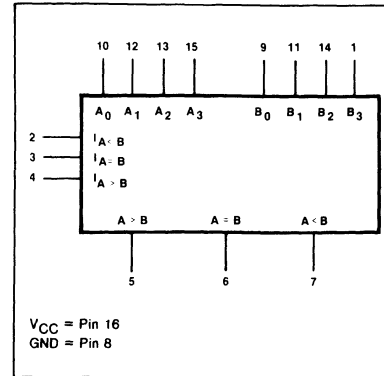
DESCRIPTION

The "85" is an expandable 4-Bit Magnitude Comparator. It compares two 4-bit binary weighted words (A_0 - A_3) and (B_0 - B_3), where A_3 and B_3 are the most significant bits. The expansion inputs $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ are treated as the least significant inputs for comparison purposes. The three active HIGH outputs are "A greater than B" ($A>B$), "A equals B" ($A=B$), and "A less than B" ($A<B$). These devices can be cascaded to almost any length.

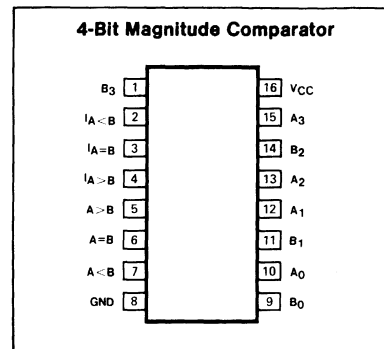
FEATURES

- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating
- Use 54S/74S85 for very high speed comparisons

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N7485N	• N74LS85N	
Ceramic DIP	N7485F	• N74LS85F	S5485F	• S54LS85F
Flatpak			S5485W	• S54LS85W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_0 - A_3	Operand A inputs	I_{IH} (μA)	120	150	60
		I_{IL} (mA)	-4.8	-6.0	-1.2
B_0 - B_3	Operand B inputs	I_{IH} (μA)	120	150	60
		I_{IL} (mA)	-4.8	-6.0	-1.2
$I_{A=B}$	Expander A = B input	I_{IH} (μA)	120	150	60
		I_{IL} (mA)	-4.8	-6.0	-1.2
$I_{A<B}$	Expander A less than B input	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
$I_{A>B}$	Expander A greater than B input	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
A = B	A equal to B output	I_{OH} (μA)	-400	-1000	-400
		I_{OL} (mA)	16	20	4/8 ^(a)
A < B	A less than B output	I_{OH} (μA)	-400	-1000	-400
		I_{OL} (mA)	16	20	4/8 ^(a)
A > B	A greater than B output	I_{OH} (μA)	-400	-1000	-400
		I_{OL} (mA)	16	20	4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "85" is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0 — A_3) and (B_0 — B_3), where A_3 and B_3 are the most significant bits.

The operation of the "85" is described in the Truth Table showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the $A>B$, $A=B$ and $A<B$ outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B} = \text{HIGH}$, $I_{A=B} = \text{LOW}$, and $I_{A<B} = \text{HIGH}$.

The parallel expansion scheme shown in Figure A demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ LOW. The "85" can be used as a 5-bit comparator only when the outputs are used to drive the (A_0 — A_3) and (B_0 — B_3) inputs of another "85" device. The parallel technique can be expanded to any number of bits as shown in Table I.

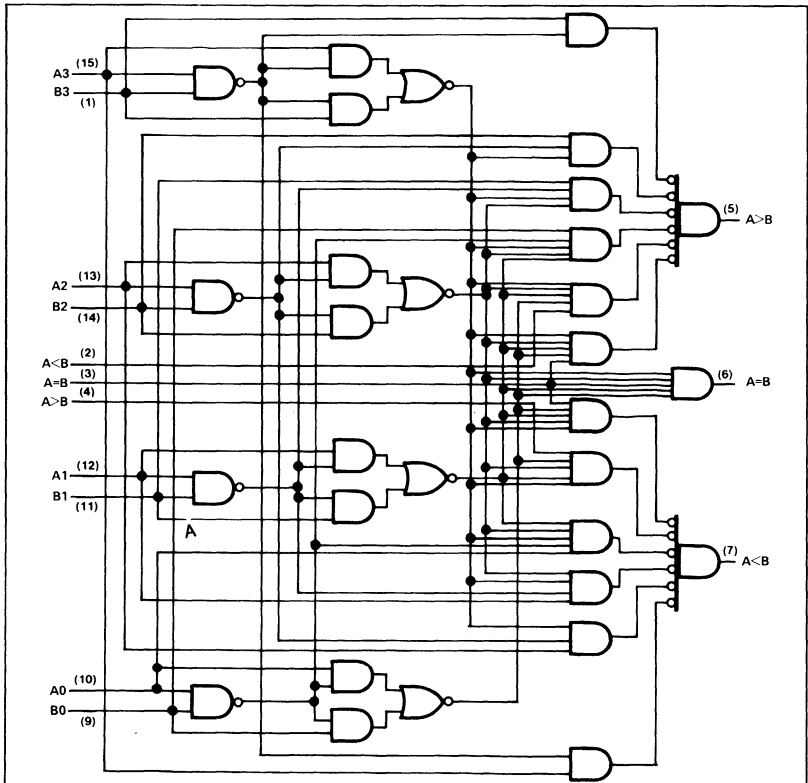
WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS		
		54/74	54S/74S	54LS/74LS
1 - 4 Bits	1	23ns	12ns	23ns
5 - 25 Bits	2 - 6	40ns	22ns	46ns
25 - 120 Bits	8 - 31	63ns	34ns	69ns

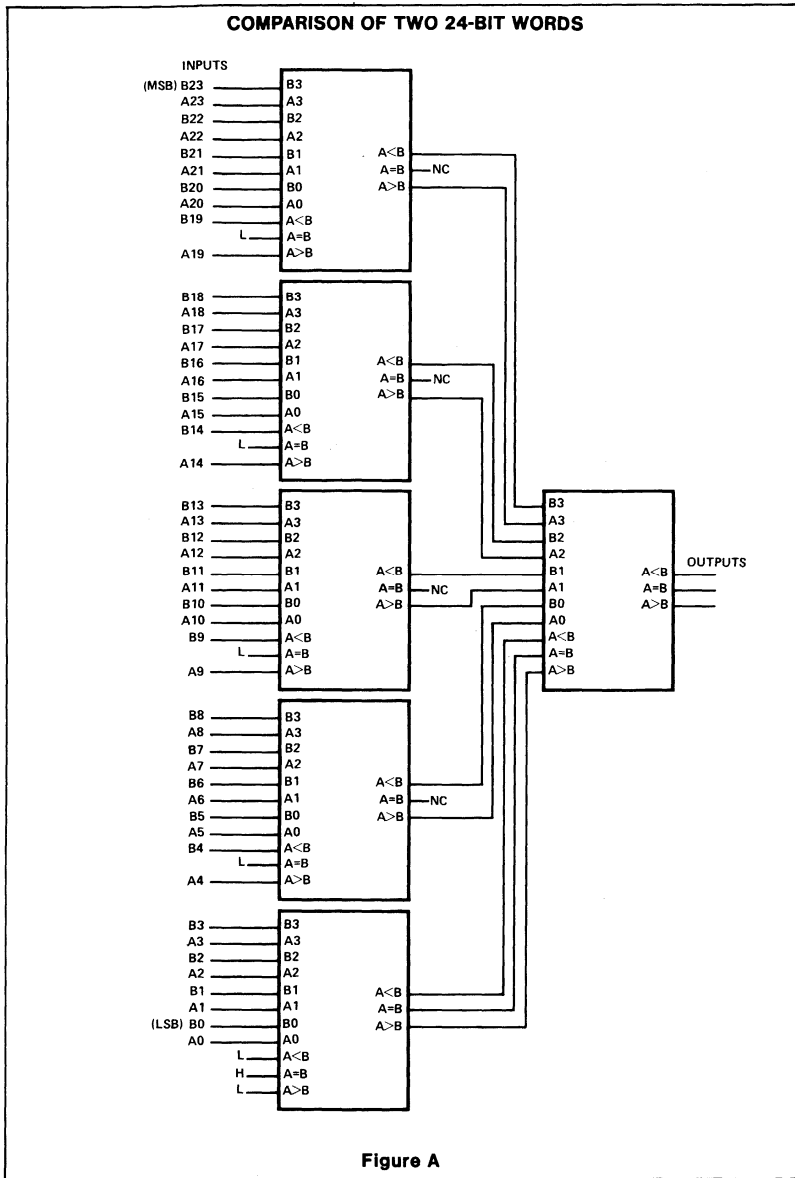
TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$A>B$	$A<B$	$A=B$
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = HIGH voltage level X = Don't care
L = LOW voltage level

LOGIC DIAGRAM





DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

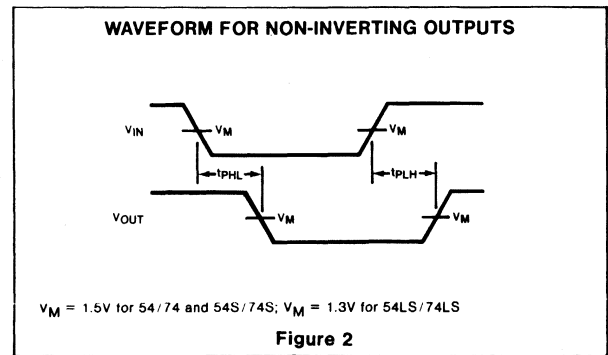
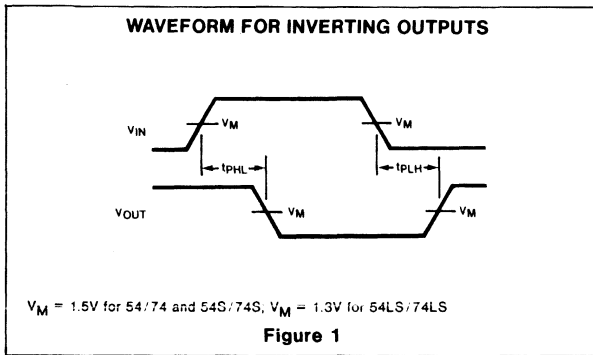
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$		88		115		20	mA
	$V_{CC} = \text{Max}, T_A = 125^\circ\text{C}$ (S54S85W only)				110			mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A or B input to A < B, A > B output		26 30		16 16.5		36 30	ns ns
t _{PLH} t _{PHL}	Propagation delay A or B input to A = B output		35 30		18 16.5		45 45	ns ns
t _{PLH} t _{PHL}	Propagation delay expansion inputs to A < B, A > B, outputs		11 17		7.5 8.5		22 17	ns ns
t _{PLH} t _{PHL}	Propagation delay I _A = B input to A = B output		20 17		10.5 7.5		20 26	ns ns



**54/7486
54S/74S86
54LS/74LS86**

PIN CONFIGURATION

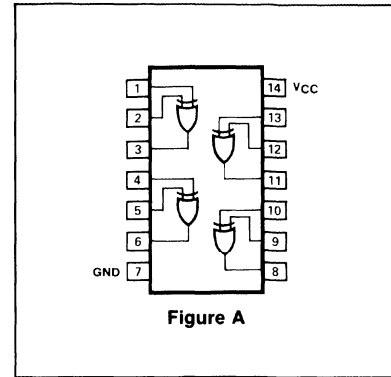


Figure A

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A Fig. A	N7486N N74S86N • N74LS86N	
Ceramic DIP	Fig. A Fig. A	N7486F N74S86F • N74LS86F	S5486F S54S86F • S54LS86F
Flatpak	Fig. A Fig. A		S5486W S54S86W • S54LS86W

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = LOW voltage level
H = HIGH voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40		50	20
	I_{IL} (mA)	-1.6		-2.0	-0.4
Outputs	I_{OH} (μA)	-800		-1000	-400
	I_{OL} (mA)	16		20	$4/8^{(a)}$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_{IN} = 0V$		43				75		10	mA
			50				75		10	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15 pF$ $R_L = 400 \Omega$				$C_L = 15 pF$ $R_L = 280 \Omega$		$C_L = 15 pF$ $R_L = 2k \Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output		23 17				10.5 10		23 17	ns
t_{PLH} t_{PHL}	Propagation delay A or B to output		30 22				10.5 10		30 22	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54S/74S89
54LS/74LS89 (Preliminary data)

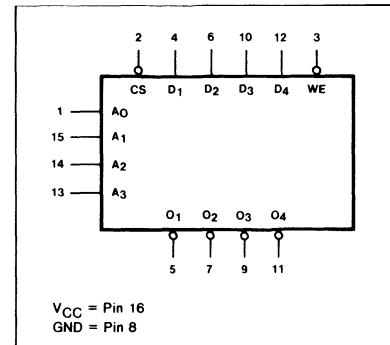
DESCRIPTION

The "89" is a 64-Bit high-speed Read/Write Random Access Memory for use as a "scratch pad" memory with non-destructive read-out. Memory cells are organized in a matrix to provide 16 words of four bits each. Four buffered Address (A₀-A₃) inputs are decoded on the chip to select one of the sixteen memory words for read or write operations. Four buffered Data inputs (D₁-D₄) and four open-collector data outputs are provided for versatile memory expansion. Data at the outputs is inverted from the data which was written into the memory. When the write mode is selected the outputs are the complement of the data inputs.

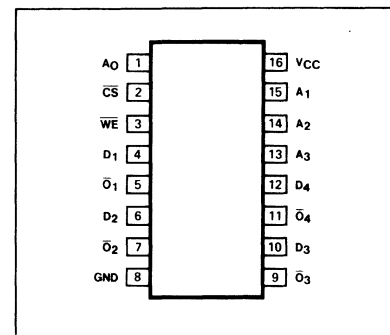
FEATURES

- 16-words by 4-bit memory
- On-chip address decoding
- Inverted data at outputs
- Open collector outputs for easy expansion

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C		MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C	
	Plastic DIP	N74S89N	• N74LS89N	
Ceramic DIP	N74S89F	• N74LS89F	S54S89F	• S54LS89F
Flatpak				

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A ₀ -A ₃	Address inputs	I _{IH} (μA) I _{IL} (μA)		25/10(a) -150/-100(a)	20 -100
\overline{CS}	Chip Select (active LOW) enable input	I _{IH} (μA) I _{IL} (μA)		25/10(a) -150/-100(a)	20 -400
\overline{WE}	Write Enable (active LOW) input	I _{IH} (μA) I _{IL} (μA)		25/10(a) -150/-100(a)	20 -400
D ₁ -D ₄	Data inputs	I _{IH} (μA) I _{IL} (μA)		25/10(a) -150/-100(a)	20 -400
$\overline{O_1}$ - $\overline{O_4}$	Data (inverting) outputs	I _{OH} (μA) I _{OL} (mA)		+100 16	+100 12/24(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "89" is a high-speed array of 64 memory cells organized as 16 words of four bits each. A one-of-sixteen address decoder selects a single word which is specified by the four Address inputs (A₀-A₃). A READ operation is initiated after the address lines are stable when the Write Enable (WE) input is HIGH and the Chip Select-Memory Enable (CS) input is LOW. Data is read at the outputs inverted from the data which was written into the memory.

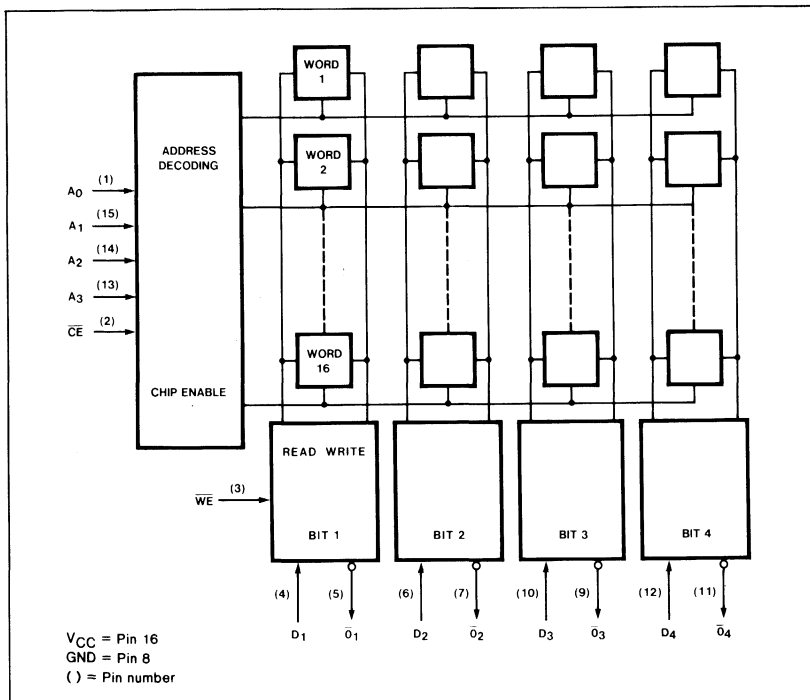
A WRITE operation requires that the WE and CS inputs be LOW. The address inputs must be stable during the WRITE mode for predictable operation. When the write mode is selected the outputs are the complement of the data inputs. The selected memory cells are transparent to changes in the data during the WRITE mode. Therefore, data must be stable one setup time before the LOW-to-HIGH transition of CE or WE.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CS	WE	D _n	O _n
Write	L	L	L	H
	L	L	H	L
Read	L	H	X	Data
Inhibit Writing	H	L	L	H
	H	L	H	L
Store-Disable Outputs	H	H	X	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 Data = Read complement of data from addressed word location

BLOCK DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min, I _{OL} = 16mA	Mil				0.5			V
		Com				0.45			V
	V _{CC} = Min	I _{OL} = 12mA						0.4	V
		I _{OL} = 24mA						0.5 ^(c)	V
I _{CC} Supply Current	V _{CC} = Max	Mil				120		45	mA
		Com				105		37	mA

See BIPOLAR & MOS MEMORY DATA MANUAL for 54S/74S89 AC Characteristics

NOTES

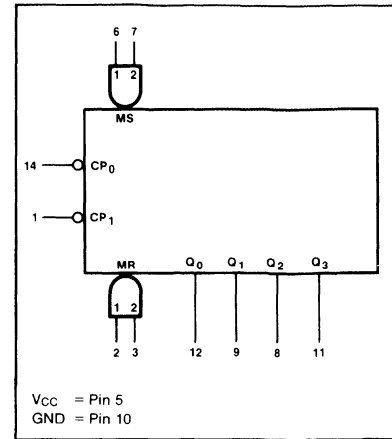
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications
 c. This parameter for Commercial Range only.

54/7490
54LS/74LS90

DESCRIPTION

The "90" is a high-speed 4-bit ripple type decade counter divided into two sections. The counter has a divide-by-two section and a divide-by-five section which are triggered by HIGH-to-LOW transitions on the clock inputs. Either section can be used separately or tied together (Q to \overline{CP}) to form a BCD or a bi-quinary counter. The counter has a 2-input gated Master Reset (Clear) and also a 2-input gated Master Set (Preset 9).

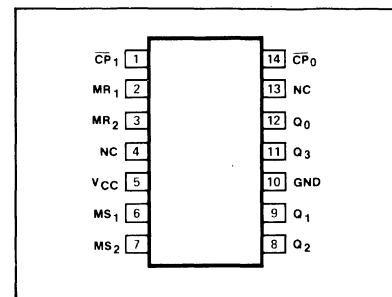
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	V _{CC} = 5V ± 5%; T _A = 0°C to +70°C		V _{CC} = 5V ± 10%; T _A = -55°C to +125°C	
Plastic DIP	N7490N	• N74LS90N		
Ceramic DIP	N7490F	• N74LS90F	S5490F	• S54LS90F
Flatpak			S5490W	• S54LS90W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}_0	Clock (active LOW going edge) input to ÷2 section	I _{IH} (μA) I _{IL} (mA)	80 -3.2		40 -2.4
\overline{CP}_1	Clock (active LOW going edge) input to ÷5 section	I _{IH} (μA) I _{IL} (mA)	160 -6.4		80 -3.2
MR ₁ , MR ₂	Master Reset (Clear) inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
MS ₁ , MS ₂	Master Set (Preset-9) inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
Q ₀	Output from ÷2 section	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8 ^(a)
Q ₁ , Q ₂ , Q ₃	Outputs from ÷5 section	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "90" is a 4-bit ripple type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output is designed and specified to drive the rate fan-out plus the CP₁ input of the device.

A gated AND asynchronous Master Reset (MR₁ • MR₂) is provided which overrides both clock and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set (MS₁ • MS₂) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) Counter the CP₁ input must be externally connected to the Q₀ output. The CP₀ input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the Q₃ output must be connected externally to the CP₀ input. The input count is then applied to the CP₁ input and a divide-by-ten square wave is obtained at output Q₀. To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (CP₀ as the input and Q₀ as the output). The CP₁ input is used to obtain divide-by-five operation at the Q₃ output.

MODE SELECTION—TRUTH TABLE

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X			Count	
X	L	X	L			Count	
L	X	X	L			Count	
X	L	L	X			Count	

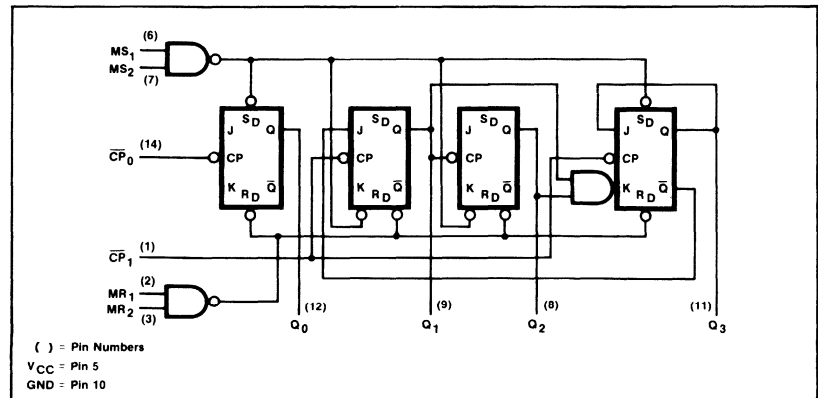
H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE—TRUTH TABLE

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q₀ connected to input CP₁.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		46				15	mA
			53				15	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

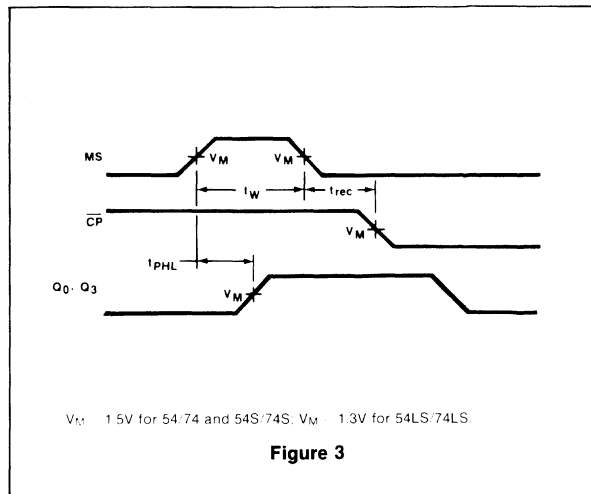
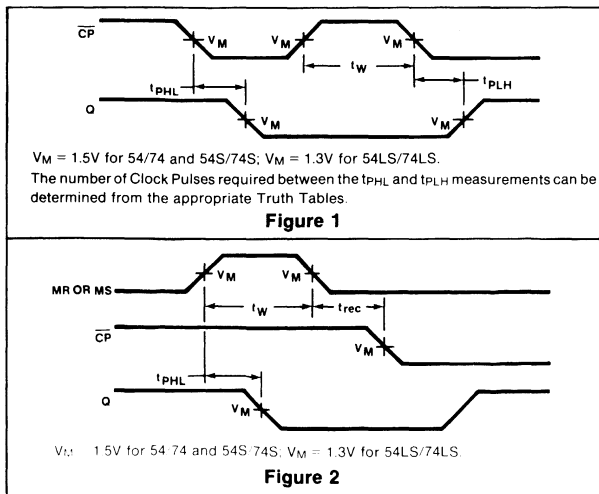
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$				$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	$\overline{\text{CP}}_0$ Input count frequency	Figure 1	10				30	MHz
f_{MAX}	$\overline{\text{CP}}_1$ Input count frequency	Figure 1	10				15	MHz
t_{PLH}	Propagation delay	Figure 1					16	ns
t_{PHL}	$\overline{\text{CP}}_0$ Input to Q_0 Output						18	ns
t_{PLH}	Propagation delay	Figure 1					16	ns
t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_1 Output						21	ns
t_{PLH}	Propagation delay	Figure 1					32	ns
t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_2 Output						35	ns
t_{PLH}	Propagation delay	Figure 1					32	ns
t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_3 Output						35	ns
t_{PLH}	Propagation delay	Figure 1		100			48	ns
t_{PHL}	$\overline{\text{CP}}_0$ Input to Q_3 Output			100			50	ns
t_{PHL}	MR Input to any Output	Figure 2					40	ns
t_{PLH}	MS Input to Q_0 and Q_3 Outputs	Figure 3					30	ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs	Figure 2					40	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w	$\overline{\text{CP}}_0$ Pulse width	Figure 1	50			15		ns
t_w	$\overline{\text{CP}}_1$ Pulse width	Figure 1	50			30		ns
t_w	MR Pulse width	Figure 2	50			15		ns
t_{rec}	Recovery time MR to $\overline{\text{CP}}$	Figure 2				25		ns
t_{rec}	Recovery time MS to $\overline{\text{CP}}$	Figure 2 and 3				25		ns

AC WAVEFORMS



54/7491A

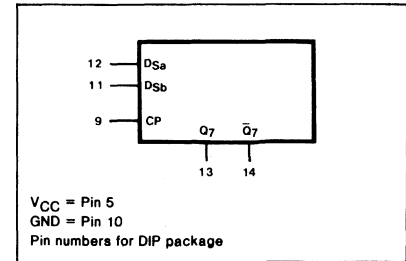
DESCRIPTION

The "91" is an 8-Bit Shift Register with gated serial inputs and true and complement serial outputs. The common buffered Clock (CP) input loads data into the first bit and shifts the register one place to the right synchronous with the LOW-to-HIGH clock transition.

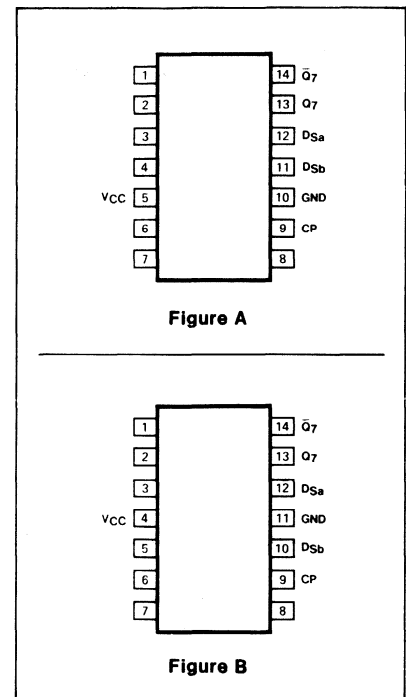
FEATURES

- 8-Bit serial-in-serial-out shift register
- Common buffered clock
- 2-input gate for serial data entry
- True and complement outputs

LOGIC SYMBOL



PIN CONFIGURATIONS



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	Fig. A	N7491AN	
Ceramic DIP	Fig. A	N7491AF	S5491AF
Flatpak	Fig. B		S5491AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D _{Sa} , D _{Sb}	Data Inputs	I_{IH} (μA)	40		
		I_{IL} (mA)	-1.6		
CP	Clock (active HIGH going edge) input	I_{IH} (μA)	40		
		I_{IL} (mA)	-1.6		
Q ₇ & \bar{Q}_7	Outputs	I_{OH} (μA)	-400		
		I_{OL} (mA)	16		

FUNCTIONAL DESCRIPTION

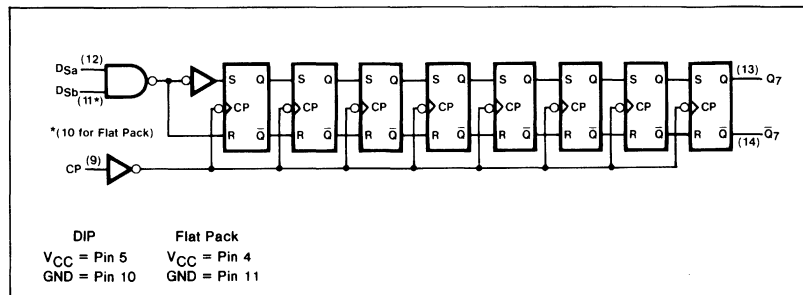
The "91" is an 8-bit serial-in-serial-out shift register. The serial data is entered through a 2-input AND gate (D_{Sa} & D_{Sb}). HIGH data is entered when both D_{Sa} and D_{Sb} are HIGH. LOW data is entered when either serial data input is LOW. The data inputs are edge-triggered and must be stable just one set-up time prior to the LOW-to-HIGH transition of the Clock input (CP) for predictable operation. The data is shifted one bit to the right ($Q_0 \rightarrow Q_1 \rightarrow \dots \rightarrow Q_7$) synchronous with each LOW-to-HIGH clock transition. The "91" has no reset capacity, so initialization requires the shifting in of at least eight bits of known data. Once the register is fully loaded, the Q output follows the serial inputs delayed by eight clock pulses. The complement (\bar{Q}) output from the last stage is also available for simpler decoding applications.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			First Stage		OUTPUTS	
	CP	D_{Sa}	D_{Sb}	Q_0	\bar{Q}_0	Q_7	\bar{Q}_7
Shift, reset first stage	↑	1	X	L	H	q_6	\bar{q}_6
	↑	X	1	L	H	q_6	q_6
Shift, set first stage	↑	h	h	H	L	q_6	\bar{q}_6

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 q_n = Lower case letters indicate the state of the referenced register output one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply Current	$V_{CC} = \text{Max}$	Mil	50					mA
		Com	58					mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Figure 1	10						MHz
t_{PLH} Propagation delay	Figure 1		40					ns
t_{PHL} Clock to output			40					ns

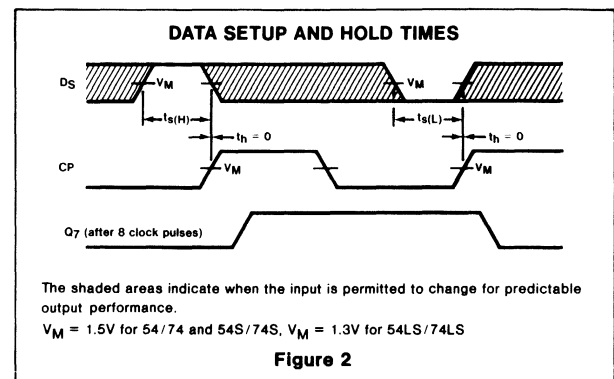
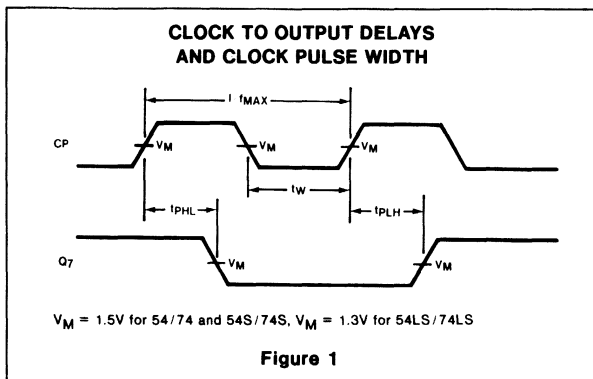
Note

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w Clock pulse width	Figure 1	25						ns
t_s Setup time Data to clock	Figure 2	25						ns
t_h Hold time Data to clock	Figure 2	0						ns

AC WAVEFORMS

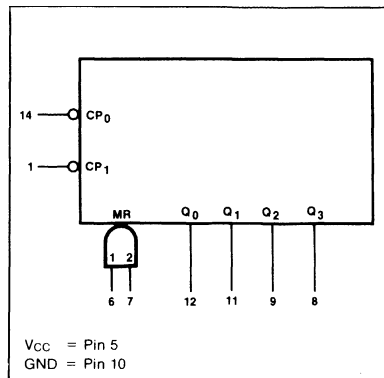


54/7492
54LS/74LS92

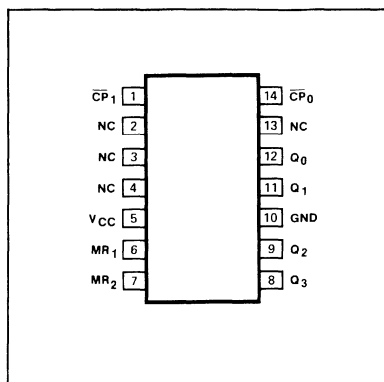
DESCRIPTION

The "92" is a high-speed 4-bit ripple type counter divided into two sections. The counter has a divide-by-two section and a divide-by-six section which are triggered by HIGH-to-LOW transitions of the clock inputs. Either section can be used separately or tied together (Q_0 to \overline{CP}_1) to form a modulo-12 counter. The counter has a 2-input gated Master Reset (Clear).

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7492N • N74LS92N	
Ceramic DIP	N7492F • N74LS92F	S5492F • S54LS92F
Flatpak		S5492W • S54LS92W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}_0	Clock (Active LOW going edge) input to $\div 2$ section	I_{IH} (μA) I_{IL} (mA)	80 -3.2		40 -2.4
\overline{CP}_1	Clock (Active LOW going edge) input to $\div 6$ section	I_{IH} (μA) I_{IL} (mA)	160 -6.4		80 -3.2
MR ₁ , MR ₁	Master Reset (Clear) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
Q ₀	Output from $\div 2$ section	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8 ^(a)
Q ₁ , Q ₂ , Q ₃	Output from $\div 6$ section	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "92" is a 4-bit ripple type Divide-by-12 Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-six section. Each section has separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output is designed and specified to drive the rated fan-out plus the CP₁ input of the device.

A gated AND asynchronous Master Reset (MR₁ MR₂) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a Modulo-12, Divide-by-12 Counter the CP₁ input must be externally connected to the Q₀ output. The CP₀ input receives the incoming count and Q₃ produces a symmetrical divide-by-12 square wave output. In a divide-by-six counter no external connections are required. The first flip-flop is used as a binary element for the divide-by-two function. The CP₁ input is used to obtain divide-by-three operation at the Q₁ and Q₂ outputs and divide-by-six operation at the Q₃ output.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H		Count		
H	L		Count		
L	L		Count		

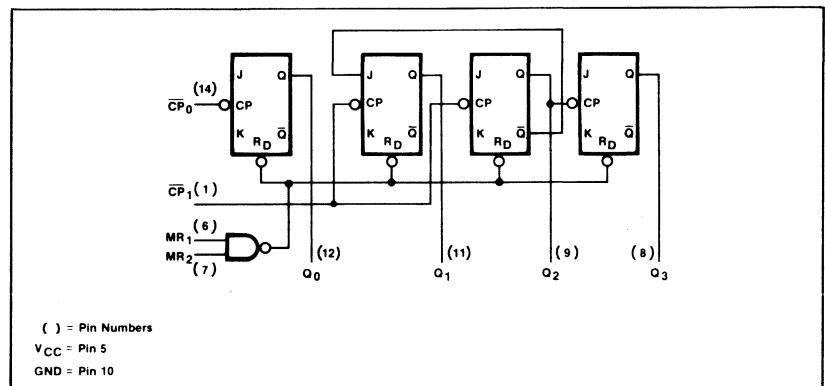
H = HIGH voltage level
L = LOW voltage level
X = Don't care

TRUTH TABLE

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q₀ connected to Input CP₁.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil		44			15	mA
		Com		51			15	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

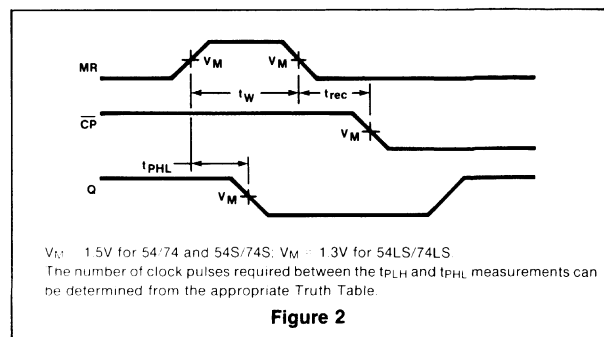
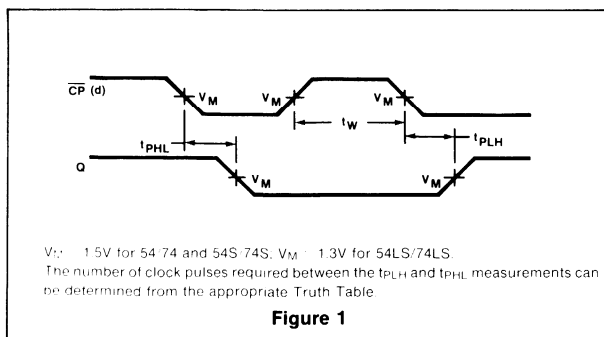
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$				$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	$\overline{\text{CP}}_0$ Input count frequency	Figure 1				32		MHz
f_{MAX}	$\overline{\text{CP}}_1$ Input count frequency	Figure 1				16		MHz
t_{PLH}	Propagation delay	Figure 1				16		ns
t_{PHL}	$\overline{\text{CP}}_0$ input to Q_0 output	Figure 1				18		ns
t_{PLH}	Propagation delay	Figure 1				16		ns
t_{PHL}	$\overline{\text{CP}}_1$ input to Q_1 output	Figure 1				21		ns
t_{PLH}	Propagation delay	Figure 1				16		ns
t_{PHL}	$\overline{\text{CP}}_1$ input to Q_2 output	Figure 1				21		ns
t_{PLH}	Propagation delay	Figure 1				32		ns
t_{PHL}	$\overline{\text{CP}}_1$ input to Q_3 output	Figure 1				35		ns
t_{PLH}	Propagation delay	Figure 1		100		48		ns
t_{PHL}	$\overline{\text{CP}}_0$ input to Q_3 output	Figure 1		100		50		ns
t_{PHL}	$\overline{\text{MR}}$ Input to any output	Figure 2				40		ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w	$\overline{\text{CP}}_0$ Pulse width	Figure 1				15		ns
t_w	$\overline{\text{CP}}_1$ Pulse width	Figure 1				30		ns
t_w	MR Pulse width	Figure 2				15		ns
t_{rec}	Recovery time MR to CP	Figure 2				25		ns

AC WAVEFORMS

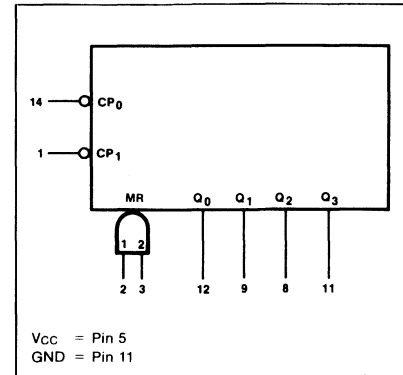


54/7493
54LS/74LS93

DESCRIPTION

The "93" is a high-speed 4-bit ripple type counter divided into two sections. The counter has a divide-by-two section and a divide-by-eight section which are triggered by HIGH-to-LOW transitions on the clock inputs. Either section can be used separately or tied together (Q₀ to CP₁) to form a modulo-16 counter. The counter has a 2-input gated Master Reset (Clear).

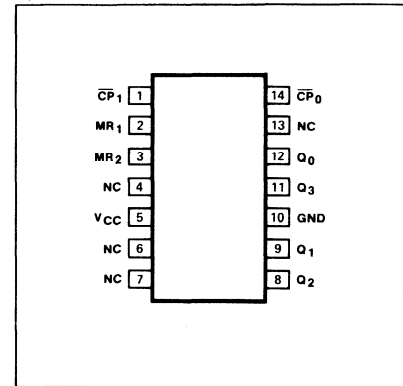
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to 70°C		MILITARY RANGES V _{CC} = 5V ± 10%; T _A = -55°C to +125°C	
	Plastic DIP	N7493N	• N74LS93N	
Ceramic DIP	N7493F	• N74LS93F	S5493F	• S54LS93F
Flatpak			S5493W	• S54LS93W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP ₀	Clock (Active LOW going edge) input (to ÷ 2 Section)	I _{IH} (μA) I _{IL} (mA)	80 -3.2		40 -2.4
CP ₁	Clock (Active LOW going edge) input (to ÷ 8 Section)	I _{IH} (μA) I _{IL} (mA)	80 -3.2		40 -1.6
MR ₁ , MR ₂	Master Reset (Clear) inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
Q ₀	Output from ÷2 section	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8 ^(a)
Q ₁ , Q ₂ , Q ₃	Outputs from ÷8 section	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "93" is a 4-bit ripple type Binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output is designed and specified to drive the rated fan-out plus the \overline{CP}_1 input of the device.

A gated AND asynchronous Master Reset (MR₁ MR₂) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q₀ must be connected externally to input \overline{CP}_1 . The input count pulses are applied to input \overline{CP}_0 . Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q₀, Q₁, Q₂ and Q₃ outputs as shown in the truth table. As a 3-bit ripple counter the input count pulses are applied to input \overline{CP}_1 . Simultaneous frequency divisions of 2, 4 and 8 are available at the Q₁, Q₂ and Q₃ outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

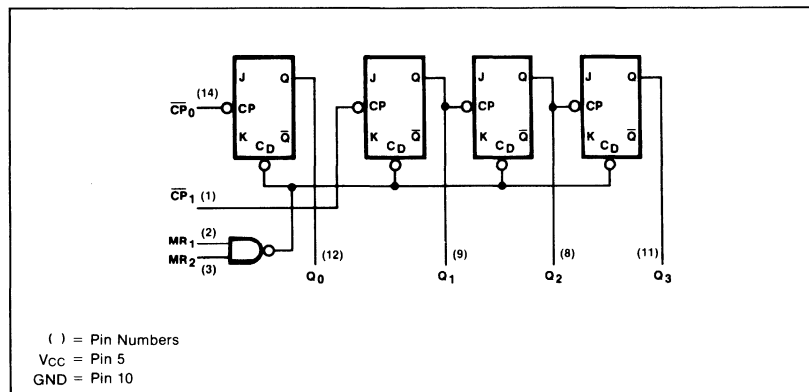
H = HIGH voltage level
L = LOW voltage level
X = Don't care

TRUTH TABLE

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q₀ connected to Input \overline{CP}_1 .

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil	46				15	mA
		Com	53				15	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

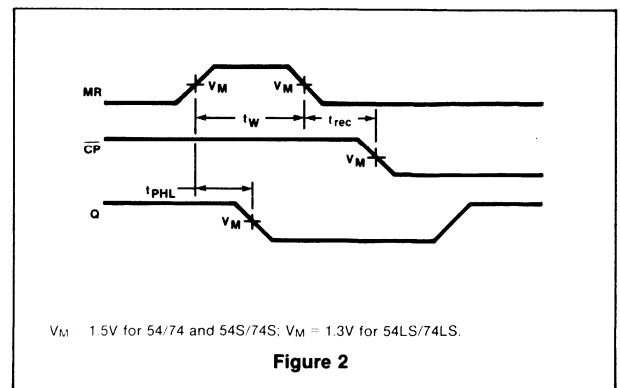
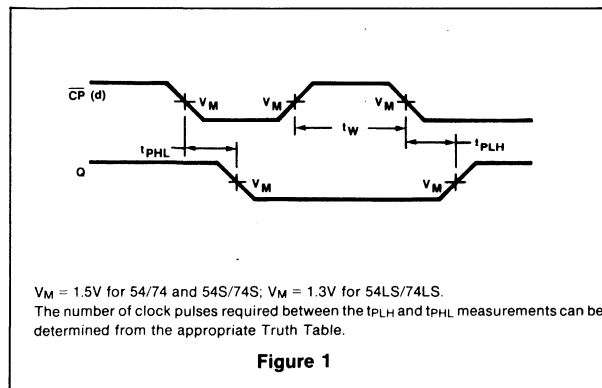
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{ pF}$ $R_L = 400\ \Omega$				$C_L = 15\text{ pF}$ $R_L = 2\text{ k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	\overline{CP}_0 Input count frequency	Figure 1				32		MHz
f_{MAX}	\overline{CP}_1 Input count frequency	Figure 1				16		MHz
t_{PLH}	Propagation delay	Figure 1				16		ns
t_{PHL}	\overline{CP}_0 input to Q_0 output	Figure 1				18		ns
t_{PLH}	Propagation delay	Figure 1				16		ns
t_{PHL}	\overline{CP}_1 input to Q_1 output	Figure 1				21		ns
t_{PLH}	Propagation delay	Figure 1				32		ns
t_{PHL}	\overline{CP}_1 input to Q_2 output	Figure 1				35		ns
t_{PLH}	Propagation delay	Figure 1				51		ns
t_{PHL}	\overline{CP}_1 input to Q_3 output	Figure 1				51		ns
t_{PLH}	Propagation delay	Figure 1		135		70		ns
t_{PHL}	\overline{CP}_0 input to Q_3 output	Figure 1		135		70		ns
t_{PHL}	MR Input to any output	Figure 2				40		ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w	\overline{CP}_0 Pulse width	Figure 1				15		ns
t_w	\overline{CP}_1 Pulse width	Figure 1				30		ns
t_w	MR Pulse width	Figure 2				15		ns
t_{rec}	Recovery time MR to \overline{CP}	Figure 2				25		ns

AC WAVEFORMS



54/7494

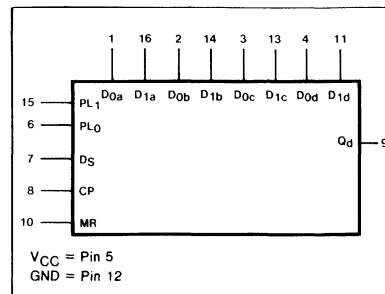
DESCRIPTION

The "94" is a 4-Bit Shift Register with serial and parallel inputs and a serial output. The shifting and serial data entry are synchronous with positive going edge of the clock pulse. The parallel data entry is an asynchronous ones transfer from two sources. The registered can be cleared with a HIGH on the asynchronous Master Reset input.

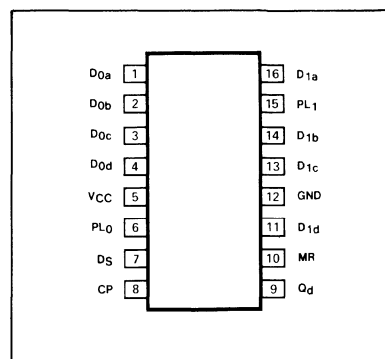
FEATURES

- 4-Bit parallel-to-serial converter
- Two asynchronous ones transfer parallel data ports
- Buffered active HIGH Master Reset
- Buffered positive edge triggered clock

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N7494N	
Ceramic DIP	N7494F	S5494F
Flatpak		S5494W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA)	40		
		I _{IL} (mA)	-1.6		
DS	Serial data input	I _{IH} (μA)	40		
		I _{IL} (mA)	-1.6		
PL ₀ , PL ₁	Parallel Load inputs	I _{IH} (μA)	160		
		I _{IL} (mA)	-6.4		
D _{0a} -D _{0d}	Data inputs from Source "0"	I _{IH} (μA)	40		
		I _{IL} (mA)	-1.6		
D _{1a} -D _{1d}	Data inputs from Source "1"	I _{IH} (μA)	40		
		I _{IL} (mA)	-1.6		
MR	Master Reset (active HIGH) input	I _{IH} (μA)	40		
		I _{IL} (mA)	-1.6		
Q _d	Serial data output	I _{OH} (μA)	-400		
		I _{OL} (mA)	16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "94" is a 4-bit shift register with serial and parallel (ones transfer) data entry. To facilitate parallel ones transfer from two sources, two Parallel Load inputs (PL₀ & PL₁) with associated parallel data inputs (D_{0a}-D_{0d} & D_{1a}-D_{1d}) are provided. To accommodate these extra inputs only the output of the last stage is available. The asynchronous Master Reset (MR) is active HIGH. When MR is HIGH, it overrides the clock and clears the register, forcing Q_d LOW.

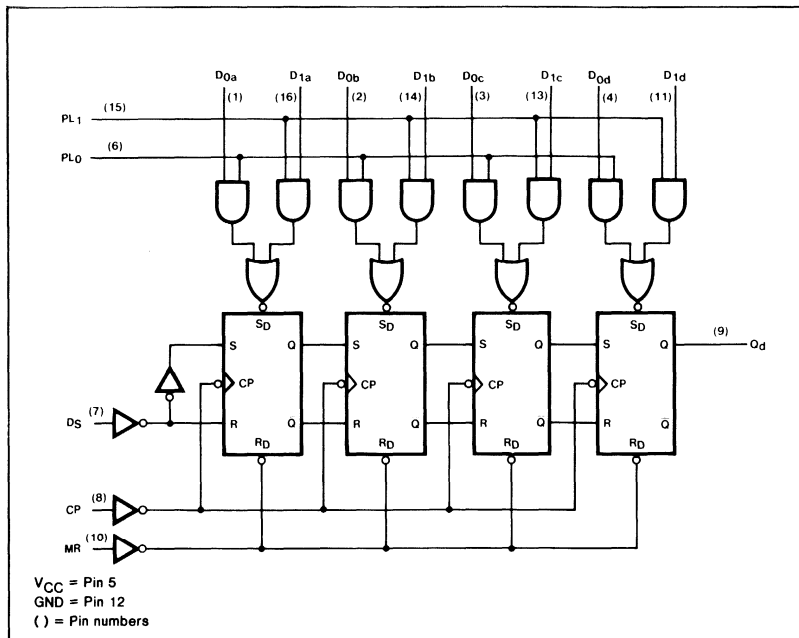
Four flip-flops are connected so that shifting is synchronous; they change state when the clock goes from LOW-to-HIGH. Data is accepted at the serial D_S input prior to this clock transition. The two parallel load inputs and parallel data inputs allow an asynchronous ones transfer from two sources. The flip-flops can be set independently to the HIGH state when the appropriate parallel input is activated. Parallel inputs D_{0a} through D_{0d} are activated during the time the PL₀ is HIGH and Parallel inputs D_{1a} through D_{1d} are activated when PL₁ is HIGH. If both sets of inputs are activated, a HIGH on either input will set the flip-flops to a HIGH. The register should not be clocked while the Parallel Load inputs are activated. The Parallel Load and Parallel Data inputs will override the MR if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	PL ₀	PL ₁	D _{0n}	D _{1n}	MR	CP	D _S	Q _a	Q _b	Q _c	Q _d
Parallel Load	H	L	L	X	X	X	X	Q _a	Q _b	Q _c	Q _d
	H	L	H	X	X	X	X	H	H	H	H
	L	H	X	L	X	X	X	Q _a	Q _b	Q _c	Q _d
Reset (clear)	L	L	X	X	H	X	X	L	L	L	L
Shift right	L	L	X	X	L	↑	l	L	q _a	q _b	q _c
	L	L	X	X	L	↑	h	H	q _a	q _b	q _c

- H = HIGH voltage level
- h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
- L = LOW voltage level
- l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
- q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition
- x = Don't care
- ↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max.	Mil	50					mA
		Com	58					mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω						
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1	10						MHz
t _{PLH} Propagation delay	Figure 1		40					ns
t _{PHL} Clock to output			40					ns
t _{PLH} Propagation delay Parallel Load or Parallel Data to output	Figure 2		35					ns
t _{PHL} Propagation delay MR to output	Figure 2		40					ns

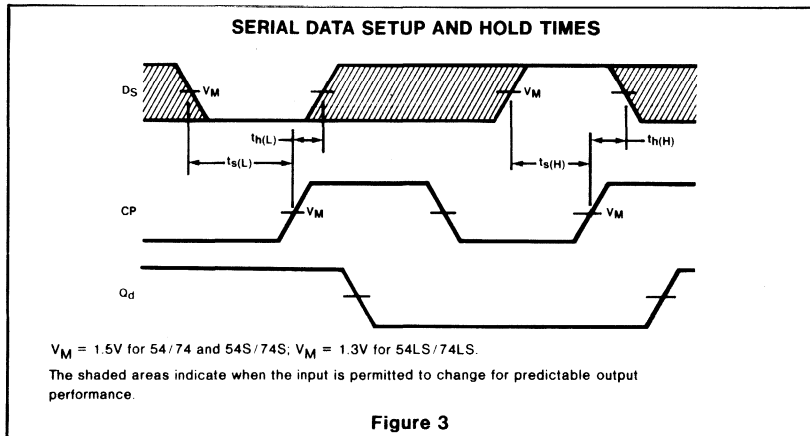
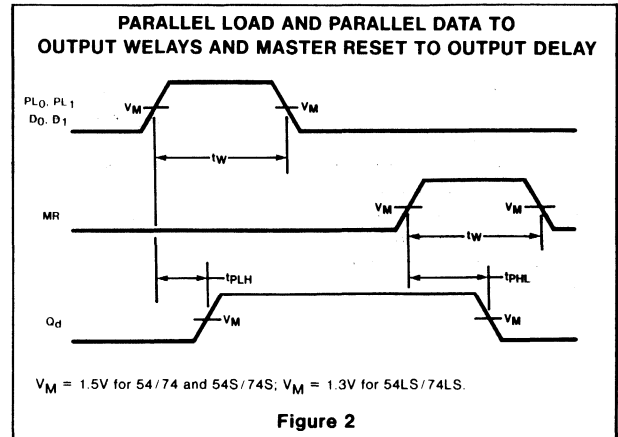
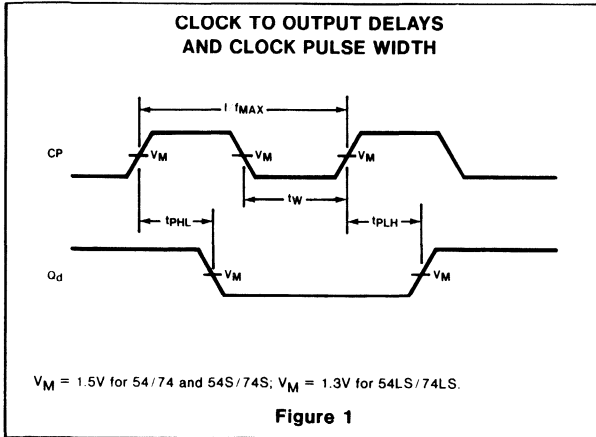
NOTE

b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _{W(L)} Clock pulse width, LOW	Figure 1	35						ns
t _{W(H)} MR pulse width, HIGH	Figure 2	30						ns
t _{W(H)} Parallel Load or Data pulse width, HIGH	Figure 2	30						ns
t _{S(H)} Setup time HIGH D _S to CP	Figure 3	35						ns
t _{S(L)} Setup time LOW D _S to CP	Figure 3	25						ns
t _H Hold time HIGH or LOW D _S to CP	Figure 3	0						ns

AC WAVEFORMS



54/7495A
54LS/74LS95B

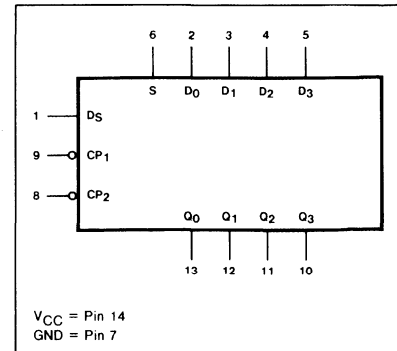
DESCRIPTION

The "95" is a 4-Bit Shift Register with serial and parallel synchronous modes. Separate clock inputs selected by a mode select input activate the serial shift right and parallel load. The data is transferred from the serial or parallel D inputs to the Q outputs synchronously with the HIGH-to-LOW transition of the appropriate clock input.

FEATURES

- Separate negative-edge-triggered shift and parallel load clocks
- Common mode control input
- Shift right serial input
- Synchronous shift or load capabilities

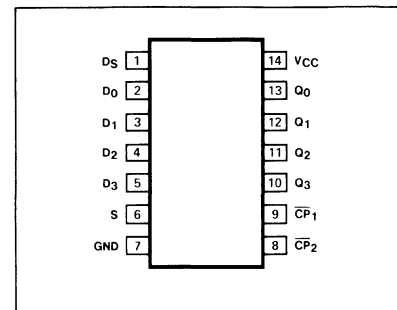
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	N7495AN	• N74LS95BN		
Ceramic DIP	N7495AF	• N74LS95BF	S5495AF	• S54LS95BF
Flatpak			S5495AW	• S54LS95BW

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}_1	Serial Clock (active LOW going edge) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
\overline{CP}_2	Parallel Clock (active LOW going edge) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
S	Mode Select input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		20 -0.4
D_S	Serial Data input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
D_0-D_3	Parallel Data input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
Q_0-Q_3	Register outputs	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "95" is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a serial data (D_S) and four parallel data (D_0 - D_3) inputs and four parallel outputs (Q_0 - Q_3). The serial or parallel mode of operation is controlled by a mode select input (S) and two clock inputs (\overline{CP}_1 and \overline{CP}_2). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected clock input.

When the mode select input (S) is HIGH, \overline{CP}_2 is enabled. A HIGH-to-LOW transition on enabled \overline{CP}_2 loads parallel data from the D_0 - D_3 inputs into the register. When S is LOW, \overline{CP}_1 is enabled. A HIGH-to-LOW transition on enabled \overline{CP}_1 shifts the data from serial input D_S to Q_0 and transfers the data in Q_0 to Q_1 , Q_1 to Q_2 , and Q_2 to Q_3 respectively (shift right). Shift left is accomplished by externally connecting Q_3 to D_2 , Q_2 to D_1 , Q_1 to D_0 and operating the "95" in the parallel mode (S=HIGH).

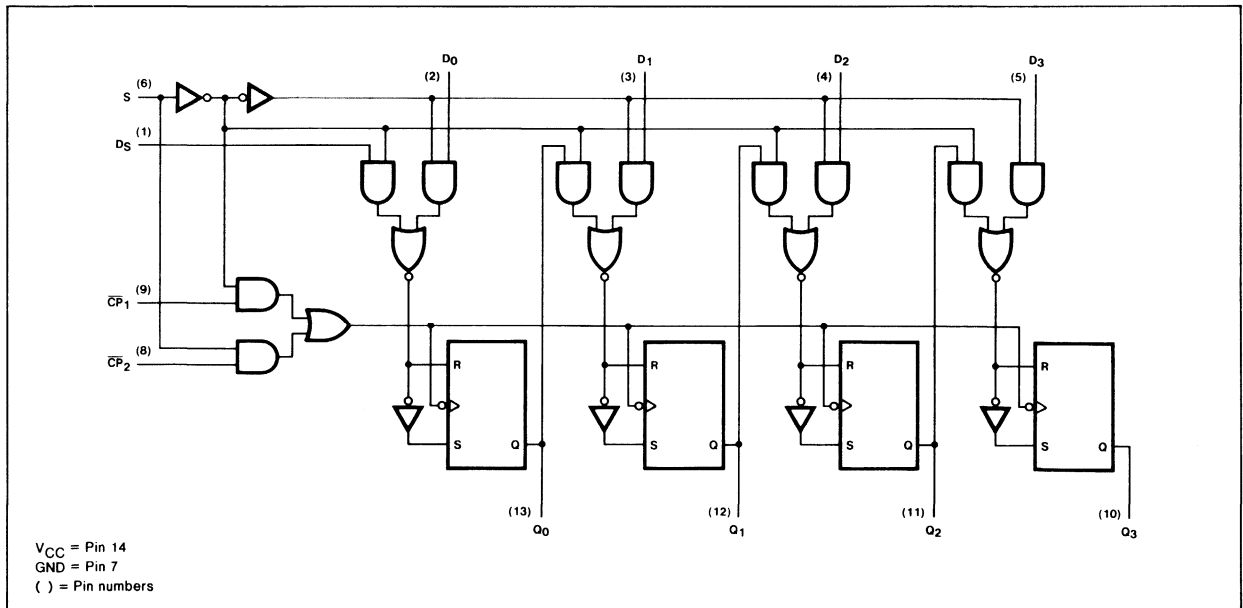
In normal operations the mode select (S) should change states only when both Clock inputs are LOW. However, changing S from HIGH-to-LOW while \overline{CP}_2 is LOW, or changing S from LOW-to-HIGH while \overline{CP}_1 is LOW will not cause any changes on the register outputs.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	\overline{CP}_1	\overline{CP}_2	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Parallel Load	H	X	↓	X	l	L	L	L	L
	H	X	↓	X	h	H	H	H	H
Shift right	L	↓	X	l	X	L	q ₀	q ₁	q ₂
	L	↓	X	h	X	H	q ₀	q ₁	q ₂
Mode change	↑	L	X	X	X	no change			
	↑	H	X	X	X	undetermined			
	↓	X	L	X	X	no change			
	↓	X	H	X	X	undetermined			

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
 ↓ = HIGH-to-LOW transition of Clock or mode Select.
 ↑ = LOW-to-HIGH transition of mode Select.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		63				21	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum Clock Frequency	Figure 1	25				25		MHz
t _{PLH} Propagation delay	Figure 1		27				27	ns
t _{PHL} Clock to output	Figure 1		32				32	ns

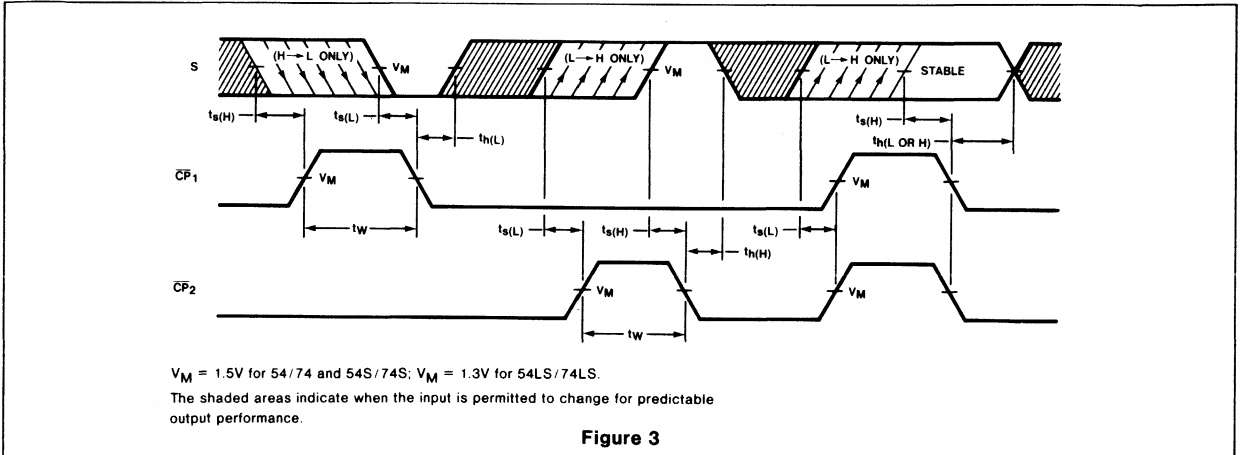
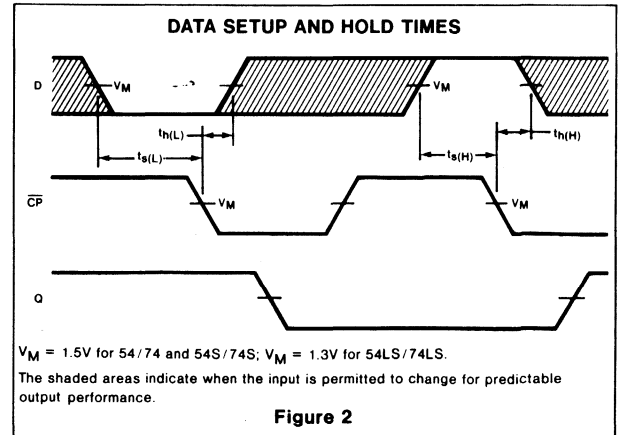
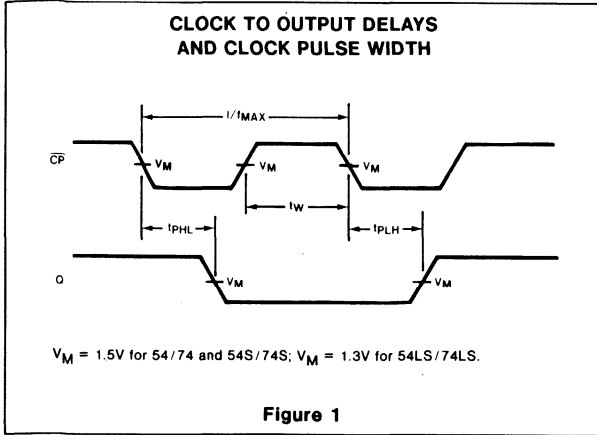
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _{W(H)} Clock pulse width, HIGH	Figure 1	20				20		ns
t _s Setup time Data to Clock	Figure 2	15				20		ns
t _h Hold time Data to Clock	Figure 2	0				10		ns
t _{s(L)} Setup time LOW Mode Select to \overline{CP}_1	Figure 3	30				20		ns
t _{h(L)} Hold time LOW Mode Select to \overline{CP}_1	Figure 3	0				0		ns
t _{s(H)} Setup time HIGH Mode Select to \overline{CP}_2	Figure 3	30				20		ns
t _{h(H)} Hold time HIGH Mode Select to \overline{CP}_2	Figure 3	0				0		ns
t _{s(H)} Setup time HIGH Mode Select to \overline{CP}_1 (L→H)	Figure 3	5				20		ns
t _{s(L)} Setup time LOW Mode Select to \overline{CP}_2 (L→H)	Figure 3	5				20		ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54/7496
54LS/74LS96

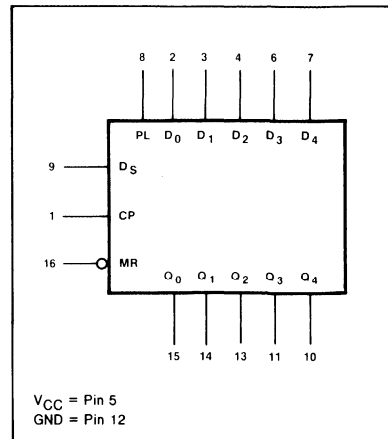
DESCRIPTION

The "96" is a 5-Bit Shift Register with serial and parallel data inputs and parallel outputs. The shifting and serial data entry are synchronous with the positive going edge of the clock pulse. The parallel data entry is an asynchronous ones transfer. The register can be cleared with a LOW on the asynchronous Master Reset input.

FEATURES

- 5-Bit parallel-to-serial or serial-to-parallel converter
- Asynchronous ones transfer parallel data entry
- Buffered positive triggered clock
- Buffered active LOW Master Reset

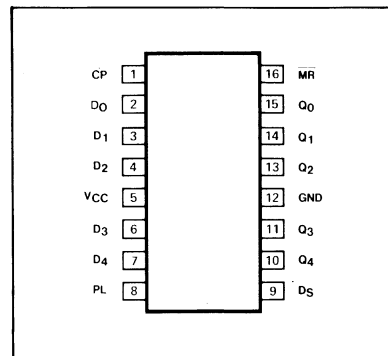
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N7496N • N74LS96N	
Ceramic DIP	N7496F • N74LS96F	S5496F • S54LS96F
Flatpak		S5496W • S54LS96W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		20 -0.4
DS	Serial Data input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		20 -0.4
D ₀ -D ₄	Parallel Data input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		20 -0.4
PL	Parallel Load input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	200 -8.0		100 -2.0
MR	Master Reset (active LOW) input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		20 -0.4
Q ₀ -Q ₄	Register outputs	$I_{OH} (\mu A)$ $I_{OL} (mA)$	-400 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "96" is a 5-bit shift register with both serial and parallel (ones transfer) data entry. Since the "96" has the output of each stage available as well as a D-type serial input and ones transfer inputs on each stage, it can be used in 5-bit serial-to-parallel, serial-to-serial and some parallel-to-serial data operations.

The "96" is five master / slave flip-flops connected to perform right shift. The flip-flops change state on the LOW-to-HIGH transition of the clock. The serial data (D_S) input is edge-triggered and must be stable only one setup time before the LOW-to-HIGH clock transition.

Each flip-flop has asynchronous set inputs allowing them to be independently set HIGH. The set inputs are controlled by a common active HIGH Parallel Load (PL) input. The PL input is not buffered, and care must be taken not to overload the driving element. When the PL is HIGH, a HIGH on the parallel data (D_0 - D_4) inputs will set the associated flip-flops HIGH. A LOW on the D_0 - D_4 inputs will cause "no change" in the appropriate flip-flops.

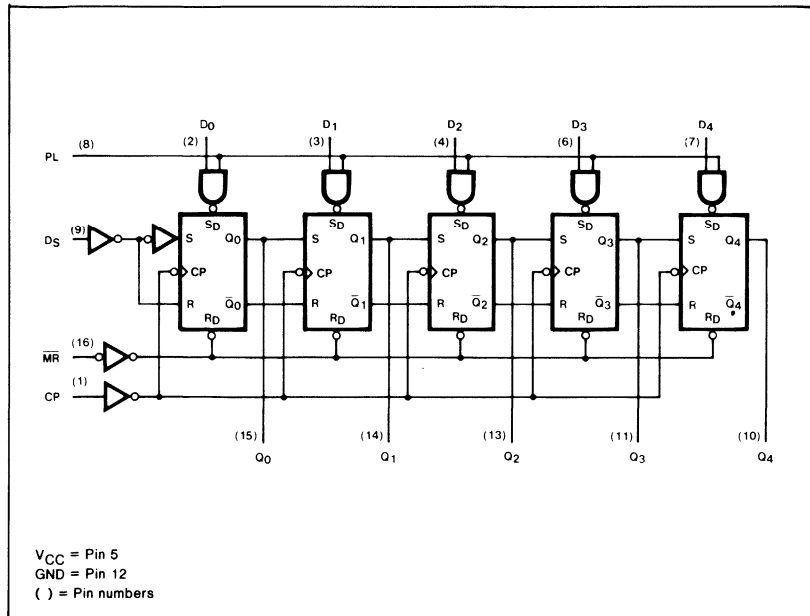
The asynchronous active LOW Master Reset (\overline{MR}) is buffered. When LOW, the \overline{MR} overrides the clock and clears the register if the PL is not active. The parallel load inputs override the \overline{MR} forcing the flip-flops HIGH if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS				
	PL	D_n	MR	CP	D_S	Q_0	Q_1	Q_2	Q_3	Q_4
Parallel Load	H	L	X	X	X	Q_0	Q_1	Q_2	Q_3	Q_4
	H	H	X	X	X	H	H	H	H	H
Reset (clear)	L	X	L	X	X	L	L	L	L	L
Shift right	L	X	H	↑	l	L	q_0	q_1	q_2	q_3
	L	X	H	↑	h	H	q_0	q_1	q_2	q_3

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil	68				20	mA
		Com	79				20	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

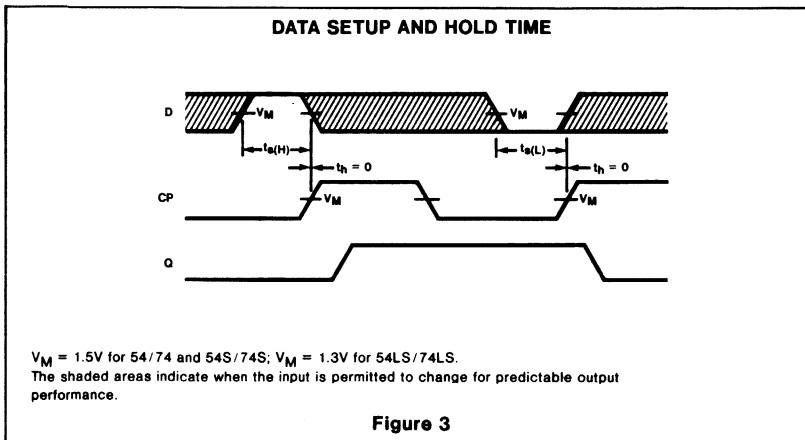
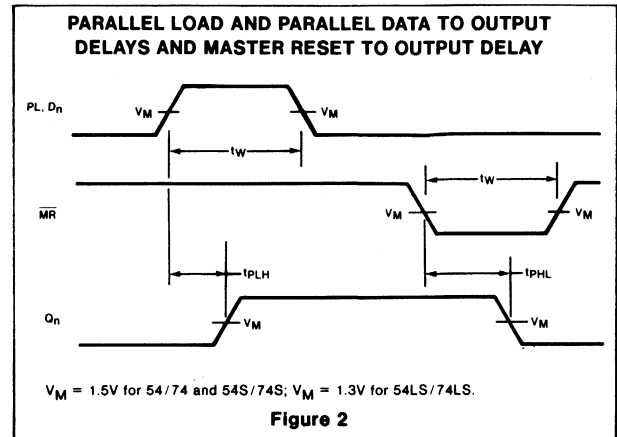
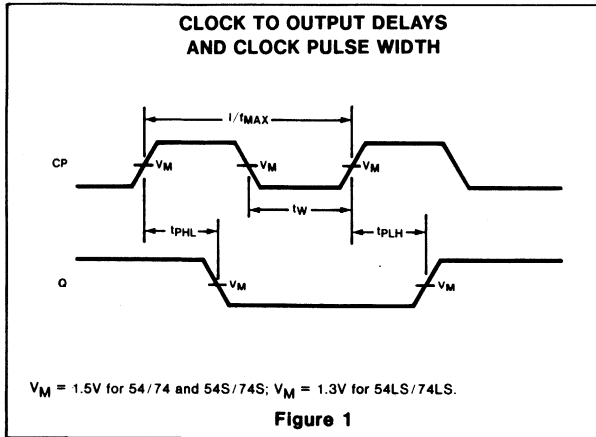
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2KΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1	10				25		MHz
t _{PLH} Propagation delay	Figure 1		40				40	ns
t _{PHL} Clock to output			40				40	ns
t _{PLH} Propagation delay Parallel Load or Parallel Data to output	Figure 2		35				35	ns
t _{PHL} Propagation delay MR to output	Figure 2		55				55	ns

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _W (L) Clock pulse width, LOW	Figure 1	35				20		ns
t _W (L) $\overline{\text{MR}}$ pulse width, LOW	Figure 2	30				30		ns
t _W (H) Parallel Load or Data pulse width, HIGH	Figure 2	30				30		ns
t _s Setup time D _S to CP	Figure 3	30				30		ns
t _h Hold time D _S to CP	Figure 3	0				0		ns

NOTE

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.



54/74100

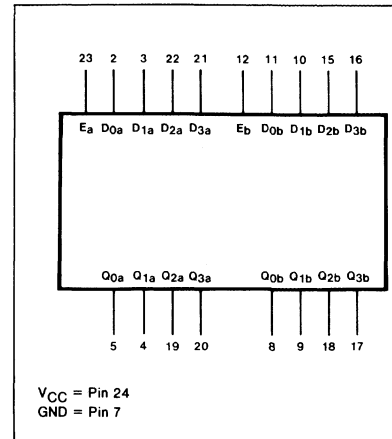
DESCRIPTION

The "100" is a Dual 4-Bit Transparent Latch. Each 4-bit latch has an active HIGH enable for easy expansion. When the Enable input (E) is HIGH, the data on the D inputs is loaded into the latch and appear at the outputs. A LOW on the enable will latch the data and hold the outputs stable.

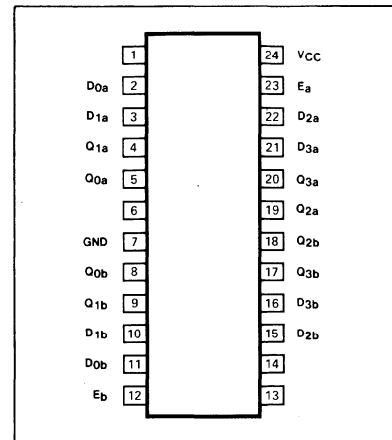
FEATURES

- Two independent 4-bit latches
- See "116" for asynchronous Master Reset version
- See "373" for 20-pin package version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74100N	
Ceramic DIP	N74100F	S54100F
Flatpak		S54100W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
E	Enable (active HIGH) input	I_{IH} (μA) I_{IL} (mA)	320 -12.8		
D ₀ -D ₃	Data inputs	I_{IH} (μA) I_{IL} (mA)	80 -3.2		
Q ₀ -Q ₃	Latch outputs	I_{OH} (μA) I_{OL} (mA)	-400 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

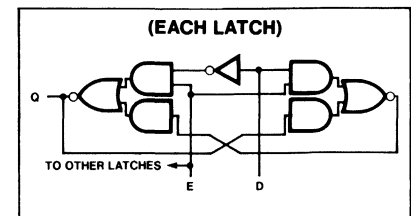
FUNCTIONAL DESCRIPTION

The "100" has two independent 4-bit transparent latches. Each 4-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the output. The outputs follow the data inputs as long as E is HIGH. The data on the D inputs one set-up time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS
	E	D _n	Q _n
Data Enabled	H H	L H	L H
Data Latched	L	X	q

LOGIC DIAGRAM



H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max, All inputs = 0V	Mil		92				mA
		Com		106				mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Enable to output	Figure 1	C _L = 15pF R _L = 400Ω						ns
			30					ns
t _{PLH} Propagation delay t _{PHL} Data to output	Figure 2		30					ns
			25					ns

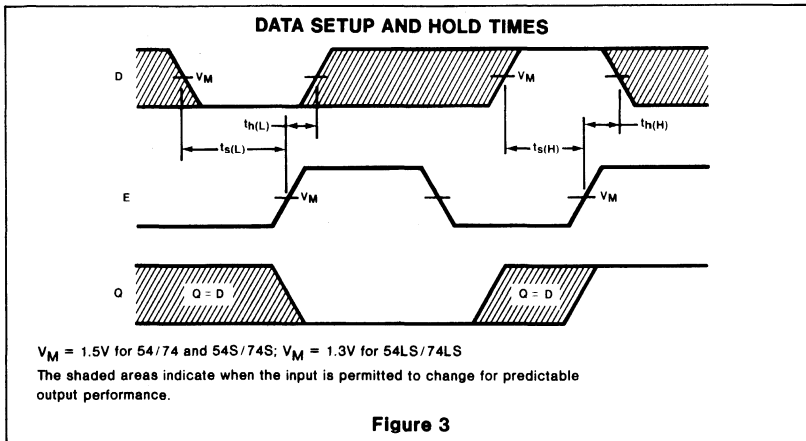
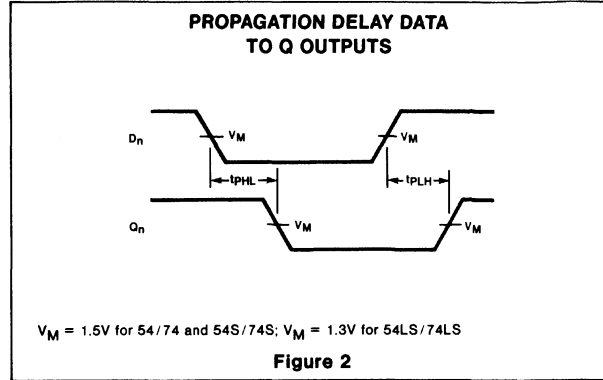
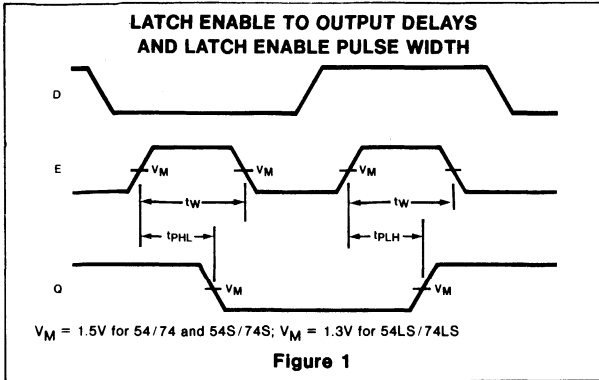
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Enable pulse width	Figure 1	20						ns
t _s Setup time Data to enable	Figure 3	20						ns
t _h Hold time Data to enable	Figure 3	5.0						ns

AC WAVEFORMS



54H/74H101

DESCRIPTION

The "101" is a JK Negative Edge-Triggered Flip-Flop featuring AND-OR gated JK inputs and a direct Set input. The Set (\bar{S}_D) is an asynchronous active LOW input. When LOW, the \bar{S}_D overrides the clock and data inputs and sets the Q output HIGH and the \bar{Q} output LOW.

A HIGH level on the Clock (\overline{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the \overline{CP} is HIGH, and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \overline{CP} .

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74H101N	
Ceramic DIP	Fig. A	N74H101F	S54H101F
Flatpak	Fig. B		S54H101W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP}	Clock input	I_{IH} (μA)		-1.0		
		I_{IL} (mA)		-4.8		
\bar{S}_D	Set input	I_{IH} (μA)		100		
		I_{IL} (mA)		-2.0		
JK	Data inputs	I_{IH} (μA)		50		
		I_{IL} (mA)		-2.0		
Q & \bar{Q}	Outputs	I_{OH} (μA)		-500		
		I_{OL} (mA)		20		

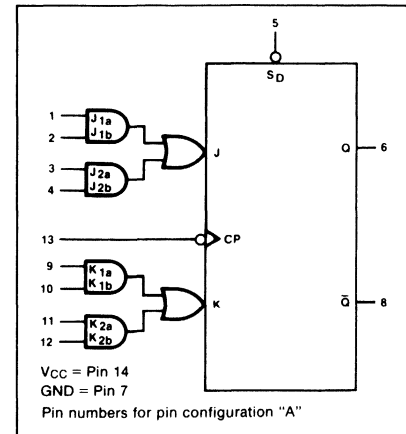
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$I_{IH}(\overline{CP})$	Input HIGH current			0	-1.0					mA
I_{CC}	Supply current				38					mA

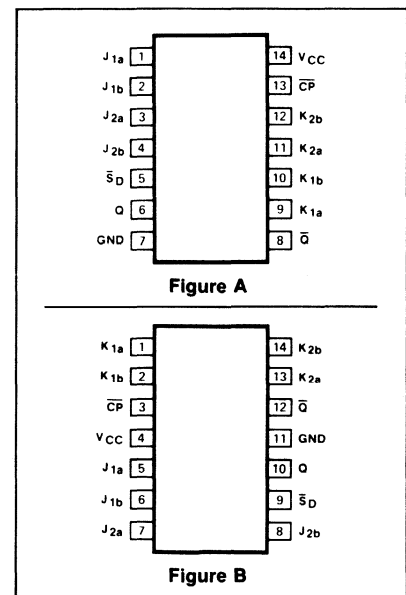
NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

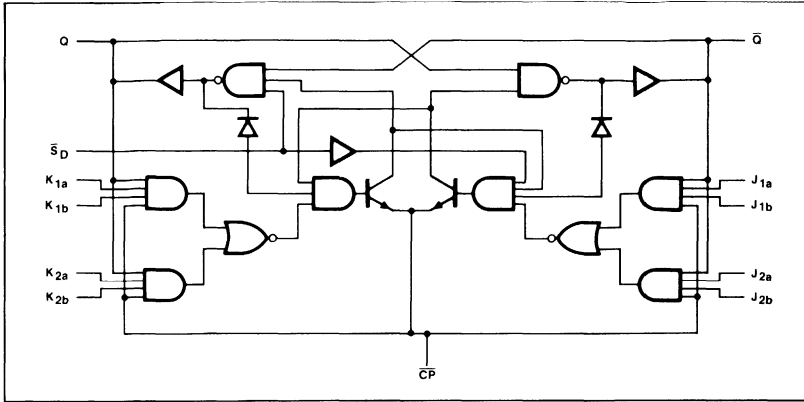
LOGIC SYMBOL



PIN CONFIGURATIONS



LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\overline{CP}	J	K	Q	\bar{Q}
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	\bar{q}	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
 $J = (J_{1a} \cdot J_{1b}) + (J_{2a} \cdot J_{2b})$
 $K = (K_{1a} \cdot K_{1b}) + (K_{2a} \cdot K_{2b})$

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
					$C_L = 25 \text{ pF}$ $R_L = 280 \Omega$						
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 4			40						MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 4				15 20					ns ns
t_{PLH}	Propagation delay Set to output	Waveform 5				12					ns
t_{PHL}		Waveform 5, CP = HIGH				20					ns
t_{PHL}		Waveform 5, CP = LOW				35					ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)	Waveform 4			10						ns
$t_{w(L)}$	Clock pulse width (LOW)	Waveform 4			15						ns
$t_{w(L)}$	Set pulse width (LOW)	Waveform 5			16						ns
$t_{s(H)}$	Setup time HIGH J or K to Clock	Waveform 4			10						ns
$t_{h(H)}$	Hold time HIGH J or K to Clock	Waveform 4			0						ns
$t_{s(L)}$	Setup time LOW J or K to Clock	Waveform 4			13						ns
$t_{h(L)}$	Hold time LOW J or K to Clock	Waveform 4			0						ns

54H/74H102

DESCRIPTION

The "102" is a JK Negative Edge-Triggered Flip-Flop with gated JK inputs and direct Set and Reset inputs. The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the clock and data inputs forcing the outputs to their steady state level as shown in the Truth Table.

A HIGH level on the Clock (\overline{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the \overline{CP} is HIGH, and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \overline{CP} .

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74H102N	
Ceramic DIP	Fig. A	N74H102F	S54H102F
Flatpak	Fig. B		S54H102W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP} Clock input	I_{IH} (μA) I_{IL} (mA)		-1.0 -4.8		
\bar{R}_D Reset input	I_{IH} (μA) I_{IL} (mA)		100 -2.0		
\bar{S}_D Set input	I_{IH} (μA) I_{IL} (mA)		100 -2.0		
JK Data inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0		
Q & \bar{Q} Outputs	I_{OH} (μA) I_{OL} (mA)		-500 20		

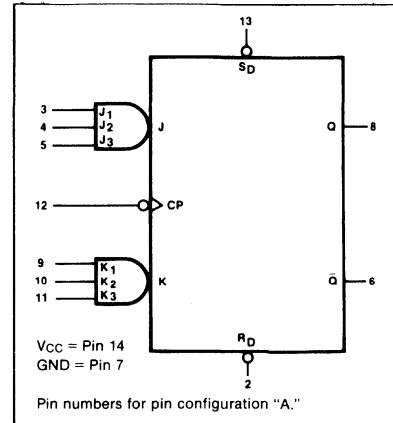
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$I_{IH}(\overline{CP})$ Input HIGH current	$V_{CC} = \text{Max}, V_{CP} = 2.4V$			0	-1.0					mA
I_{CC} Supply current	$V_{CC} = \text{Max}, V_{CP} = 0V$				38					mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC SYMBOL



PIN CONFIGURATIONS

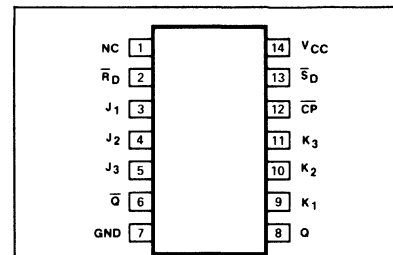


Figure A

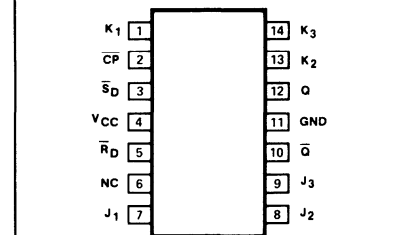
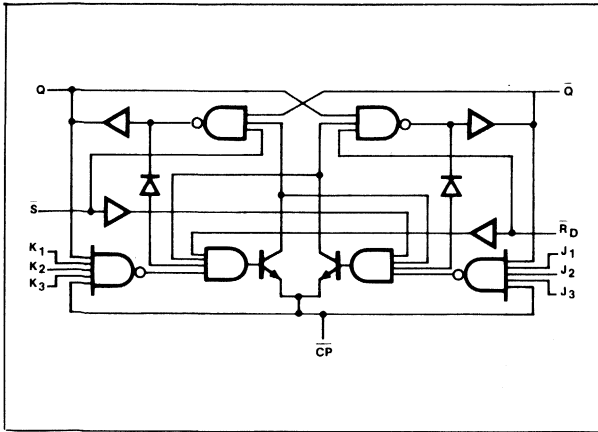


Figure B

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	$\bar{C}P$	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	q	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	q

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
 J = J₁ • J₂ • J₃
 K = K₁ • K₂ • K₃

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				C _L = 25pF R _L = 280Ω						
		Min	Max	Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock frequency				40					MHz
t _{PLH} t _{PHL}	Propagation delay Clock to Output				15 20					ns ns
t _{PLH}	Propagation delay Set or Reset to Output	Waveform 5			12					ns
t _{PHL}		Waveform 5, CP = HIGH			20					ns
t _{PHL}		Waveform 5, CP = LOW			35					ns

AC SETUP REQUIREMENTS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{w(H)}	Clock pulse width (HIGH)			10						ns
t _{w(L)}	Clock pulse width (LOW)			15						ns
t _{w(L)}	Set or Reset pulse width (LOW)			16						ns
t _{s(H)}	Setup time HIGH J or K to Clock			10						ns
t _{h(H)}	Hold time HIGH J or K to Clock			0						ns
t _{s(L)}	Setup time LOW J or K to Clock			13						ns
t _{h(L)}	Hold time LOW J or K to Clock			0						ns

NOTE

c. Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

54H/74H103

DESCRIPTION

The "103" is a Dual JK Negative Edge-Triggered Flip-Flop with separate Clock and direct Reset inputs. The Reset ($\overline{R_D}$) is an asynchronous active LOW input. When LOW, the $\overline{R_D}$ overrides the Clock and data inputs and resets (clears) the flip-flop.

A HIGH level on the Clock (\overline{CP}) input en-

ables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the \overline{CP} is HIGH, and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \overline{CP} .

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74H103N	
Ceramic DIP	Fig. A	N74H103F	S54H103F
Flatpak	Fig. A		S54H103W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP} Clock input	I_{IH} (μA)		-1.0		
	I_{IL} (mA)		-4.8		
$\overline{R_D}$ Reset input	I_{IH} (μA)		100		
	I_{IL} (mA)		-2.0		
JK Data inputs	I_{IH} (μA)		50		
	I_{IL} (mA)		-2.0		
Q & \overline{Q} Outputs	I_{OH} (μA)		-500		
	I_{OL} (mA)		20		

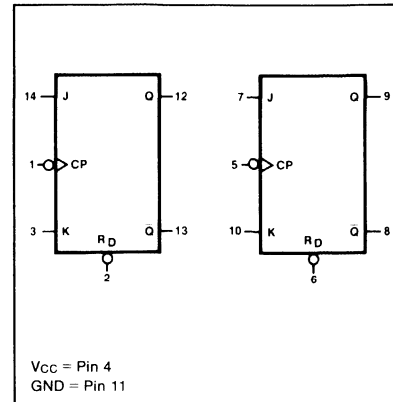
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$I_{IH}(\overline{CP})$ Input HIGH current	$V_{CC} = \text{Max}, V_{CP} = 2.4V$			0	-1.0					mA
I_{CC} Supply current	$V_{CC} = \text{Max}, V_{CP} = 0V$				76					mA

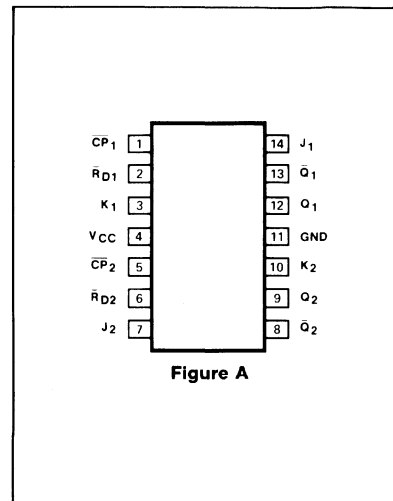
NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

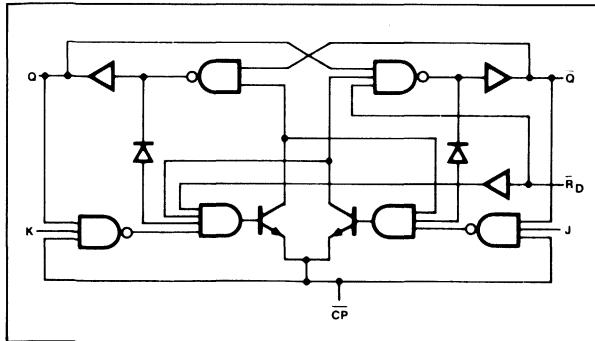
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{R}_D	CP	J	K	Q	\bar{Q}
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	↓	h	h	\bar{q}	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				$C_L = 25\text{pF}$ $R_L = 280\Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum Clock frequency	Waveform 4			40						MHz
t_{PLH} Propagation delay t_{PHL} Clock to Output	Waveform 4				15 20					ns ns
t_{PLH} Propagation delay t_{PHL} Reset to Output	Waveform 5				12					ns
	Waveform 5, CP = HIGH				20					ns
	Waveform 5, CP = LOW				35					ns

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$ Clock pulse width (HIGH)	Waveform 4			10						ns
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 4			15						ns
$t_{w(L)}$ Set or Reset pulse width (LOW)	Waveform 5			16						ns
$t_s(H)$ Setup time HIGH J or K to Clock	Waveform 4			10						ns
$t_h(H)$ Hold time HIGH J or K to Clock	Waveform 4			0						ns
$t_s(L)$ Setup time LOW J or K to Clock	Waveform 4			13						ns
$t_h(L)$ Hold time LOW J or K to Clock	Waveform 4			0						ns

54H/74H106

DESCRIPTION

The "106" is a Dual JK Negative Edge-Triggered Flip-Flop with individual JK, Clock, direct Set and direct Reset inputs. The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and data inputs forcing the outputs to their steady state level as shown in the Truth Table.

A HIGH level on the Clock (\overline{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the \overline{CP} is HIGH, and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \overline{CP} .

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	Fig. A	N74H106N	
Ceramic DIP	Fig. A	N74H106F	S54H106F
Flatpak	Fig. A		S54H106W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP} Clock input	I_{IH} (mA)		-1.0		
	I_{IL} (mA)		-4.8		
\bar{R}_D Reset input	I_{IH} (μA)		100		
	I_{IL} (mA)		-2.0		
\bar{S}_D Set input	I_{IH} (μA)		100		
	I_{IL} (mA)		-2.0		
JK Data inputs	I_{IH} (μA)		50		
	I_{IL} (mA)		-2.0		
Q & \bar{Q} Outputs	I_{OH} (μA)		-500		
	I_{OL} (mA)		20		

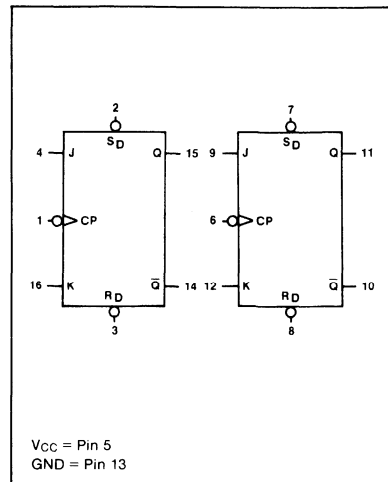
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$I_{IH}(\overline{CP})$ Input HIGH current	$V_{CC} = \text{Max}, V_{CP} = 2.4V$			0	-1.0					mA
I_{CC} Supply current	$V_{CC} = \text{Max}, V_{CP} = 0V$				76					mA

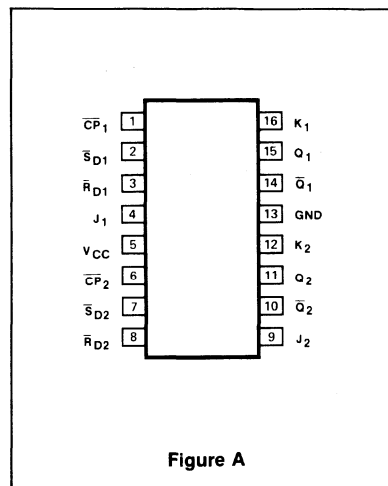
NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

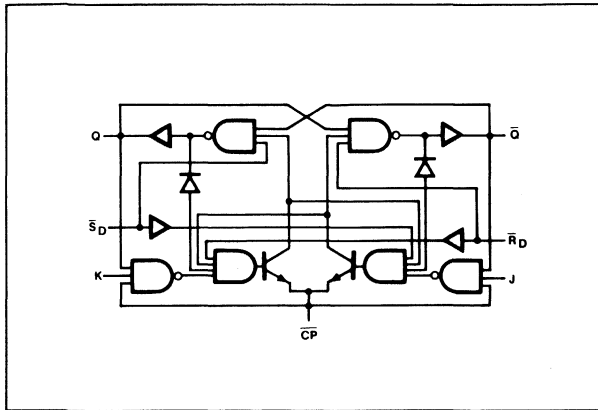
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	\bar{C}_P	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	\bar{q}	q
Load "0" (Reset)	H	H	↓	l	l	L	H
Load "1" (Set)	H	H	↓	h	l	L	L
Hold "no change"	H	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				$C_L = 25\text{ pF}$ $R_L = 280\ \Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency			40						MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Output				15 20					ns ns
t_{PLH}	Propagation delay Set or Reset to Output				12					ns
t_{PHL}		Waveform 5, CP = HIGH			20					ns
t_{PHL}		Waveform 5, CP = LOW			35					ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)			10						ns
$t_{w(L)}$	Clock pulse width (LOW)			15						ns
$t_{w(L)}$	Set or Reset pulse width (LOW)			16						ns
$t_s(H)$	Setup time HIGH J or K to Clock			10						ns
$t_h(H)$	Hold time HIGH J or K to Clock			0						ns
$t_s(L)$	Setup time LOW J or K to Clock			13						ns
$t_h(L)$	Hold time LOW J or K to Clock			0						ns

NOTE

c. Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

54/74107
54LS/74LS107

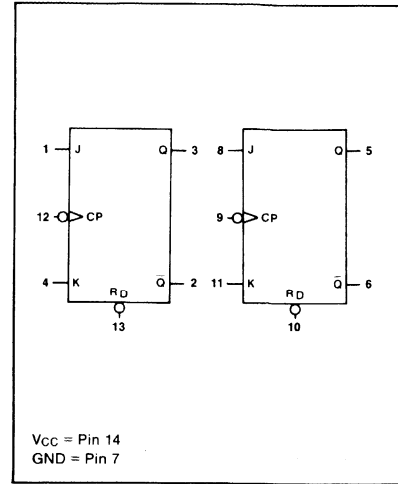
DESCRIPTION

The "107" is a dual Flip-Flop with individual JK, Clock and direct Reset inputs. The 74107 is a positive pulse triggered flip-flop. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. For these devices the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS107 is a negative edge triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset (\bar{R}_D) is an asynchronous active LOW input. When LOW, it overrides the Clock and data inputs forcing the Q output LOW and the \bar{Q} output HIGH.

LOGIC SYMBOL



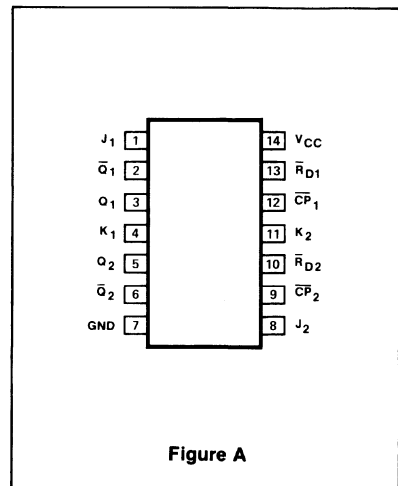
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		V _{CC} = 5V ± 5%; T _A = 0°C to +70°C		V _{CC} = 5V ± 10%; T _A = -55°C to +125°C	
Plastic DIP	Fig. A	N74107N	•	N74LS107N	
Ceramic DIP	Fig. A	N74107F	•	N74LS107F	S54107F • S54LS107F
Flatpak	Fig. A				S54107W • S54LS107W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
$\bar{C}P$	Clock input	I _{IH} (μA) I _{IL} (mA)	80 -3.2			80 -0.8
\bar{R}_D	Reset input	I _{IH} (μA) I _{IL} (mA)	80 -3.2			60 -0.8
JK	Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6			20 -0.4
Q & \bar{Q}	Outputs	I _{OH} (μA) I _{OL} (mA)	-400 16			-400 4/8 (a)

PIN CONFIGURATION



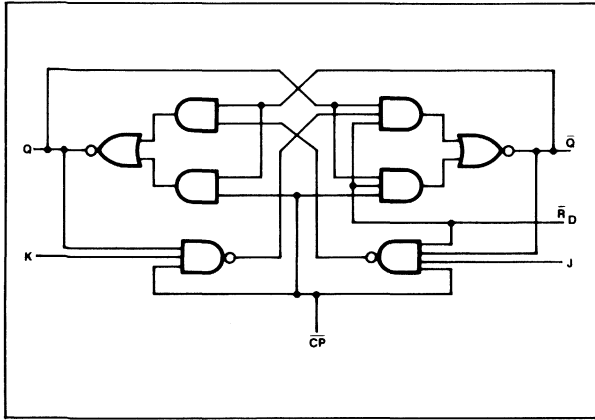
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current		40						8.0	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	R _D	CP(d)	J	K	Q	Q̄
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	⌈⌋	h	h	q̄	q
Load "0" (Reset)	H	⌈⌋	l	h	L	H
Load "1" (Set)	H	⌈⌋	h	l	H	L
Hold "no change"	H	⌈⌋	l	l	q	q̄

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition^(c).
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition^(c).
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to HIGH-to-LOW Clock transition.
 ⌈⌋ = Positive clock pulse.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		C _L = 15 pF R _L = 400 Ω						C _L = 15 pF R _L = 2k Ω		
		Min	Max	Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock frequency	Waveform 4		15					30	MHz
t _{PLH} t _{PHL}	Propagation delay Clock to Output	Waveform 4			25 40				20 30	ns ns
t _{PLH} t _{PHL}	Propagation delay Reset to Output	Waveform 5			25 40				20 30	ns ns

AC SETUP REQUIREMENTS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{w(H)}	Clock pulse width (HIGH)	Waveform 4		20				20		ns
t _{w(L)}	Clock pulse width (LOW)	Waveform 4		47				13		ns
t _{w(L)}	Set or Reset pulse width (LOW)	Waveform 5		25				25		ns
t _s	Setup time J or K to Clock	Waveform 4		(c)				20		ns
t _h	Hold time J or K to Clock	Waveform 4		0				20		ns

NOTES

- c. The J and K inputs of the 54/74107 must be stable while the Clock is HIGH for conventional operation.
- d. The 54LS/74LS107 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.

54H/74H108

DESCRIPTION

The "108" is a Dual JK Negative Edge-Triggered Flip-Flop with individual JK and direct Set inputs, and common Clock and Reset inputs. The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and data inputs forcing the outputs to their steady state level as shown in the Truth Table.

A HIGH level on the Clock (\overline{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the \overline{CP} is HIGH, and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of CP.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74H108N	
Ceramic DIP	Fig. A	N74H108F	S54H108F
Flatpak			

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
\overline{CP} Clock input	I_{IH} (μA)		-1.0		
	I_{IL} (mA)		-9.6		
\bar{R}_D Reset input	I_{IH} (μA)		200		
	I_{IL} (mA)		-4.0		
\bar{S}_D Set input	I_{IH} (μA)		100		
	I_{IL} (mA)		-2.0		
JK Data inputs	I_{IH} (μA)		50		
	I_{IL} (mA)		-2.0		
Q & \bar{Q} Outputs	I_{OH} (μA)		-500		
	I_{OL} (mA)		20		

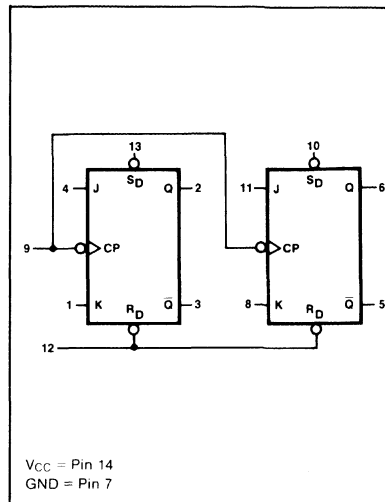
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$I_{IH}(\overline{CP})$ Input HIGH current	$V_{CC} = \text{Max}, V_{CP} = 2.4V$			0	-1.0					mA
I_{CC} Supply current	$V_{CC} = \text{Max}, V_{CP} = 0V$				76					mA

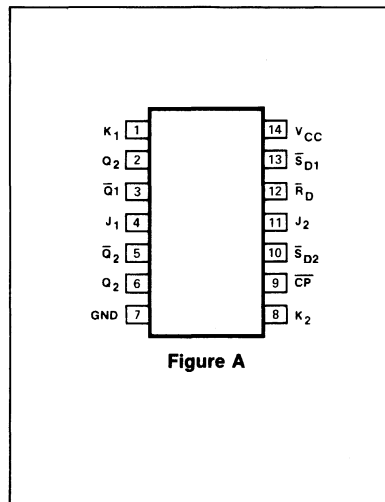
NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

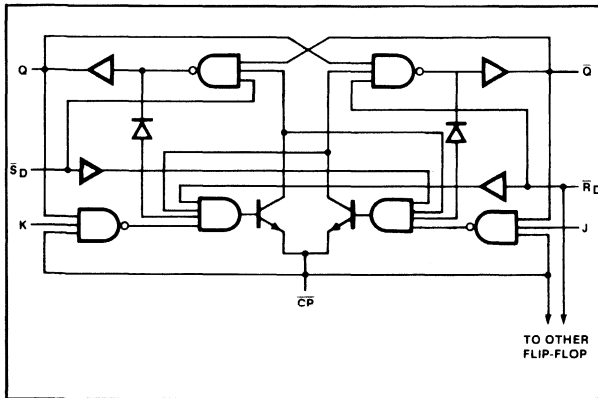
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	\bar{q}	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
				$C_L = 25\text{pF}$ $R_L = 280\Omega$						
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 4			40					MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Output	Waveform 4			15 20					ns ns
t_{PLH}	Propagation delay Set or Reset to Output	Waveform 5			12					ns
t_{PHL}		Waveform 5, CP = HIGH			20					ns
t_{PHL}		Waveform 5, CP = LOW			35					ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)	Waveform 4			10					ns
$t_{w(L)}$	Clock pulse width (LOW)	Waveform 4			15					ns
$t_{w(L)}$	Set or Reset pulse width (LOW)	Waveform 5			16					ns
$t_s(H)$	Setup time HIGH J or K to Clock	Waveform 4			10					ns
$t_h(H)$	Hold time HIGH J or K to Clock	Waveform 4			0					ns
$t_s(L)$	Setup time LOW J or K to Clock	Waveform 4			13					ns
$t_h(L)$	Hold time LOW J or K to Clock	Waveform 4			0					ns

NOTE

c. Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

54/74109
54LS/74LS109

DESCRIPTION

The "109" is a Dual Positive Edge-Triggered JK-Type Flip-Flop featuring individual J, \bar{K} , clock, set and reset inputs; also complementary Q and \bar{Q} outputs.

Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs and operate independently of the clock input.

The J and \bar{K} are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table.

The J and \bar{K} inputs must be stable just one set-up time prior to the LOW-to-HIGH transition of the clock for predictable operation. The JK design allows operation as a D flip-flop by tying the J and \bar{K} inputs together.

Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N74109N	• N74LS109N		
Ceramic DIP	Fig. A	N74109F	• N74LS109F	S54109F	• S54LS109F
Flatpak	Fig. A			S54109W	• S54LS109W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
J, \bar{K}	Data Inputs	I_{IH} (μA)	40			20
		I_{IL} (mA)	-1.6			-0.4
CP	Clock Input	I_{IH} (μA)	80			20
		I_{IL} (mA)	-3.2			-0.4
\bar{S}_D	Set Input	I_{IH} (μA)	80			40
		I_{IL} (mA)	-3.2			-0.8
\bar{R}_D	Reset Input	I_{IH} (μA)	160			40
		I_{IL} (mA)	-4.8			-0.8
Q & \bar{Q}	Outputs	I_{OH} (μA)	-800			-400
		I_{OL} (mA)	16			4/8(a)

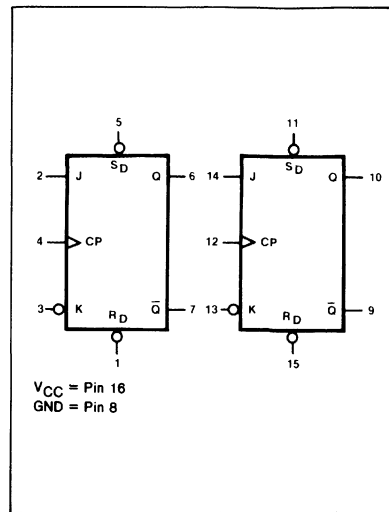
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current	$V_{CC} = \text{Max}, V_{CP} = 0V$			30				8.0	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC SYMBOL



PIN CONFIGURATION

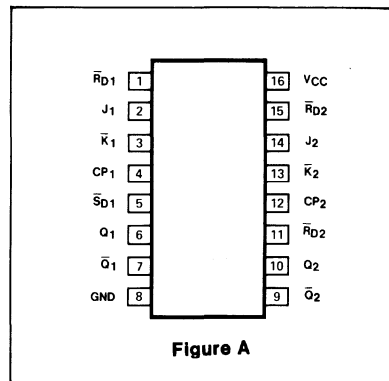
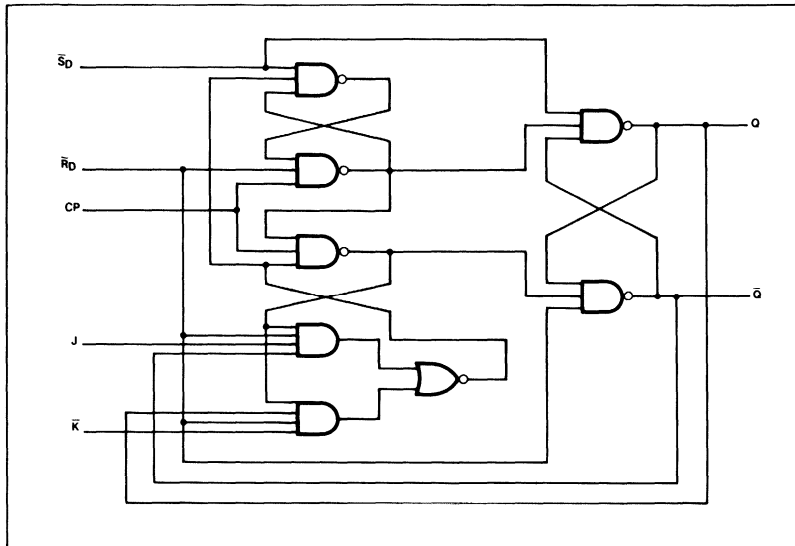


Figure A

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	J	\bar{K}	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	\bar{q}	q
Load "0" (Reset)	H	H	↑	l	h	L	H
Load "1" (Set)	H	H	↑	h	l	H	L
Hold "no change"	H	H	↑	l	h	q	\bar{q}

H = HIGH voltage level steady state
 L = LOW voltage level steady state
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition
 ↑ = LOW-to-HIGH Clock transition

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$						$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 3	25						25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 3		16 18						25 40	ns ns
t_{PLH} Propagation delay t_{PHL} Reset to output	Waveform 5		15 25						25 40	ns ns
t_{PLH} Propagation delay t_{PHL} Set to output	Waveform 5		15 35						25 40	ns ns

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{\text{W(H)}}$ Clock pulse width (HIGH)	Waveform 3	20						25		ns
$t_{\text{W(L)}}$ Clock pulse width (LOW)	Waveform 3	20						15		ns
$t_{\text{W(L)}}$ Set or Reset pulse width (LOW)	Waveform 5	20						25		ns
t_s Setup time J or K to clock	Waveform 3	10						20		ns
t_h Hold time J or K to clock	Waveform 3	6.0						5.0		ns

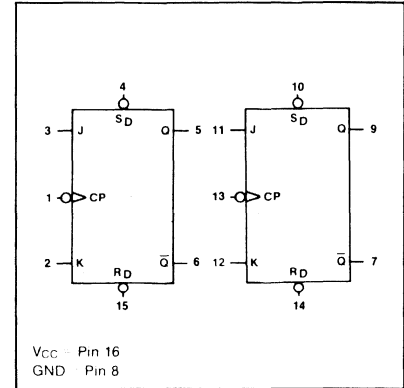
54S/74S112
54LS/74LS112

DESCRIPTION

The "112" is a Dual JK Negative Edge-Triggered Flip-Flop featuring individual J, K, Clock, Set and Reset inputs. The Set (\bar{S}_D) and Reset (\bar{R}_D) inputs, when LOW, set or reset the outputs as shown in the Truth Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\bar{C}P$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\bar{C}P$ is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\bar{C}P$.

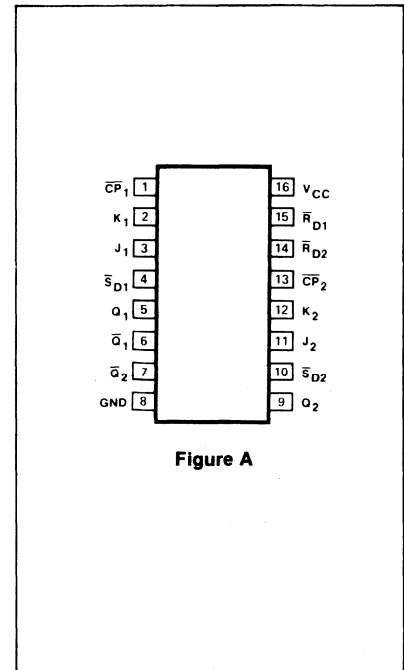
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		V _{CC} = 5V ± 5%; T _A = 0°C to +70°C		V _{CC} = 5V ± 10%; T _A = -55°C to +125°C	
Plastic DIP	Fig. A	N74S112N • N74LS112N			
Ceramic DIP	Fig. A	N74S112F • N74LS112F		S54S112F • S54LS112F	
Flatpak	Fig. A			S54S112W • S54LS112W	

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
$\bar{C}P$	Clock input	I _{IH} (μA) I _{IL} (mA)			100 -4.0	80 -0.8
\bar{R}_D	Reset input	I _{IH} (μA) I _{IL} (mA)			100 -7.0	60 -0.8
\bar{S}_D	Set input	I _{IH} (μA) I _{IL} (mA)			100 -7.0	60 -0.8
JK	Data inputs	I _{IH} (μA) I _{IL} (mA)			50 -1.6	20 -0.4
Q & \bar{Q}	Outputs	I _{OH} (μA) I _{OL} (mA)			-1000 20	-400 4/8 (a)

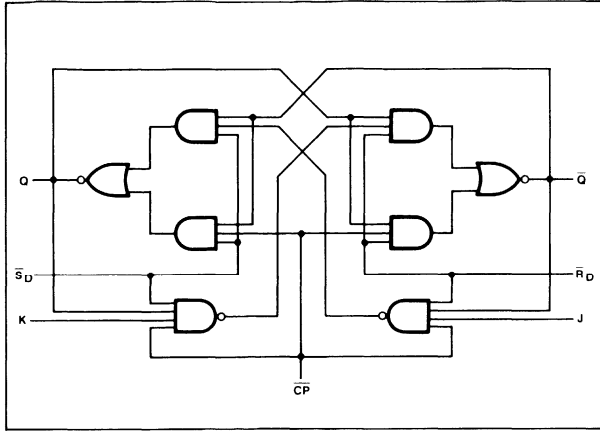
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
I _{CC}	Supply current	V _{CC} = Max, V _{CP} = 0V						50		8.0	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	S _D	R _D	CP	J	K	Q	Q̄
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined ^(c)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	q̄	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	q̄

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
						C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock frequency	Waveform 4				80		30		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to Output	Waveform 4					7.0 7.0		20 30	ns ns
t _{PLH} t _{PHL}	Propagation delay S _D or R _D to Output	Waveform 5					7.0 7.0		20 30	ns ns

AC SETUP REQUIREMENTS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{w(H)}	Clock pulse width (HIGH)	Waveform 4				6.0		20		ns
t _{w(L)}	Clock pulse width (LOW)	Waveform 4				6.5		13		ns
t _{w(L)}	Set or Reset pulse width (LOW)	Waveform 5				8.0		25		ns
t _s	Setup time J or K to Clock	Waveform 4				3.0		20		ns
t _h	Hold time J or K to Clock	Waveform 4				0		0		ns

NOTE

c. Both outputs will be HIGH while both S_D and R_D are LOW, but the output states are unpredictable if S_D and R_D go HIGH simultaneously.

**54S/74S113
54LS/74LS113**

DESCRIPTION

The "113" is a Dual JK Negative Edge-Triggered Flip-Flop featuring individual J, K, Set, and Clock inputs. The asynchronous Set (\bar{S}_D) input, when LOW, forces the outputs to the steady state levels as shown in the Truth Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\bar{C}P$) input en-

ables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\bar{C}P$ is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\bar{C}P$.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74S113N • N74LS113N	
Ceramic DIP	Fig. A	N74S113F • N74LS113F	S54S113F • S54LS113F
Flatpak	Fig. A		S54S113W • S54LS113W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
$\bar{C}P$	Clock input $I_{IH} (\mu A)$ $I_{IL} (mA)$			100 -4.0	80 -0.8
\bar{S}_D	Set input $I_{IH} (\mu A)$ $I_{IL} (mA)$			100 -7.0	60 -0.8
JK	Data inputs $I_{IH} (\mu A)$ $I_{IL} (mA)$			50 -1.6	20 -0.4
Q & \bar{Q}	Outputs $I_{OH} (\mu A)$ $I_{OL} (mA)$			-1000 20	-400 4/8 ^(a)

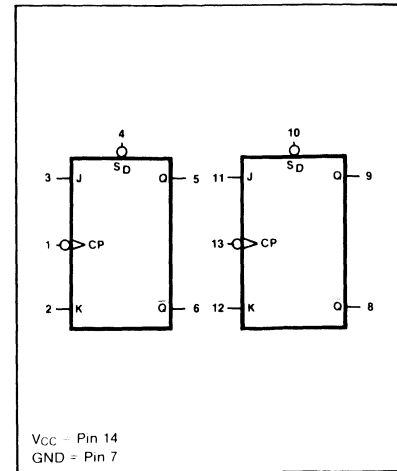
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current	$V_{CC} = \text{Max}, V_{CP} = 0V$					50		8.0	mA

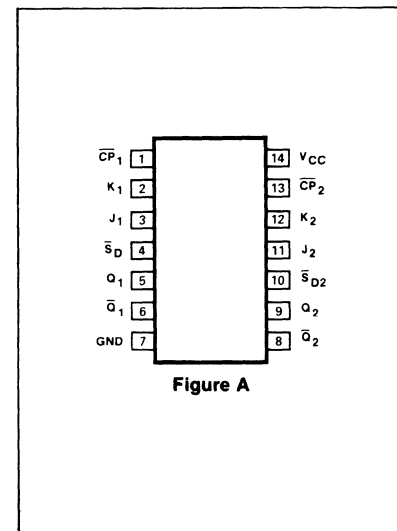
NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

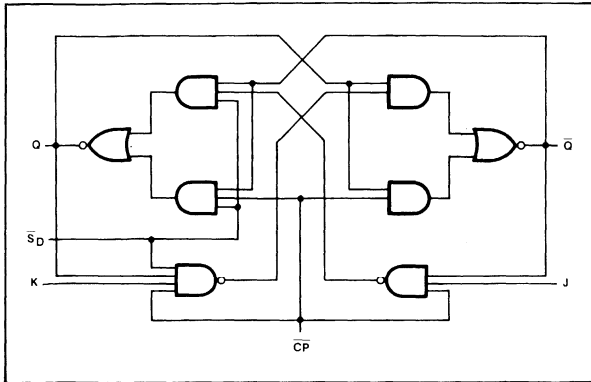
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\bar{CP}	J	K	Q	\bar{Q}
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	\bar{q}	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
						$C_L = 15\text{pF}$ $R_L = 280\Omega$		$C_L = 15\text{pF}$ $R_L = 2k\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency					80		30		MHz
t_{PLH}	Propagation delay						7.0		20	ns
t_{PHL}	Clock to Output						7.0		30	ns
t_{PLH}	Propagation delay						7.0		20	ns
t_{PHL}	Set to Output						7.0		30	ns

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)					6.0		20		ns
$t_{w(L)}$	Clock pulse width (LOW)					6.5		13		ns
$t_{w(L)}$	Set pulse width (LOW)					8.0		25		ns
t_s	Setup time J or K to Clock					3.0		20		ns
t_h	Hold time J or K to Clock					0		0		ns

54S/74S114
54LS/74LS114

DESCRIPTION

The "114" is a Dual JK Negative Edge-Triggered Flip-Flop featuring individual J, K, and Set inputs and common Clock and Reset inputs. The Set (\bar{S}_D) and Reset (\bar{R}_D) inputs, when LOW, set or reset the outputs as shown in the Truth Table regardless of the levels at the other inputs.

A HIGH level on the Clock (\bar{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the CP is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of CP.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N74S114N	• N74LS114N		
Ceramic DIP	Fig. A	N74S114F	• N74LS114F	S54S114F	• S54LS114F
Flatpak	Fig. A			S54S114W	• S54LS114W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
\bar{CP}	Clock input	$I_{IH} (\mu A)$ $I_{IL} (mA)$			200 -8.0	160 -1.44
\bar{R}_D	Reset input	$I_{IH} (\mu A)$ $I_{IL} (mA)$			200 -14.0	120 -1.6
\bar{S}_D	Set input	$I_{IH} (\mu A)$ $I_{IL} (mA)$			100 -7.0	60 -0.8
JK	Data inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$			50 -1.6	20 -0.4
Q & \bar{Q}	Outputs	$I_{OH} (\mu A)$ $I_{OL} (mA)$			-1000 20	-400 4/8 (a)

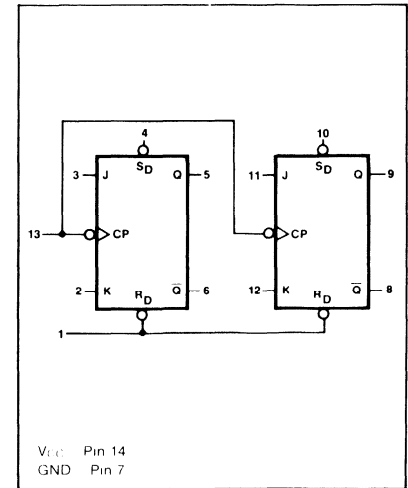
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current						50		8.0	mA

NOTES:

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC SYMBOL



PIN CONFIGURATION

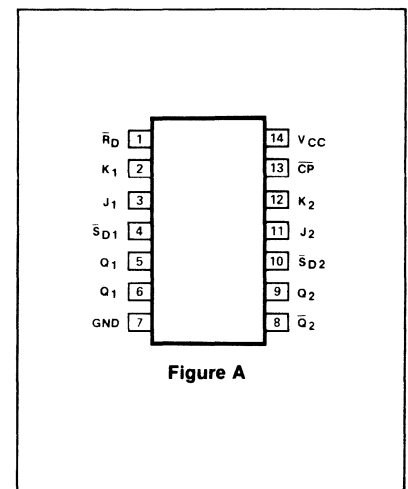
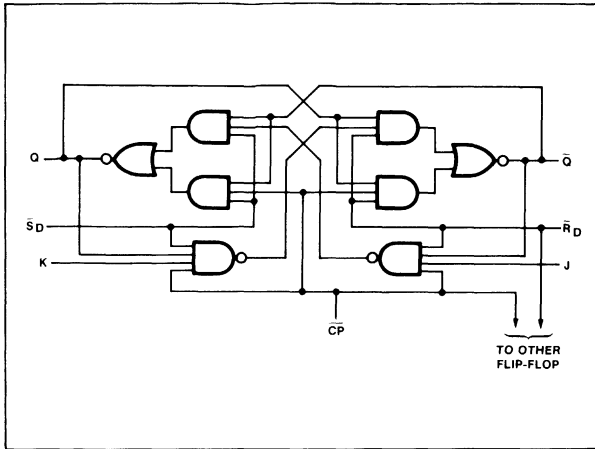


Figure A

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	$\bar{C}P$	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	\bar{q}	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
						$C_L = 15pF$	$C_L = 15pF$			
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency					80		30		MHz
t_{PLH}	Propagation delay						7.0		20	ns
t_{PHL}	Clock to Output						7.0		30	ns
t_{PLH}	Propagation delay						7.0		20	ns
t_{PHL}	\bar{S}_D or \bar{R}_D to Output						7.0		30	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ C$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)					6.0		20		ns
$t_{w(L)}$	Clock pulse width (LOW)					6.5		13		ns
$t_{w(L)}$	Set or Reset pulse width (LOW)					8.0		25		ns
t_s	Setup time J or K to Clock					3.0		20		ns
t_h	Hold time J or K to Clock					0		0		ns

NOTE

c. Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

54/74116

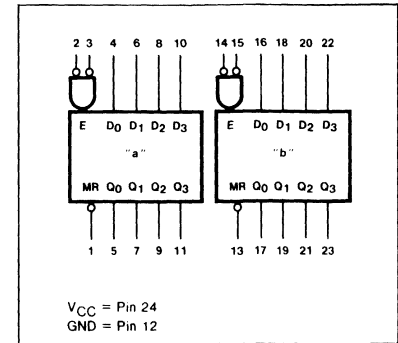
DESCRIPTION

The "116" is a Dual 4-Bit Transparent Latch. Each 4-bit latch has a 2-input enable gate for easy expansion and an asynchronous Master Reset to clear the latch. When both Enable inputs (\bar{E}_0 & \bar{E}_1) are LOW, the data on the D inputs is loaded into the latch and appear at the outputs. A HIGH on either \bar{E}_0 or \bar{E}_1 will latch the data and hold the outputs stable.

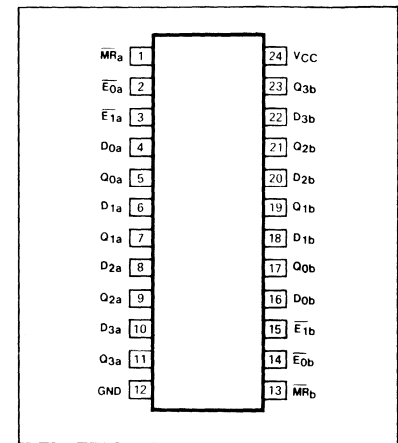
FEATURES

- Two independent 4-bit latches
- 2-Input enable gates for easy expansion
- Asynchronous Master Reset

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74116N	
Ceramic DIP	N74116F	S54116F
Flatpak		S54116W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\bar{E}_0, \bar{E}_1	Enable (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
D_0-D_3	Data inputs	I_{IH} (μA) I_{IL} (mA)	60 -2.4		
\bar{MR}	Master Reset (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
Q_0-Q_3	Latch outputs	I_{OH} (μA) I_{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "116" has two independent 4-bit transparent latches. Each 4-bit latch is controlled by a 2-input active LOW Enable gate (\bar{E}_0 & \bar{E}_1). When both \bar{E}_0 & \bar{E}_1 are LOW, the data enters the latch and appears at the output. The outputs follow the data inputs as long as \bar{E}_0 and \bar{E}_1 are LOW. The data on the D inputs one setup time before the LOW-to-HIGH transition of \bar{E}_0 or \bar{E}_1 will be stored in the latch. The latched outputs remain stable as long as either \bar{E}_0 or \bar{E}_1 is HIGH.

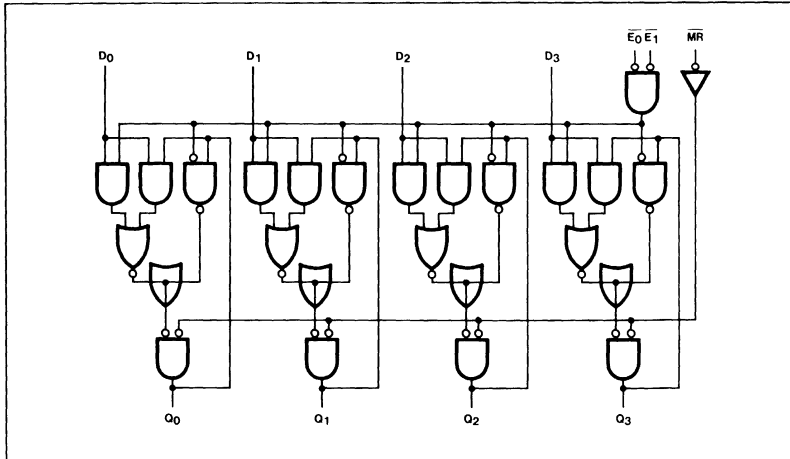
Each 4-bit latch has an active LOW asynchronous Master Reset (\bar{MR}) input. When LOW, the \bar{MR} input overrides the data and enable inputs and sets the four latch outputs LOW.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	\bar{MR}	\bar{E}_0	\bar{E}_1	D_n	Q_n
Reset (clear)	L	X	X	X	L
Enable latch	H	L	L	L	L
	H	L	L	H	H
Latch data	H	↑	L	l	L
	H	L	↑	h	H

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Enable transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Enable transition
 X = Don't care
 ↑ = LOW-to-HIGH Enable transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$, All inputs = 0V		100					mA
	$V_{CC} = \text{Max}$, $V_{\bar{E}} = 0V$		70					mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

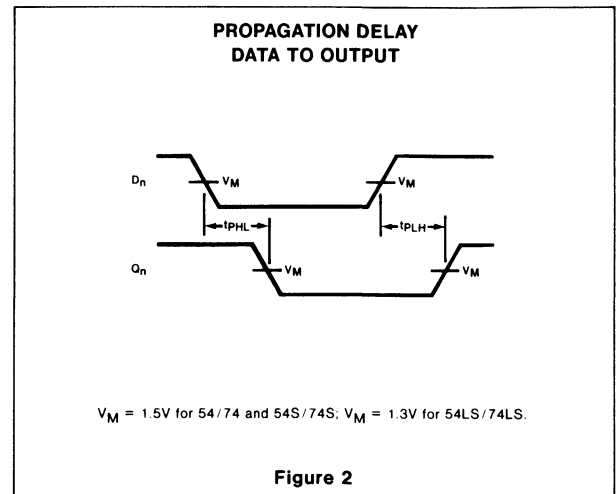
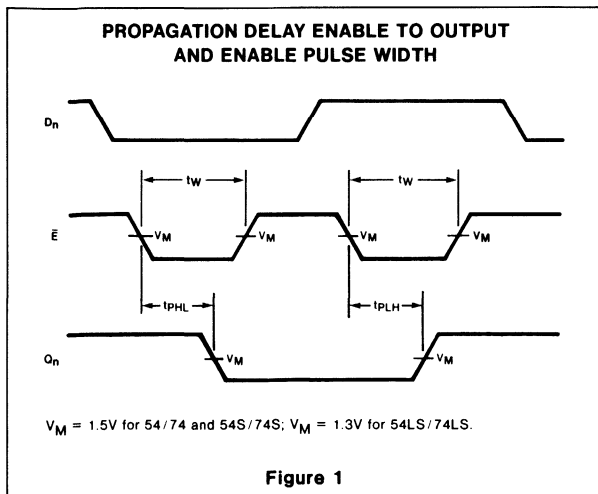
AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output		30 22					ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output		15 18					ns ns
t_{PHL}	Propagation delay \overline{MR} to output		22					ns

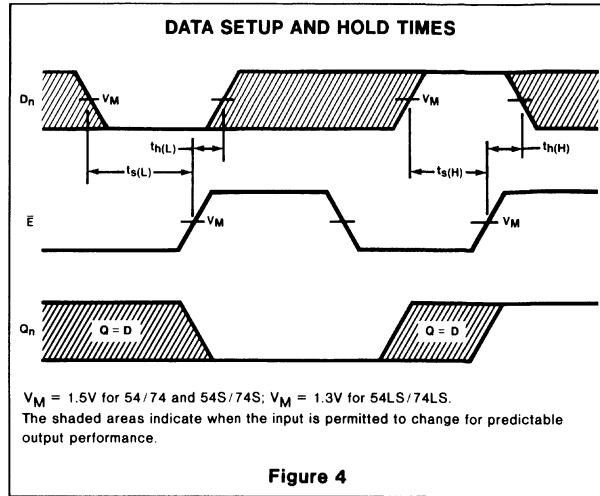
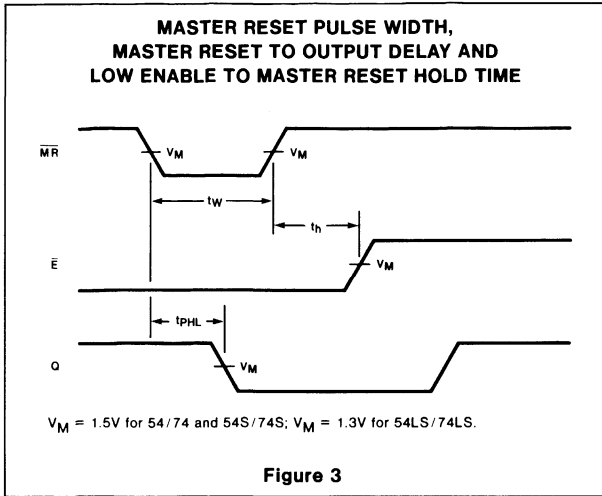
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W	Enable pulse width	18						ns
t_W	Master Reset pulse width	18						ns
$t_S(H)$	Setup time HIGH Data to Enable	8.0						ns
$t_H(H)$	Hold time HIGH Data to Enable		-2.0					ns
$t_S(L)$	Setup time LOW Data to Enable	14.0						ns
$t_H(L)$	Hold time LOW Data to Enable	8.0						ns
$t_H(L)$	Hold time LOW Enable to Master Reset to load HIGH	8.0						ns

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



54/74121

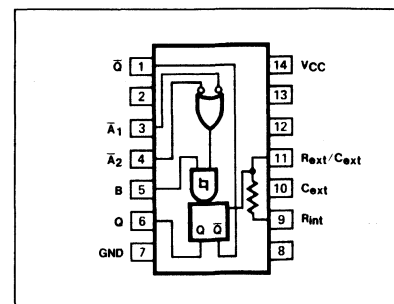
DESCRIPTION

The "121" is a Monostable Multivibrator with an active HIGH going schmitt trigger input and two gated active LOW going trigger inputs. The device is non-retriggerable and will not react to input transitions while timing out. The "121" features good pulse width stability and accuracy, and good immunity to temperature and voltage variations.

FEATURES

- Very good pulse width stability
- Virtually immune to temperature and voltage variations
- Schmitt trigger input for slow input transitions
- Internal timing resistor provided

PIN CONFIGURATION



FUNCTION TABLE

INPUTS			OUTPUTS	
\bar{A}_1	\bar{A}_2	B	Q	\bar{Q}
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎓	⎓
↓	H	H	⎓	⎓
↓	↓	H	⎓	⎓
L	X	↑	⎓	⎓
X	L	↑	⎓	⎓

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH transition
 ↓ = HIGH-to-LOW transition

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74121N	
Ceramic DIP	N74121F	S54121F
Flatpak		S54121W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\bar{A}_1, \bar{A}_2	Trigger (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
B	Trigger (active HIGH) input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		
Q	Pulse (active HIGH) output	I_{OH} (μA) I_{OL} (mA)	-400 16		
\bar{Q}	Pulse (active LOW) output	I_{OH} (μA) I_{OL} (mA)	-400 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

These multivibrators feature dual active LOW going edge inputs and a single active HIGH going edge input which can be used as an active HIGH enable input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the

inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 20 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

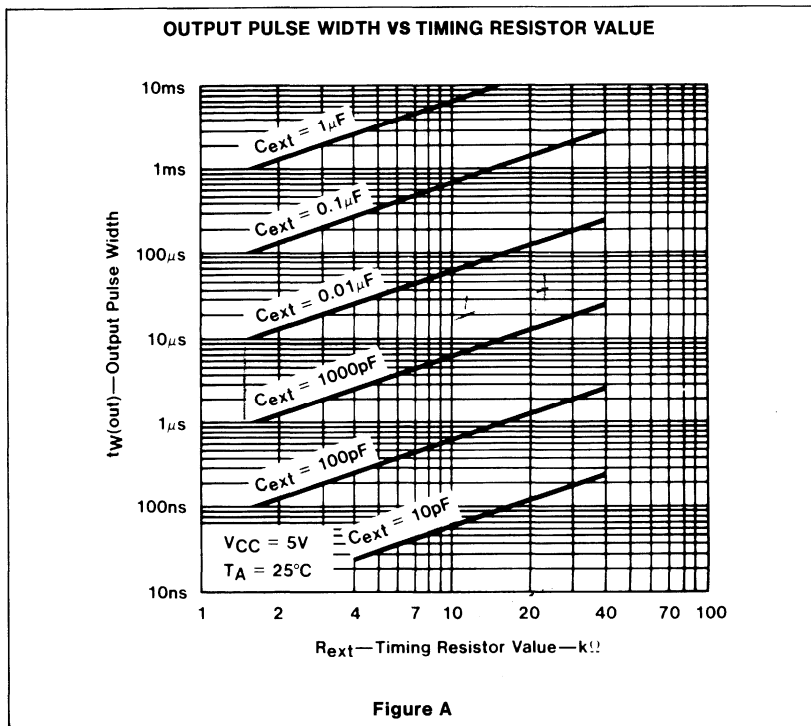
ponents.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 30kΩ for the 54121 and 2kΩ to 40kΩ for the 74121). Throughout these ranges, pulse width is defined by the relationship: (See Figure A)

$$t_{W(out)} = C_{ext}R_{ext} \ln 2$$

$$t_{W(out)} \approx 0.7C_{ext}R_{ext}$$

In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4kΩ may be used.



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply Current	V _{CC} = Max	Quiescent		25				mA
		Triggered		40				mA

NOTE
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

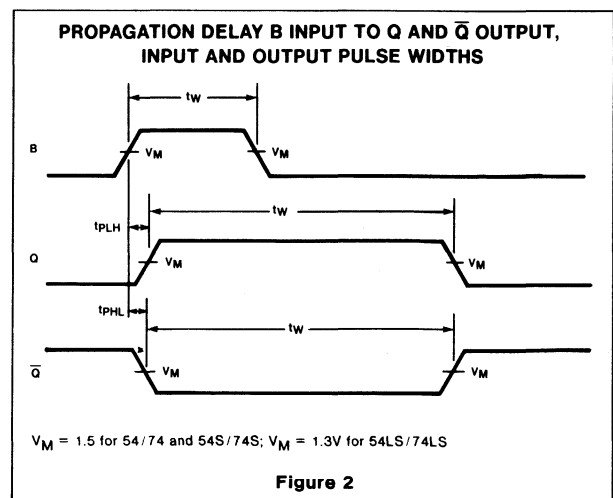
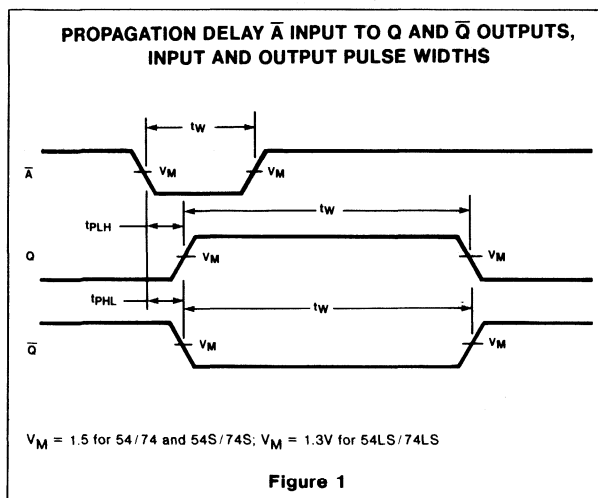
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay \bar{A} input to Q & \bar{Q} output	Figure 1 $C_{ext} = 80\text{pF}, R_{int}$ to V_{CC}		70 80				ns ns
t_{PLH} t_{PHL}	Propagation delay B input to Q & \bar{Q} output	Figure 2 $C_{ext} = 80\text{pF}, R_{int}$ to V_{CC}		55 65				ns ns
t_w	Minimum output pulse width	$C_{ext} = 0\text{pF}, R_{int}$ to V_{CC}		20	50			ns
t_w	Output pulse width	$C_{ext} = 80\text{pF}, R_{int}$ to V_{CC}		70	150			ns
		$C_{ext} = 100\text{pF}, R_{ext} = 10\text{k}\Omega$		600	800			ns
		$C_{ext} = 1\mu\text{F}, R_{ext} = 10\text{k}\Omega$		6.0	8.0			ms

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w	Minimum input pulse width to trigger	Figures 1 & 2		50				ns
R_{ext}	External timing resistor range	Mil		1.4	30			k Ω
		Com		1.4	40			k Ω
C_{ext}	External timing capacitance range			0	1000			pF
Output duty cycle	$R_{ext} = 2\text{k}\Omega$			67				%
	$R_{ext} = R_{ext}(\text{Max})$			90				%

AC WAVEFORMS



54/74122

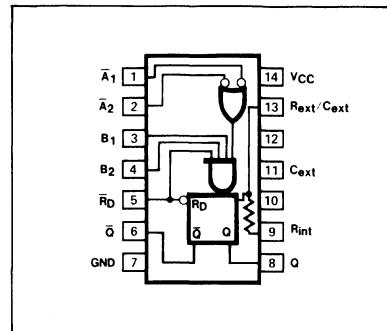
DESCRIPTION

These retriggerable monostable multi-vibrators feature dc triggering from gated active LOW inputs (\bar{A}) and active HIGH inputs (B) and also provide overriding direct reset inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding reset capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

FEATURES

- DC Triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses—up to 100% duty cycle
- Direct Reset terminates output pulse
- Compensated for V_{CC} and temperature variations

PIN CONFIGURATION



FUNCTION TABLE

INPUTS					OUTPUTS	
\bar{R}_D	\bar{A}_1	\bar{A}_2	B ₁	B ₂	Q	\bar{Q}
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	[Active HIGH pulse]	[Active LOW pulse]
H	L	X	H	↑	[Active HIGH pulse]	[Active LOW pulse]
H	X	L	↑	H	[Active HIGH pulse]	[Active LOW pulse]
H	X	L	H	↑	[Active HIGH pulse]	[Active LOW pulse]
H	H	↓	H	H	[Active HIGH pulse]	[Active LOW pulse]
H	↓	↓	H	H	[Active HIGH pulse]	[Active LOW pulse]
H	↓	H	H	H	[Active HIGH pulse]	[Active LOW pulse]
↑	L	X	H	H	[Active HIGH pulse]	[Active LOW pulse]
↑	X	L	H	H	[Active HIGH pulse]	[Active LOW pulse]

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH input transition
 ↓ = HIGH-to-LOW input transition
 [Active HIGH pulse] = Active HIGH pulse
 [Active LOW pulse] = Active LOW pulse

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74122N	
Ceramic DIP	B74122F	S54122F
Flatpak		S54122W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\bar{A}_1, \bar{A}_2	Trigger (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
B ₁ , B ₂	Trigger (active HIGH) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
\bar{R}_D	Direct Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		
Q	Pulse (active HIGH) output	I_{OH} (μA) I_{OL} (mA)	-800 16		
\bar{Q}	Pulse (active LOW) output	I_{OH} (μA) I_{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "122" is a retriggerable monostable multivibrator featuring output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data in "123" data sheet). The "122" has an internal timing resistor that allows the circuit to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated active LOW going edge inputs (\bar{A}_1 , \bar{A}_2) or the active HIGH going edge inputs (B_1 , B_2), or be reduced by use of the overriding active LOW Reset.

To use the internal timing resistor of the "122" connect R_{int} to V_{CC} . For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} left open. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC} .

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$	-10	-40					mA
I_{CC} Supply current	$V_{CC} = \text{Max}$		28					mA

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} \bar{A} input to Q & \bar{Q} output	Figure 1 $C_{ext} = 0\text{pF}, R_{ext} = 5\text{k}\Omega$		33 40					ns ns
t_{PLH} Propagation delay B t_{PHL} input to Q & \bar{Q} output	Figure 2 $C_{ext} = 0\text{pF}, R_{ext} = 5\text{k}\Omega$		28 36					ns ns
t_{PLH} Propagation delay \bar{R}_D t_{PHL} input to \bar{Q} & Q output	Figure 3 $C_{ext} = 0\text{pF}, R_{ext} = 5\text{k}\Omega$		40 27					ns ns
t_{WQ} Minimum Q pulse width	Figures 1 & 2 $C_{ext} = 0\text{pF}, R_{ext} = 5\text{k}\Omega$		65					ns
t_{WQ} Output pulse width	Figures 1 & 2 $C_{ext} = 1000\text{pF}, R_{ext} = 10\text{k}\Omega$	3.08	3.76					μs

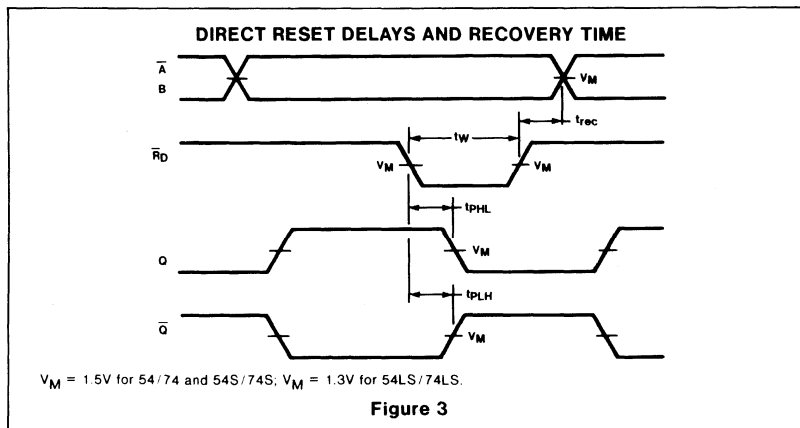
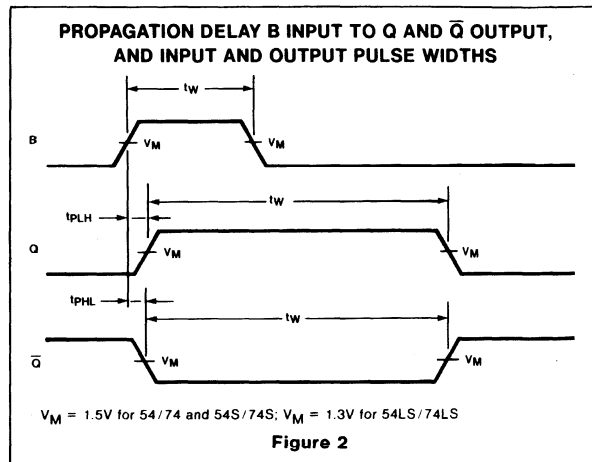
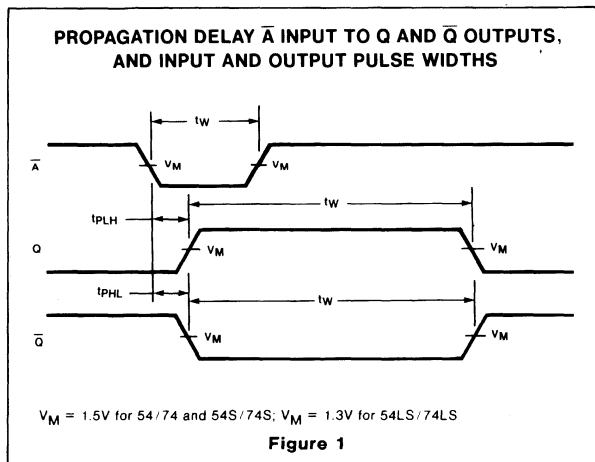
NOTES

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w	Minimum input pulse width to trigger	40						ns
R_{ext}	External timing resistor range	Mil	5.0	25				$k\Omega$
		Com	5.0	50				$k\Omega$
C_{ext}	External timing capacitance range		NO RESTRICTION					μF
$C_{Rx/Cx}$	Stray capacitance to GND at R_{ext}/C_{ext} terminal		50					μF

AC WAVEFORMS



54/74123
54LS/74LS123A (Preliminary data)

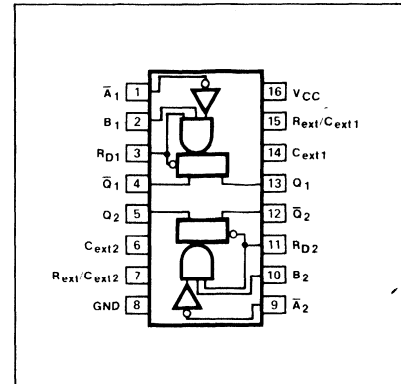
DESCRIPTION

These retriggerable monostable multivibrators feature dc triggering from gated active LOW inputs (\bar{A}) and active HIGH inputs (B) and also provide overriding direct reset inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding reset capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

FEATURES

- DC Triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses - up to 100% duty cycle
- Direct Reset terminates output pulse
- Compensated for V_{CC} and temperature variations

PIN CONFIGURATIONS



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	N74123N	• N74LS123AN		
Ceramic DIP	N74123F	• N74LS123AF	S54123F	• S54LS123AF
Flatpak			S54123W	• S54LS123AW

FUNCTION TABLE

INPUTS			OUTPUTS	
\bar{R}_D	\bar{A}	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎓	⎓
H	↓	H	⎓	⎓
↑	L	H	⎓	⎓

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\bar{A}	Trigger (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
B	Trigger (active HIGH) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
\bar{R}_D	Direct Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		20 -0.4
Q	Pulse (active HIGH) output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)
\bar{Q}	Pulse (active LOW) output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "123" is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance (R_{ext}) and capacitance (C_{ext}) values. Once triggered, the basic pulse width may be extended by retriggering the gated active LOW going edge input (\bar{A}) or the active HIGH going edge input (B), or be reduced by use of the overriding active LOW reset.

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000pF$ see Figure A for the 54/74123 and Figure B for the 54LS/74LS123.

When $C_{ext} > 1000pF$, the output pulse width is defined as:

54/74123: $t_W = 0.28 R_{ext} C_{ext} (1 + \frac{0.7}{R_{ext}})$

CY323 & 54/74122: $t_W = 0.32 R_{ext} C_{ext} (1 + \frac{0.7}{R_{ext}})$

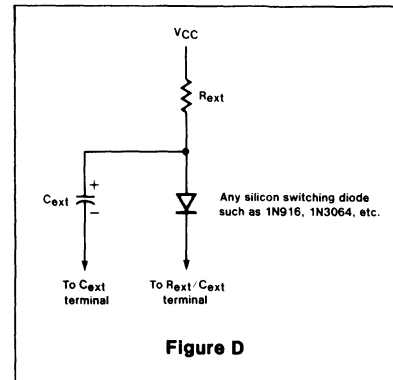
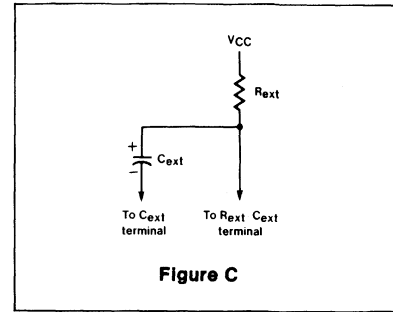
54LS/74LS123: $t_W = 0.45 R_{ext} C_{ext}$

The external resistance and capacitance are normally connected as shown in Figure C. If an electrolytic capacitor is to be used with an inverse voltage rating of less than 1V then Figure D should be used. (Inverse voltage rating of an electrolytic is normally specified at 5% of the forward voltage rating). If the inverse voltage rating is 1V or more (this includes a 100% safety margin) then Figure C can be used. Note that if Figure D is used the timing equations change as follows:

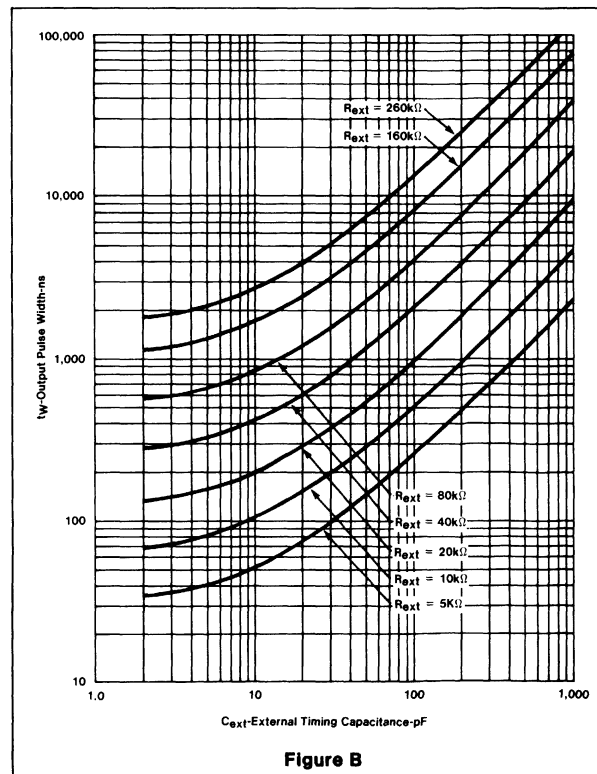
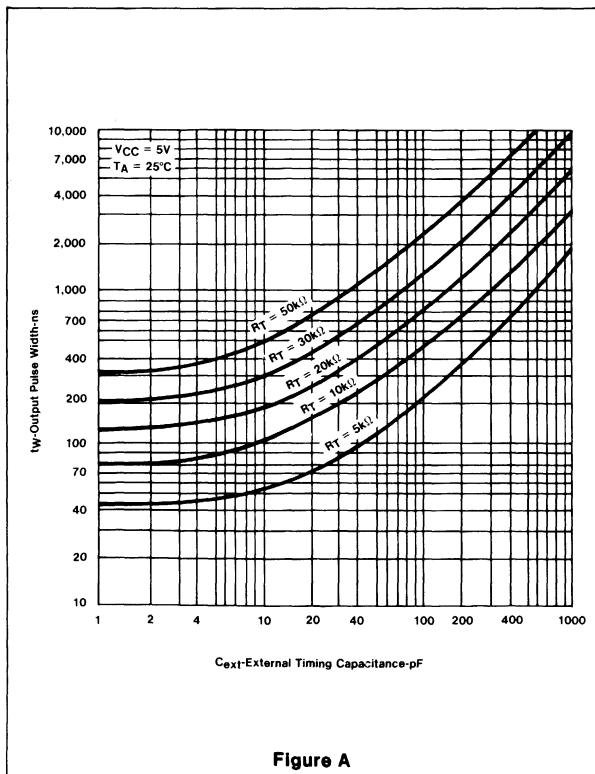
54/74123: $t_W \approx 0.25 R_{ext} C_{ext} (1 + \frac{0.7}{R_{ext}})$

CY323 & 54/74122: $t_W \approx 0.28 R_{ext} C_{ext} (1 + \frac{0.7}{R_{ext}})$

54LS/74LS123: $t_W \approx 0.4 R_{ext} C_{ext}$



TYPICAL PERFORMANCE CHARACTERISTICS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{OS} Output short circuit current	V _{CC} = Max.	-10	-40			-15	-100	mA
I _{CC} Supply current	V _{CC} = Max.		66				20	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2KΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} \bar{A} input to Q & \bar{Q} output	Figure 1 C _{ext} = 0pF, R _{ext} = 5kΩ		33 40				33 45	ns ns
t _{PLH} Propagation delay B t _{PHL} input to Q & \bar{Q} output	Figure 2 C _{ext} = 0pF, R _{ext} = 5kΩ		28 36				44 56	ns ns
t _{PLH} Propagation delay \bar{R}_D t _{PHL} input to \bar{Q} & Q output	Figure 3 C _{ext} = 0pF, R _{ext} = 5kΩ		40 27				45 27	ns ns
t _W Q Minimum Q pulse width	Figures 1 & 2 C _{ext} = 0pF, R _{ext} = 5kΩ		65				65	ns
t _W Q Output pulse width	Figures 1 & 2 C _{ext} = 1000pF, R _{ext} = 10kΩ	2.76	3.37			4.0	5.0	μs
t _W Q Output pulse width (Option available as CY323 only)	Figures 1 & 2 C _{ext} = 1000pF, R _{ext} = 10kΩ	3.08	3.76					μs

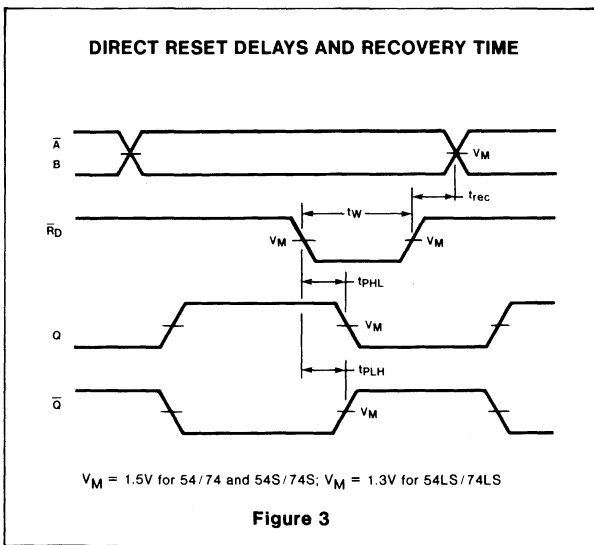
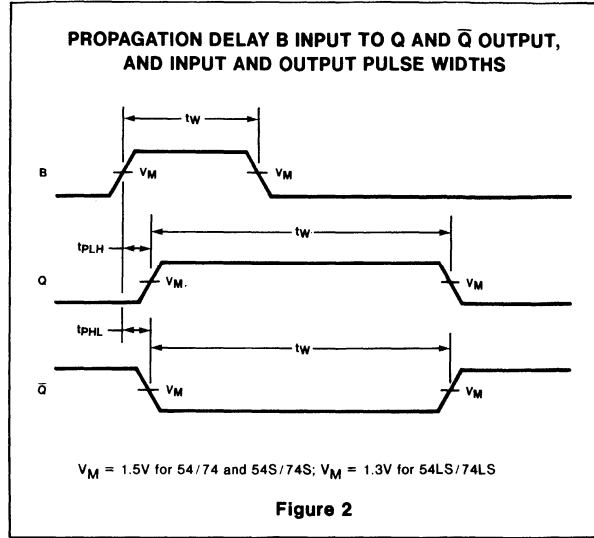
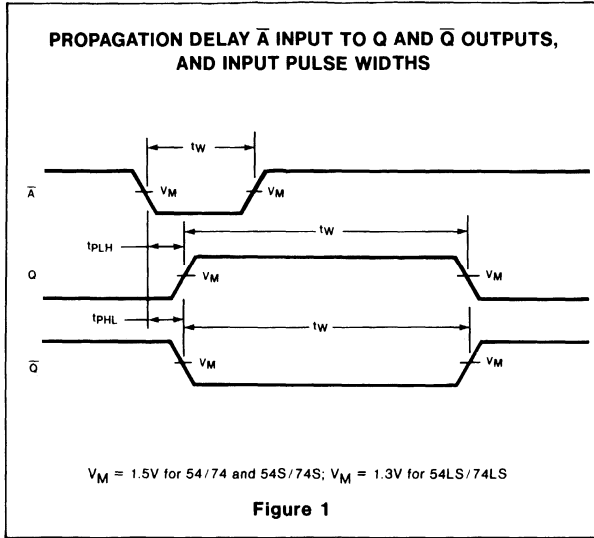
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _W Minimum input pulse width to trigger	Figures 1 & 2	40				40		ns
R _{ext} External timing resistor range	Mil	5.0	25			5.0	180	kΩ
	Com	5.0	50			5.0	260	kΩ
C _{ext} External timing capacitance range				NO RESTRICTION				pF
C _{Rx} /C _x Stray capacitance to GND at R _{ext} /C _{ext} terminal			50				50	pF

NOTE

b. For dc family characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



**54/74125
54LS/74LS125**

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N74125N	• N74LS125N		
Ceramic DIP	Fig. A	N74125F	• N74LS125F	S54125F	• S54LS125F
Flatpak	Fig. A			S54125W	• S54LS125W

PIN CONFIGURATION

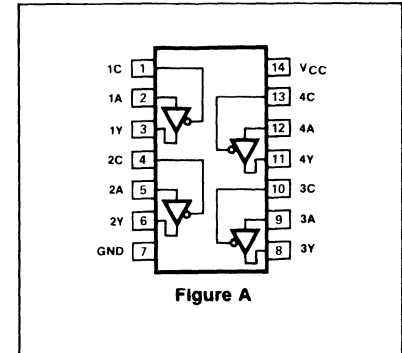


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.4
Outputs	I_{OH} (μA)	-2.0/-5.2 ^(a)			-1.0/-2.6 ^(a)
	I_{OL} (mA)	16			12/24 ^(a)

TRUTH TABLE

INPUTS		OUTPUT
C	A	Y
L	L	L
L	H	H
H	X	(Z)

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = High impedance (off)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$		0.4							V	
	$V_{IN} = V_{IL}$	$I_{OL} = 16\text{mA}$									
		$I_{OL} = 24\text{mA}$							0.4		V
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{See above table}$ $V_{INC} = V_{IL}$, $V_{INA} = 2.0V$		2.4					2.4		V	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$ $V_{OUT} = 0V$	Mil	-30	-70					-30	-100	mA
		Com	-28	-70					-30	-100	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}$ $V_{INA} = 0V$								16	mA	
I_{CCZ} Supply current	$V_{INA} = 0V$ $V_{INC} = 4.5V$		54						20	mA	

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 50\text{pF}$ $R_L = 400\Omega$						$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 2		13						18	ns
t_{PHL} Propagation delay	Waveform 2		18						15	ns
t_{pZH} Enable to HIGH	Waveform 6		18						20	ns
t_{pZL} Enable to LOW	Waveform 7		25						20	ns
t_{PHZ} Disable from HIGH	Waveform 6 (d)		8.0						18	ns
t_{PLZ} Disable from LOW	Waveform 7 (d)		12						18	ns

NOTES

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see

inside back cover for 54S/74S and 54LS/74LS specification.
c. This parameter for Commercial range only.
d. $C_L = 5\text{pF}$ for these tests.

**54/74126
54LS/74LS126**

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$	
Plastic DIP	Fig. A	N74126N	• N74LS126N		
Ceramic DIP	Fig. A	N74126F	• N74LS126F	S54126F	• S54LS126F
Flatpak	Fig. A			S54126W	• S54LS126W

PIN CONFIGURATION

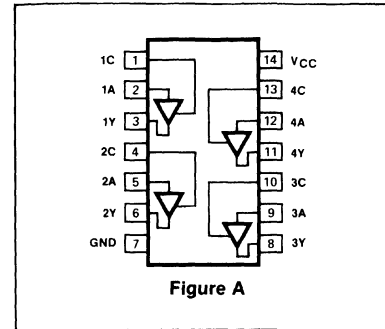


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.4
Outputs	I_{OH} (μA)	-2/-5.2 ^(a)			-1/-2.6 ^(a)
	I_{OL} (mA)	16			12/24 ^(a)

TRUTH TABLE

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = High impedance (off)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
VOL	Output LOW voltage $V_{CC} = \text{Min}$ $V_{INC} = 2.0V$, $V_{INA} = V_{IL}$	$I_{OL} = 16mA$		0.4						V
		$I_{OL} = 12mA$						0.4		V
		$I_{OL} = 24mA$						0.5 ^(c)		V
VOH	Output HIGH voltage $V_{CC} = \text{Min}$, $I_{OH} = \text{See above Table}$ $V_C = V_A = 2.0V$, $V_{INC} = V_{INA}$	2.4						2.4		V
Ios	Output Short circuit current $V_{CC} = \text{Max}$, $V_{OUT} = 0V$	Mil	-30	-70				-30	-100	mA
		Com	-28	-70				-30	-100	mA
IccL	Supply current $V_{CC} = \text{Max}$, $V_{INC} = 4.5V$		62						20	mA
IccZ	Supply current $V_{INA} = 0V$, $V_{INC} = 0V$		62						22	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 50pF$ $R_L = 400\Omega$						$C_L = 45pF$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation delay		13						18	ns
t _{PHL}	Data to output		18						15	ns
t _{PZH}	Enable to HIGH		18						25	ns
t _{PZL}	Enable to LOW		25						25	ns
t _{PHZ}	Disable from HIGH		16						18	ns
t _{PLZ}	Disable from LOW		18						18	ns

NOTES

a. The slashed numbers indicate different parametric values for Military Commercial temperature ranges respectively.
b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see

inside back cover for 54S/74S and 54LS/74LS specification.
c. This parameter for Commercial range only.
d. $C_L = 5pF$ for these tests.

54/74128

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74128N	
Ceramic DIP	Fig. A	N74128F	S54128F
Flatpak	Fig. A		S54128W

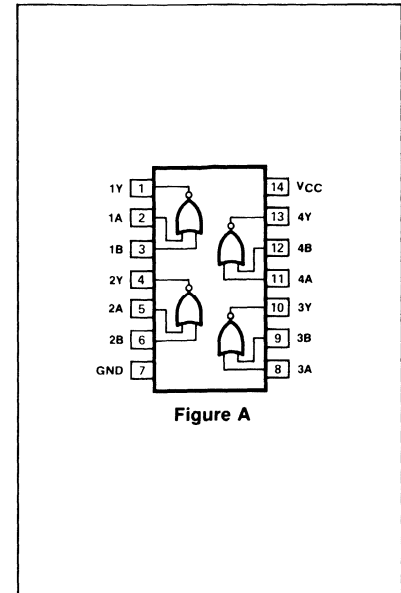


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			
	I_{IL} (mA)	-1.6			
Outputs	I_{OH} (μA)	-2400			
	I_{OL} (mA)	48			

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}, V_{IN} = 0.8V, I_{OL} = 2.4mA$	2.4								V	
	$V_{CC} = \text{Min}, V_{IN} = 0.4V, I_{OL} = -13.2mA$	2.4								V	
	$V_{CC} = \text{Min}, V_{IN} = 0.4V,$	$I_{OL} = -29mA$ Mil	2.0								V
		$I_{OL} = -42.4mA$ Com	2.0								V
I_{OS} Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$	-70	-180							mA	
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$		21							mA	
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} = 5V$		57							mA	

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$R_L = 133\Omega$								
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		9 ^(c)							ns
t_{PHL} Propagation delay	Waveform 1		12 ^(c)							ns
t_{PLH} Propagation delay	Waveform 1		15 ^(c)							ns
t_{PHL} Propagation delay	Waveform 1		18 ^(c)							ns

NOTES

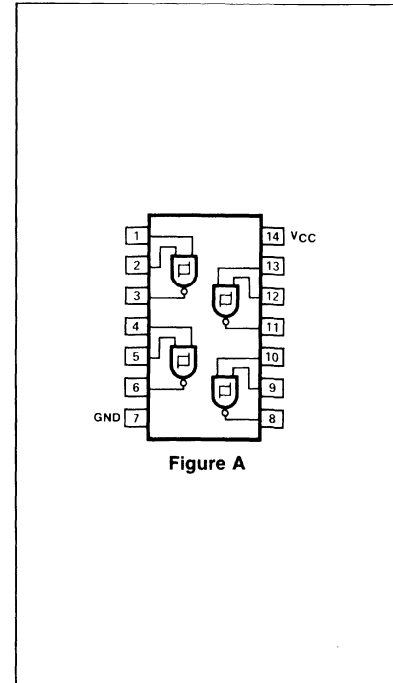
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. $C_L = 50pF$ for Max. 9 and 12; $C_L = 150pF$ for Max. 15 and 18.

**54/74132
54LS/74LS132**

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74132N • N74LS132N	
Ceramic DIP	Fig. A	N74132F • N74LS132F	S54132F • S54LS132F
Flatpak	Fig. A		S54132W • S54LS132W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.2			-0.4
Outputs	I_{OH} (μA)	-800			-400
	I_{OL} (mA)	16			4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive going threshold	$V_{CC} = 5V$						1.5	2.0	V
V_{T-}	Negative going threshold	$V_{CC} = 5V$						0.6	1.1	V
ΔV_T	Hysteresis	$V_{CC} = 5V$						0.4		V
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$							11	mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$							14	mA

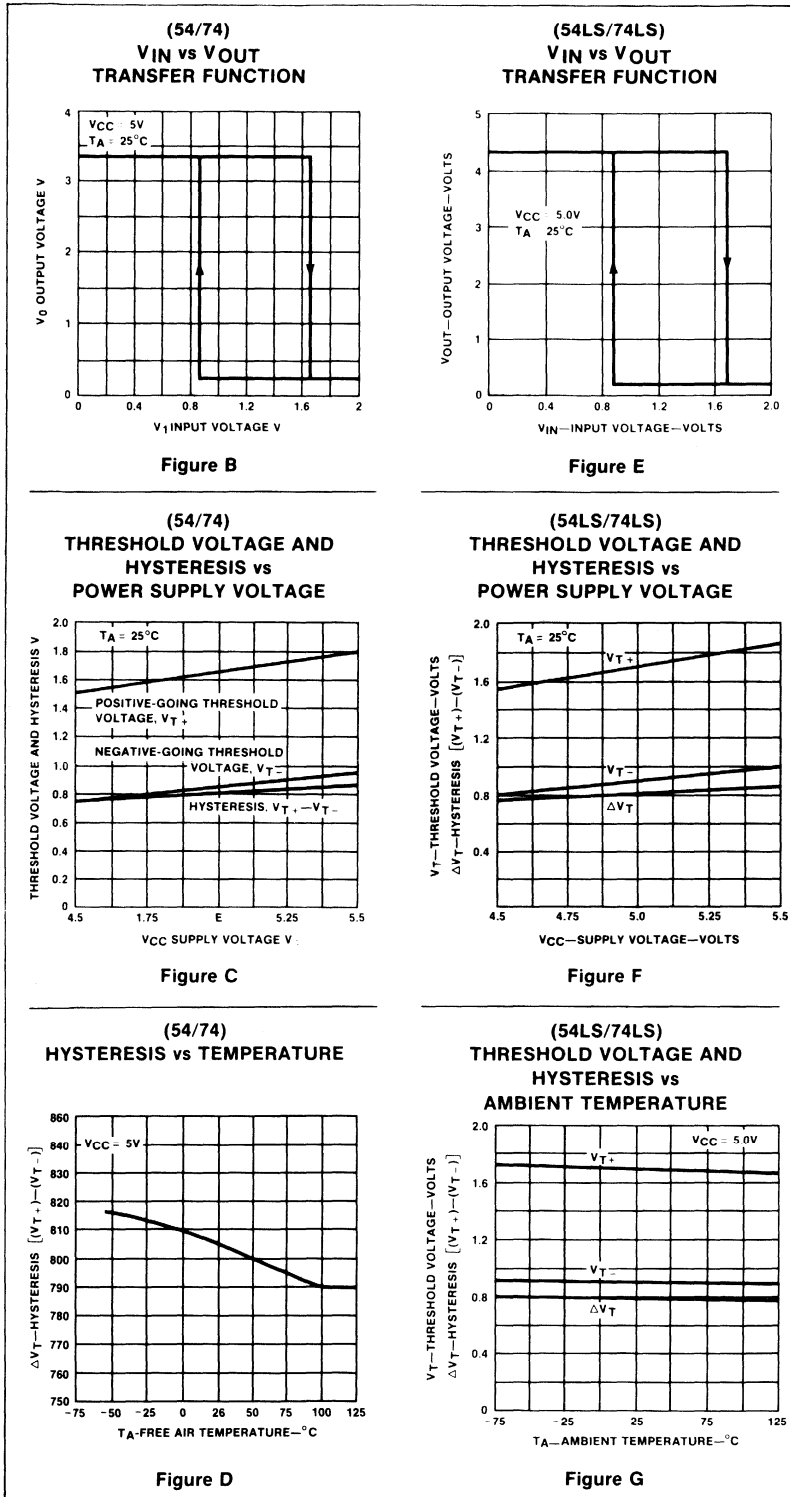
AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$						$C_L = 15pF$ $R_L = 2k\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay		22						22	ns
t_{PHL}			22						22	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

TYPICAL CHARACTERISTICS



FUNCTIONAL DESCRIPTION

The "132" contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined jitter-free output signals. In addition they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+} (Max), the gate will respond to the transitions of the other input as shown in Figure H.

AC WAVEFORMS

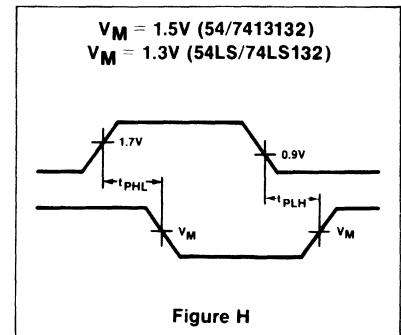


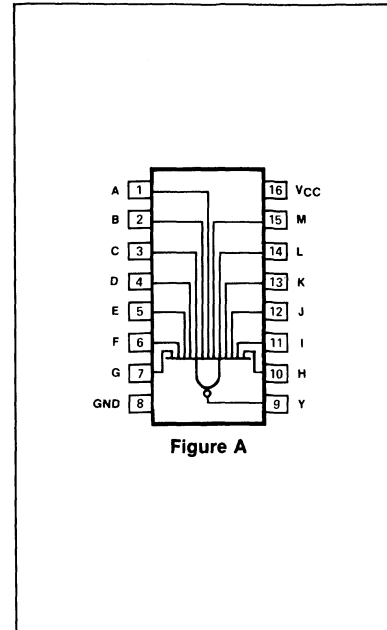
Figure H

54S/74S133

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	Fig. A	N74S133N	
Ceramic DIP	Fig. A	N74S133F	S54S133F
Flatpak	Fig. A		S54S133W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)			50	
	I_{IL} (mA)			-2.0	
Outputs	I_{OH} (μA)			-1000	
	I_{OL} (mA)			20	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$					5.0			mA
I_{CCL}	Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$					10			mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
						$C_L = 15pF$ $R_L = 280\Omega$				
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1					6.0			ns
t_{PHL}	Propagation delay	Waveform 1					7.0			ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54S/74S134

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74S134N	
Ceramic DIP	Fig. A	N74S134F	S54S134F
Flatpak	Fig. A		S54S134W

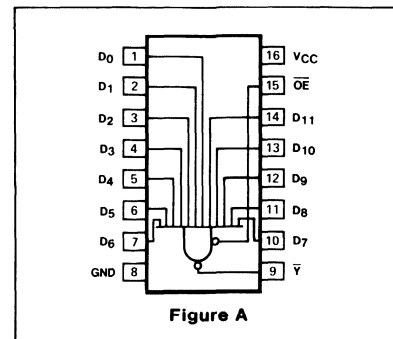


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)			50	
	I_{IL} (mA)			-2.0	
Outputs	I_{OH} (μA)			-2/-6.5(a)	
	I_{OL} (mA)			20	

TRUTH TABLE

INPUTS		OUTPUT
D_0 - - - - D_{11}	\overline{OE}	\overline{Y}
H - - - - H	L	L
one input = L	L	H
X - - - - X	H	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance "off" state

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}$, $V_{IN} = 0.8V$ $I_{OH} = \text{See Fan-Out Table}$					2.4				V
I_{CCH} Supply current	$V_{CC} = \text{Max}$	Outputs HIGH					13			mA
I_{CCL}		Outputs LOW					16			mA
I_{CCZ}		Outputs "off"					25			mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1					6.0				ns
t_{PHL} Propagation delay	Waveform 2					7.5				ns
t_{pZH} Enable to HIGH	Waveform 6, $C_L = 50pF$					19.5				ns
t_{pZL} Enable to LOW	Waveform 7, $C_L = 50pF$					21				ns
t_{PHZ} Disable from HIGH	Waveform 6	$C_L = 5pF(c)$				8.5				ns
		$C_L = 15pF$				12				ns
t_{PLZ} Disable from LOW	Waveform 7	$C_L = 5pF(c)$				14				ns
		$C_L = 15pF$				16				ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc Characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54S/74S135

PIN CONFIGURATION

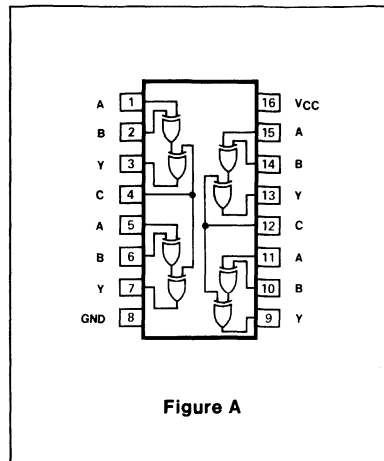


Figure A

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74S135N	
Ceramic DIP	Fig. A	N74S135F	S54S135F
Flatpak	Fig. A		S54S135W

TRUTH TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN OUT TABLE^(a)

PINS	54/74	54H/74H	54S/74S	54LS/74LS
Inputs I_{IH} (μA) I_{IL} (mA)			50	
			-2.0	
Outputs I_{OH} (μA) I_{OL} (mA)			-1000	
			20	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$						99			mA

NOTES

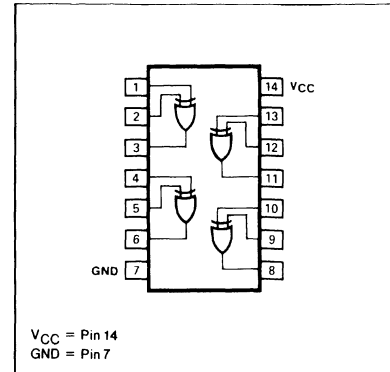
- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family DC Characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
						$C_L = 15\text{pF}$ $R_L = 280\Omega$				
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 2, C = LOW B or A = LOW					13 15			ns ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 1, C = LOW B or A = HIGH					12 13.5			ns ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 1, C = HIGH B or A = LOW					15 10			ns ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 2, C = HIGH B or A = HIGH					12 11			ns ns
t_{PLH} t_{PHL}	Propagation delay C to output	Waveform 2, A = B					12 14.5			ns ns
t_{PLH} t_{PHL}	Propagation delay C to output	Waveform 1, A \neq B					11.5 12			ns ns

54LS/74LS136

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	Fig. A	N74LS136N	
Ceramic DIP	Fig. A	N74LS136F	S54LS136F
Flatpak	Fig. A		S54LS136W

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = LOW voltage level
H = HIGH voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I _{IH} (μA)				20
	I _{IL} (mA)				-0.4
Outputs	I _{OH} (μA)				+100
	I _{OL} (mA)				4/8(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current	V _{CC} = Max, V _{IN} = 0V							10	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation delay								30	ns
t _{PHL}	A or B to output	Other input LOW Waveform 2							30	ns
t _{PLH}	Propagation delay								30	ns
t _{PHL}	A or B to output	Other input HIGH Waveform 1							30	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc Characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54S/74S138
54LS/74LS138

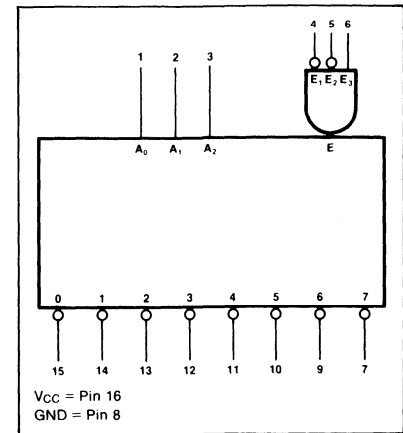
DESCRIPTION

The "138" is a HIGH speed 1-of-8 Decoder/Demultiplexer. The "138" is ideal for HIGH speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using only three "138" devices; or to a 1-of-32 decoder using four "138" devices and one inverter.

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

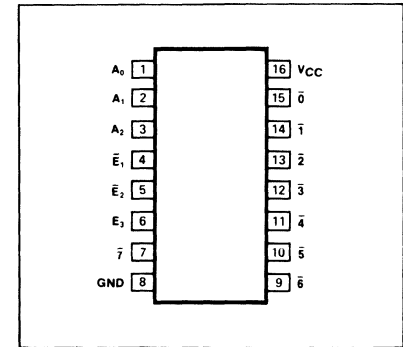
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$	
Plastic DIP	N74S138N	• N74LS138N		
Ceramic DIP	N74S138F	• N74LS138F	S54S138F	• S54LS138F
Flatpak			S54S138W	• S54LS138W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION	54/74	54S/74S	54LS/74LS
A ₀ -A ₂	Address inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$	50 -2.0	20 -0.36
\bar{E}_1, \bar{E}_2	Enable (Active LOW) inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$	50 -2.0	20 -0.36
E ₃	Enable (Active HIGH) input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	50 -2.0	20 -0.36
$\bar{0}-\bar{7}$	Decoder outputs	$I_{OH} (\mu A)$ $I_{OL} (mA)$	-1000 20	-400 4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "138" decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW outputs ($\bar{0}-\bar{7}$). The device features three Enable inputs: two active LOW (\bar{E}_1, \bar{E}_2) and one active HIGH (E_3). Every output will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple Enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four "138's" and one inverter.

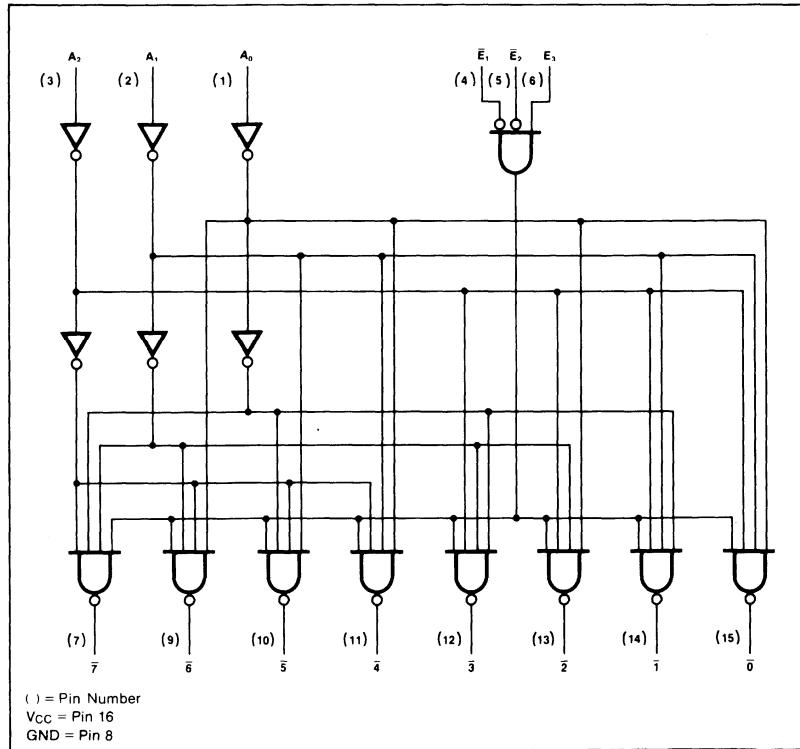
The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES
 H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

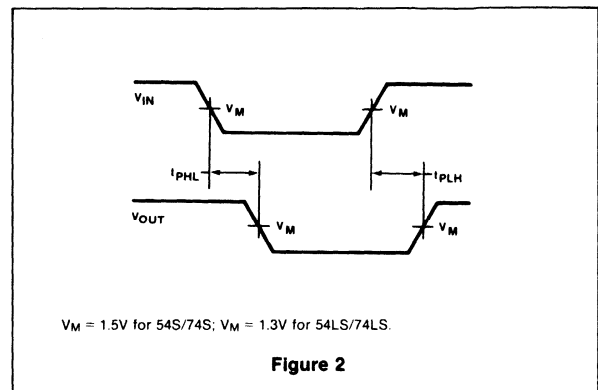
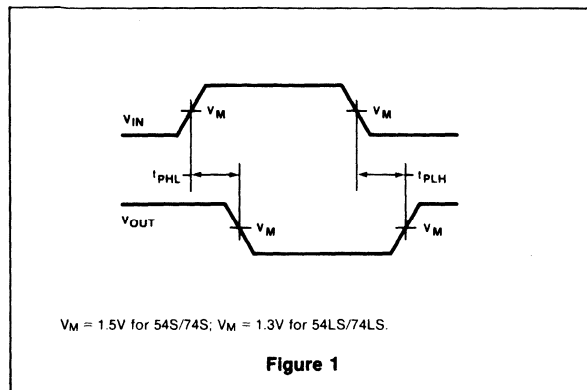
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current				74		10	mA

NOTE
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
				$C_L = 15\text{ pF}$ $R_L = 280\ \Omega$		$C_L = 15\text{ pF}$ $R_L = 2\text{ k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output				12		27	ns
t_{PLH} t_{PHL}	Propagation delay \bar{E}_1 and \bar{E}_2 to output				8.0		18	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to output				11		26	ns
t_{PLH} t_{PHL}	Propagation delay E_3 to output				11		38	ns

AC WAVEFORMS



54S/74S139
54LS/74LS139

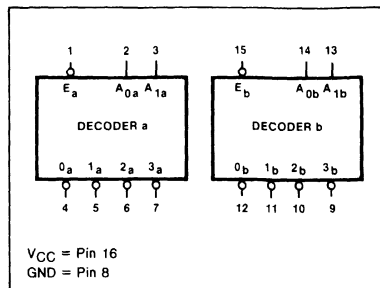
DESCRIPTION

The "139" is a high speed Dual 1-of-4 Decoder/Demultiplexer. This device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input useable as a data input for a 1-of-4 demultiplexer. Each half of the "139" is useable as a function generator providing all four minterms of two variables.

FEATURES

- Demultiplexing capability
- Two independent 1-of-4 decoders
- Multifunction capability
- Replaces 9321 and 93L21 for higher performance

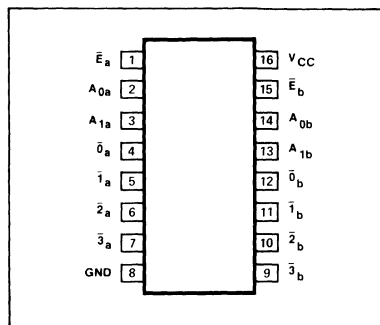
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C		MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C	
	Plastic DIP	N74S139N	• N74LS139N	
Ceramic DIP	N74S139F	• N74LS139F	S54S139F	• S54LS139F
Flatpak			S54S139W	• S54LS139W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A ₀ , A ₁	Address inputs	I _{IH} (μA) I _{IL} (mA)		50 -2.0	20 -0.36
\bar{E}	Enable (Active LOW) inputs	I _{IH} (μA) I _{IL} (mA)		50 -2.0	20 -0.36
$\bar{0}$ - $\bar{3}$	Decoder outputs	I _{OH} (μA) I _{OL} (mA)		-1000 20	-400 4/8(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current				90		11	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

FUNCTIONAL DESCRIPTION

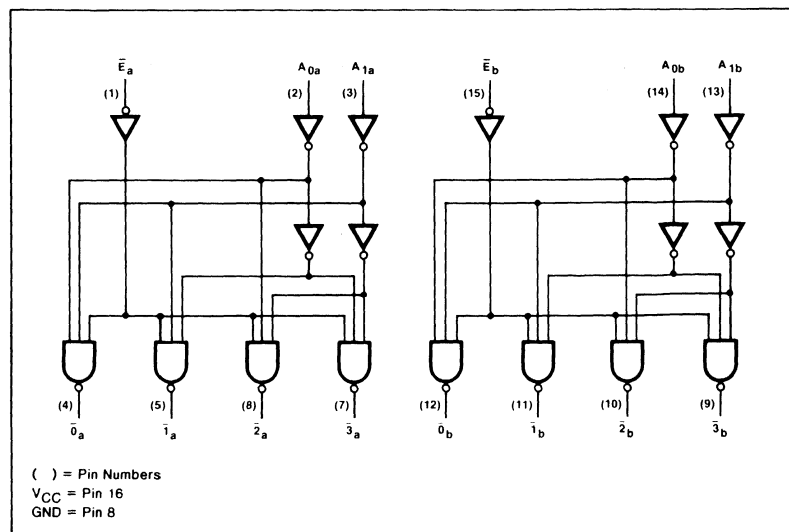
The "139" is a high speed dual 1-of-4 Decoder/Demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active LOW outputs ($\bar{0} - \bar{3}$). Each decoder has an active LOW Enable (\bar{E}). When \bar{E} is HIGH, every output is forced HIGH. The Enable can be used as the data input for a 1-of-4 demultiplexer application.

TRUTH TABLE

INPUTS			OUTPUTS			
\bar{E}	A_0	A_1	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level

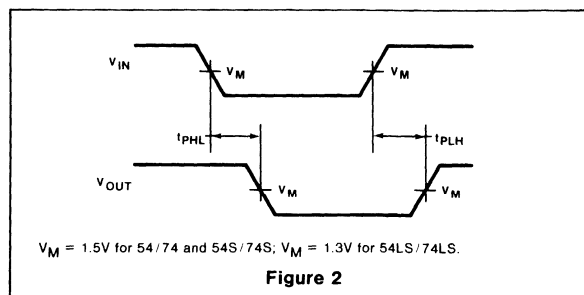
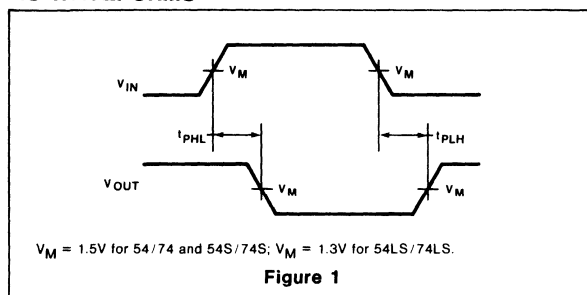
LOGIC DIAGRAM



AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
				$C_L = 15\text{pF}$ $R_L = 280\Omega$		$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Figure 1			12 12		29 38	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Figure 2			8.0 10		24 32	ns ns

AC WAVEFORMS



54S/74S140

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74S140N	
Ceramic DIP	Fig. A	N74S140F	S54S140F
Flatpak	Fig. A		S54S140W

PIN CONFIGURATION

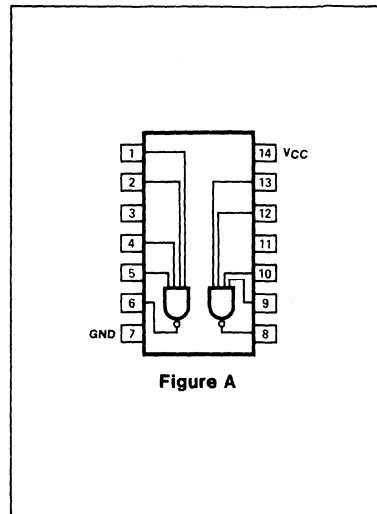


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)			100	
	I_{IL} (mA)			-4.0	
Outputs	I_{OH} (mA)			-3.0	
	I_{OL} (mA)			60	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}, V_{IN} = 0.8V$ $I_{OH} = -3.0mA$	Mil.				2.5				V
		Com.				2.7				V
	$V_{CC} = \text{Min}, V_{IN} = 0.5V,$ $R_O = 50\Omega$ to GND					2.0				V
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}, V_{IN} = 2V, I_{OL} = 60mA$						0.5			V
I_{OS} Short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$					-50	-225			mA
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$						18			mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$						44			mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

SYMBOL	PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
							$C_L = 50pF$ $R_L = 93\Omega$				
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PLH}	Propagation delay	Waveform 1						6.5 6.5			ns ns

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc Characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

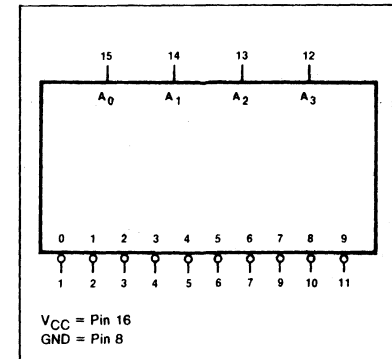
54/74145
54LS/74LS145 (Preliminary data)

DESCRIPTION

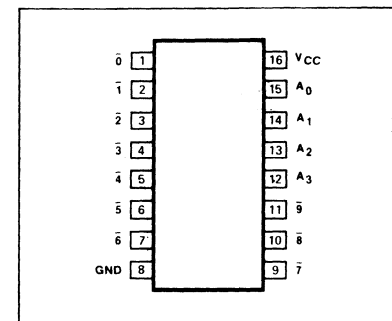
The "145" is a TTL MSI array. It features standard TTL inputs and high voltage, high current (80mA) outputs. The "145" minimum output breakdown is 15 volts.

FEATURES

- 80mA output drive capability
- 15V output breakdown voltage
- See "45" for 30V output voltage
- See "42" for standard TTL outputs

LOGIC SYMBOL**ORDERING CODE** (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ\text{C}$ to $+70^\circ\text{C}$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$	
Plastic DIP	N74145N	• N74LS145N		
Ceramic DIP	N74145F	• N74LS145F	S54145F	• S54LS145F
Flatpak			S54145W	• S54LS145W

PIN CONFIGURATION**INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)**

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
$A_0 - A_3$	Address inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
$\bar{0} - \bar{9}$	Active LOW outputs	I_{OH} (μA) I_{OL} (mA)	+250 80		+250 12/80(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$	$I_{OL} = 12\text{mA}$					0.4	V
		$I_{OL} = 20\text{mA}$		0.4				V
		$I_{OL} = 24\text{mA}$					0.5(c)	V
		$I_{OL} = 80\text{mA}$		0.9			1.7(c)	V
I_{OH} Output HIGH current	$V_{CC} = \text{Min}$, $V_{OUT} = 15\text{V}$		250				250	μA
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil	62				13	mA
		Com	70				13	mA

NOTES

- The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- This parameter for Commercial range only.

FUNCTIONAL DESCRIPTION

The "145" is a 1-of-10 decoder with open collector outputs. This decoder accepts BCD inputs on the A₀ to A₃ address lines and generates ten mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A₃ used as an active LOW enable.

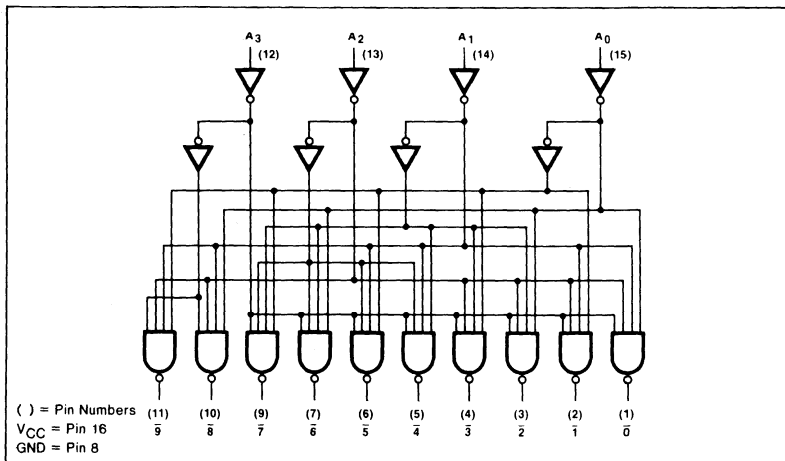
The "145" features an output breakdown voltage of 15V. This device is ideal as a lamp or solenoid driver.

TRUTH TABLE

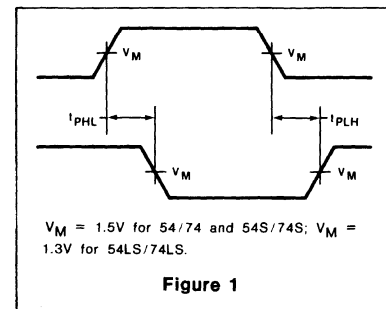
A ₃	A ₂	A ₁	A ₀	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

LOGIC DIAGRAM



AC WAVEFORM



AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 100Ω				C _L = 45pF R _L = 667Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay	Figure 1		50				50	ns
t _{PHL} Address to output			50				50	ns

54/74147

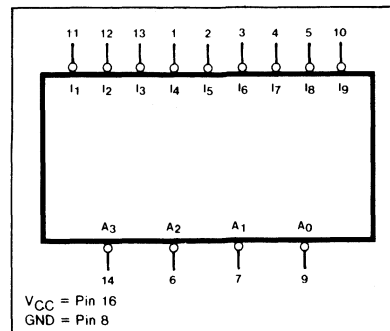
DESCRIPTION

The "147" 10-Line-to-4-Line Priority Encoder decodes the nine inputs to ensure that only the highest-order data line is encoded to four-line (8421) BCD outputs. Only nine data inputs are provided since the implied decimal "zero" condition requires no data input. The "zero" is encoded when all nine data lines are at a HIGH logic level. All of the "147" inputs and outputs are active LOW which simplifies mechanical switch encoding.

FEATURES

- Encodes 10-line decimal to 4-line BCD
- Useful for 10-position switch encoding
- Used in code converters and generators

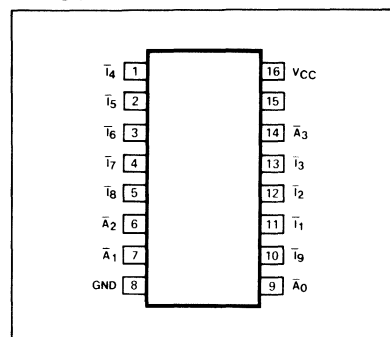
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74147N	
Ceramic DIP	N74147F	S54147F
Flatpak		S54147W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
$\bar{T}_1 - \bar{T}_9$	Priority (active LOW) inputs	I_{IH} (μ A) I_{IL} (mA)	40 -1.6		
$\bar{A}_0 - \bar{A}_3$	Address (active LOW) outputs	I_{OH} (μ A) I_{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "147" 9-input priority encoder accepts data from nine active LOW inputs (\bar{I}_1 - \bar{I}_9) and provides a binary representation on the four active LOW outputs (\bar{A}_0 - \bar{A}_3). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line \bar{I}_9 having the highest priority.

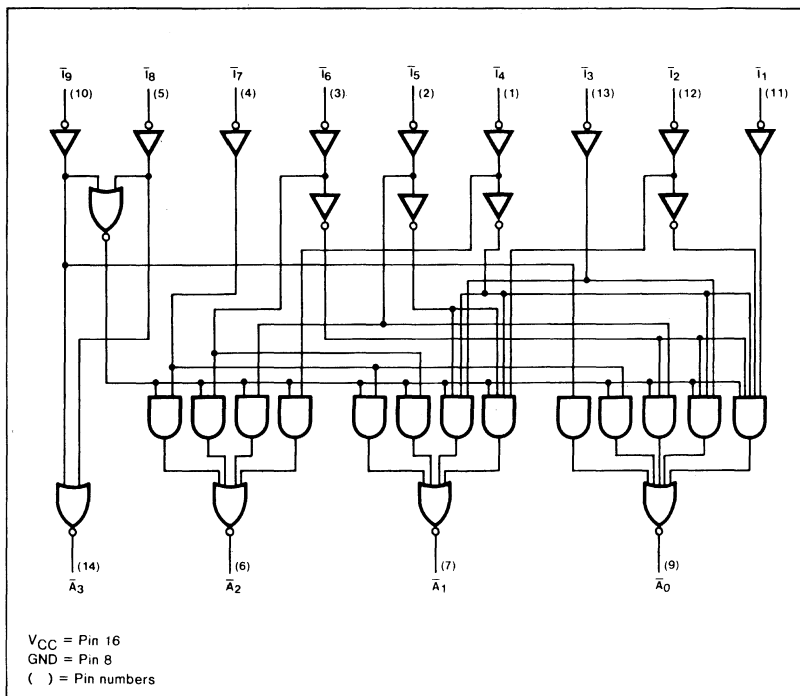
The device provides the 10-line-to-4-line priority encoding function by use of the implied decimal "zero." The "zero" is encoded when all nine data inputs are HIGH forcing all four outputs HIGH.

TRUTH TABLE

INPUTS									OUTPUTS			
\bar{I}_1	\bar{I}_2	\bar{I}_3	\bar{I}_4	\bar{I}_5	\bar{I}_6	\bar{I}_7	\bar{I}_8	\bar{I}_9	\bar{A}_3	\bar{A}_2	\bar{A}_1	\bar{A}_0
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{OS}	Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$		-35	-85			mA
I_{CC}	Supply current	$V_{CC} = \text{Max}, V_{\bar{I}} = 0V$			70			mA
		$V_{CC} = \text{Max}, \text{inputs open}$			62			mA

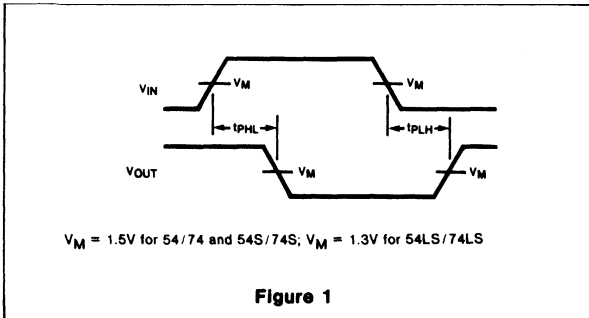
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay any input to output	Figure 1						ns ns

AC WAVEFORMS



54/74148

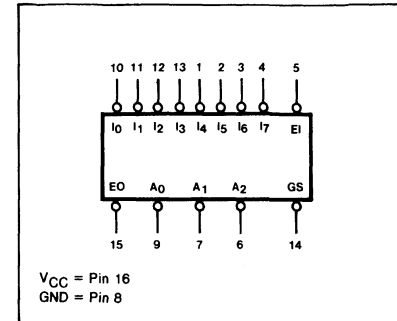
DESCRIPTION

The "148" is an 8-Input Priority Encoder designed to accept eight parallel inputs and produce the binary weighted code of the highest order input. Cascading capability has been provided to allow expansion without the need for external circuitry.

FEATURES

- Code conversions
- Multi-channel D/A converter
- Decimal to BCD converter
- Cascading for priority encoding of "N" bits
- Input enable capability
- Priority encoding—automatic selection of highest priority input line
- Output Enable—active LOW when all inputs HIGH
- Group Signal output—active when any input is LOW

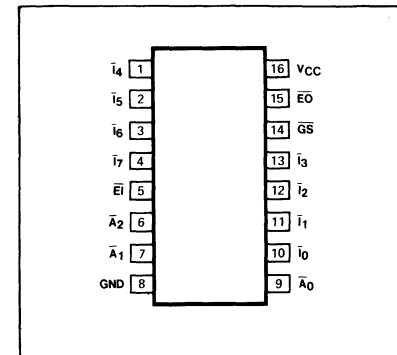
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74148N	
Ceramic DIP	N74148F	S54148F
Flatpak		S54148W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\bar{i}_0	Priority (active LOW) input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		
$\bar{i}_1-\bar{i}_7$	Priority (active LOW) inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$	80 -3.2		
\bar{E}_i	Enable (active LOW) input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	80 -3.2		
$\bar{A}_0-\bar{A}_2$	Address (active LOW) outputs	$I_{OH} (\mu A)$ $I_{OL} (mA)$	-800 16		
\bar{E}_O	Enable (active LOW) output	$I_{OH} (\mu A)$ $I_{OL} (mA)$	-800 16		
\bar{G}_S	Group Signal (active LOW) output	$I_{OH} (\mu A)$ $I_{OL} (mA)$	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "148" 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line \bar{I}_7 having the highest priority.

A HIGH on the Input Enable ($\bar{E}I$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

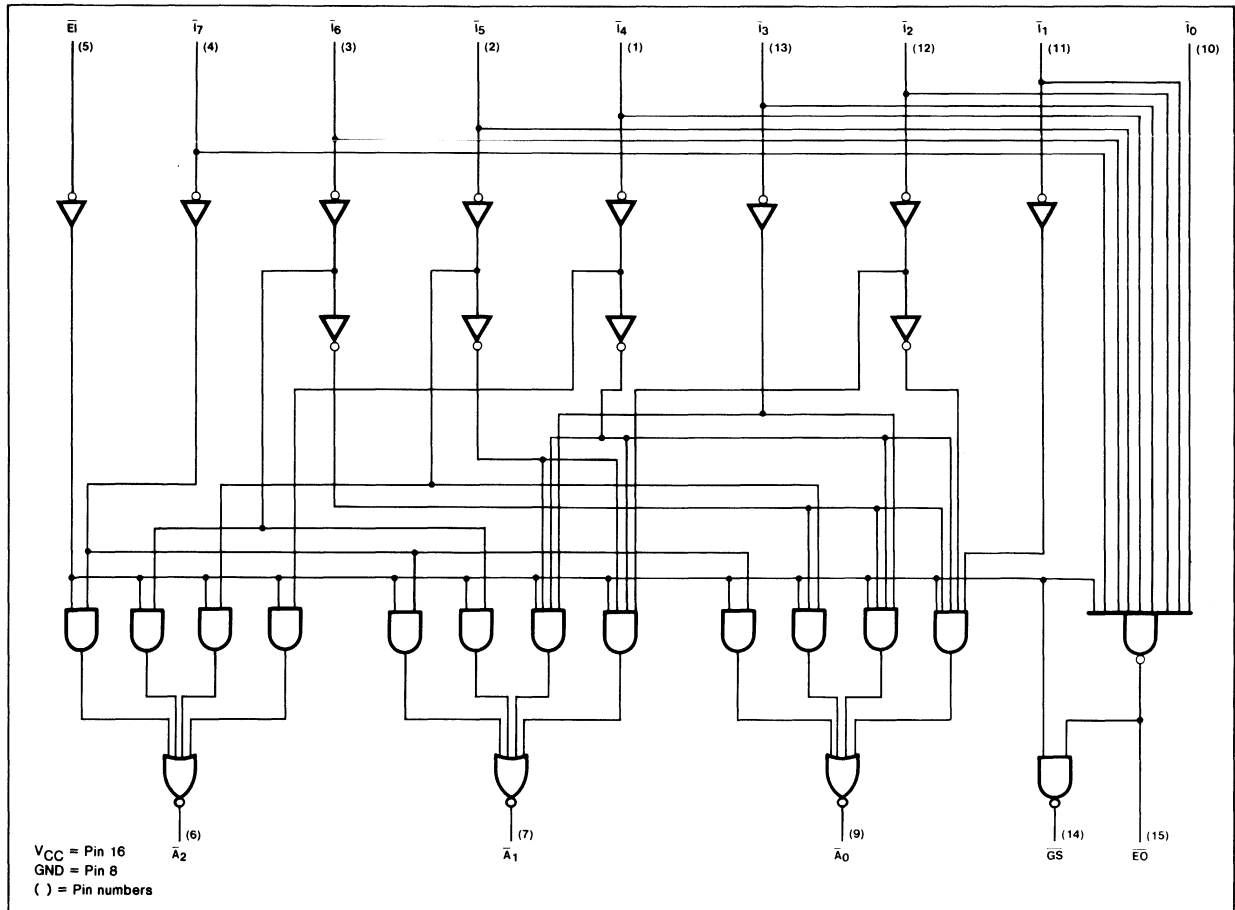
A Group Signal output ($\bar{G}S$) and an Enable Output ($\bar{E}O$) are provided with the three data outputs. The $\bar{G}S$ is active level LOW when any input is LOW; this indicates when any input is active. The $\bar{E}O$ is active level LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority coding of N input signals. Both $\bar{E}O$ and $\bar{G}S$ are active HIGH when the input enable is HIGH.

TRUTH TABLE

INPUTS									OUTPUTS				
$\bar{E}I$	\bar{I}_0	\bar{I}_1	\bar{I}_2	\bar{I}_3	\bar{I}_4	\bar{I}_5	\bar{I}_6	\bar{I}_7	$\bar{G}S$	\bar{A}_0	\bar{A}_1	\bar{A}_2	$\bar{E}O$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{OS}	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V		-35	-85			mA
I _{CC}	Supply current	V _{CC} = Max, V ₇ = V _{EI} = 0V			60			mA
		V _{CC} = Max, inputs open			55			mA

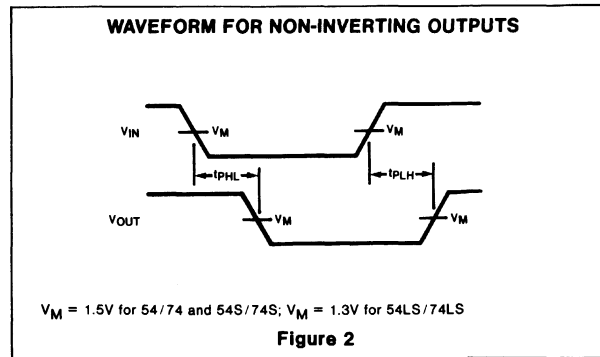
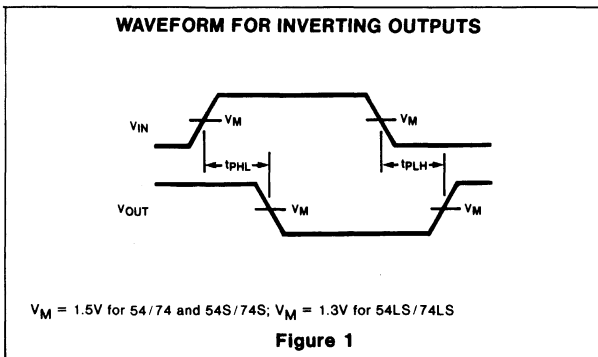
AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω						
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay I _n input to A _n outputs	Figure 1						ns ns
t _{PLH} t _{PHL}	Propagation delay I _n input to E _O output	Figure 1						ns ns
t _{PLH} t _{PHL}	Propagation delay I _n input to GS output	Figure 2						ns ns
t _{PLH} t _{PHL}	Propagation delay E _I input to A _n outputs	Figure 2						ns ns
t _{PLH} t _{PHL}	Propagation delay E _I input to E _O output	Figure 2						ns ns
t _{PLH} t _{PHL}	Propagation delay E _I input to GS output	Figure 2						ns ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications

AC WAVEFORMS



54/74150

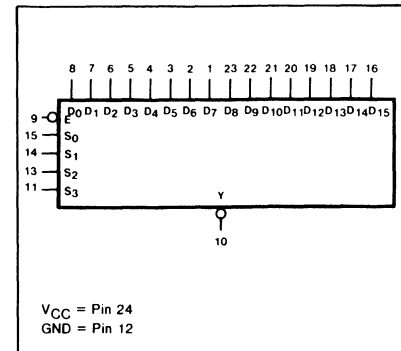
DESCRIPTION

The "150" is a 16-input digital Multiplexer providing, in one package, the ability to select one bit of data from up to 16 sources. The active LOW Enable can be used to strobe the multiplexer. The multiplexer output (\bar{Y}) inverts the selected data.

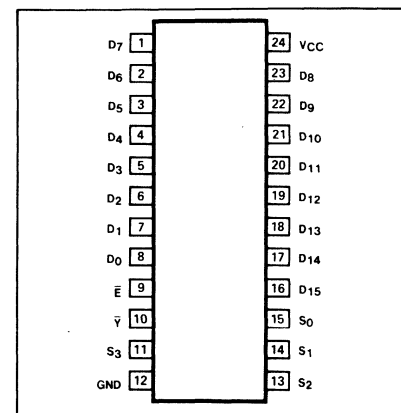
FEATURES

- Select data from 16 sources
- Demultiplexing capability
- Active LOW enable or strobe
- Inverting data output

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ\text{C}$ to $+70^\circ\text{C}$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
Plastic DIP	N74150N	
Ceramic DIP	N74150F	S54150F
Flatpak		S54150W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S_0-S_3	Select inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
\bar{E}	Enable (Active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
I_0-I_{15}	Multiplexer inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		
\bar{Y}	Inverting Multiplexer output	I_{OH} (μA) I_{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

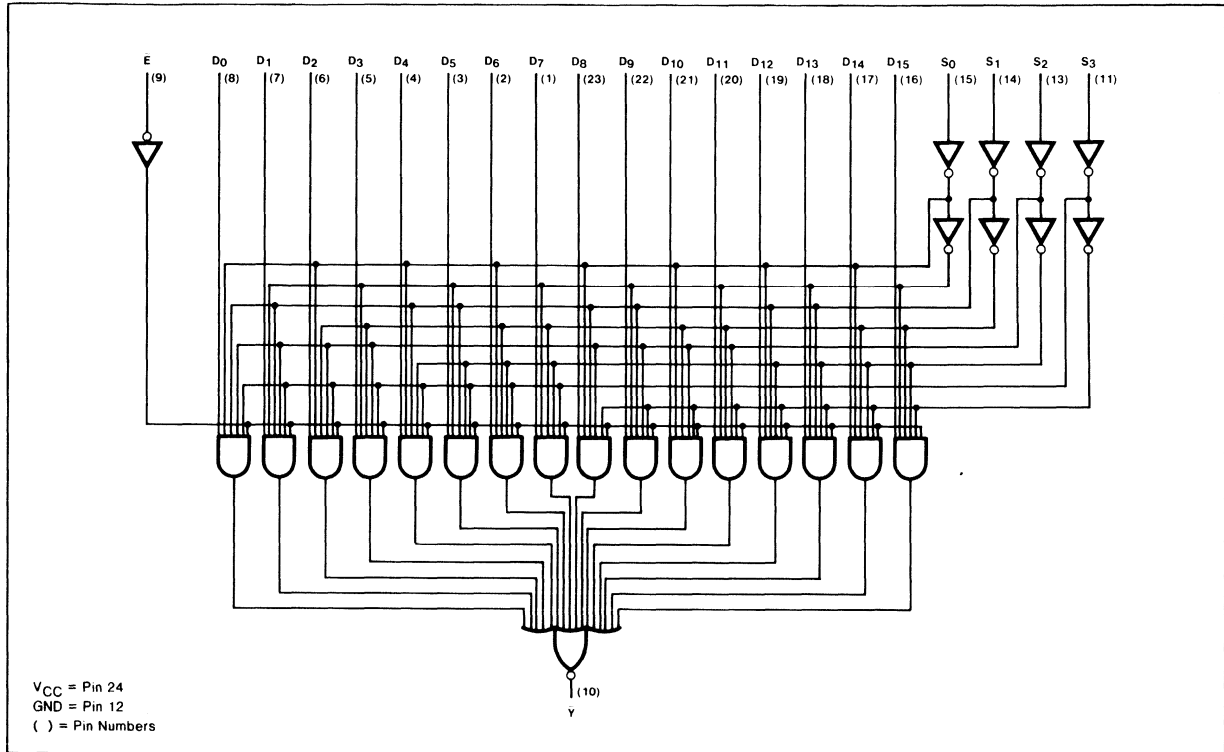
The "150" is a logical implementation of a single pole, 16-position switch with the switch position controlled by the state of four select inputs, S₀, S₁, S₂, S₃. The multiplexer output (\bar{Y}) inverts the selected data. The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH the \bar{Y} output is HIGH regardless of all other inputs. In one package the "150" provides the ability to select from 16 sources of data or control information.

TRUTH TABLE

INPUTS					INPUTS																OUTPUT	
S ₃	S ₂	S ₁	S ₀	E	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅	Y	
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54 / 74		54S / 74S		54LS / 74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current		68					mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

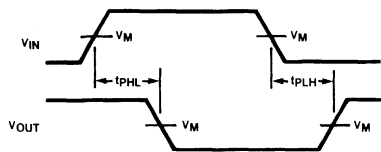
PARAMETER	TEST CONDITIONS	54 / 74		54S / 74S		54LS / 74LS		UNIT
		C _L = 15pF R _L = 400Ω						
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation delay		35					ns
t _{PHL}	Select to \bar{Y} output		33					ns
t _{PLH}	Propagation delay		24					ns
t _{PHL}	Enable to \bar{Y} output		30					ns
t _{PLH}	Propagation delay		20					ns
t _{PHL}	Data to \bar{Y} output		14					ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS

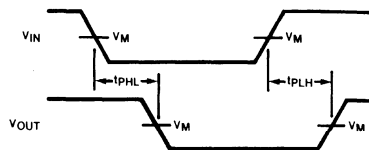
WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

Figure 1

WAVEFORM FOR NON-INVERTING OUTPUTS



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

Figure 2

54/74151
54S/74S151
54LS/74LS151

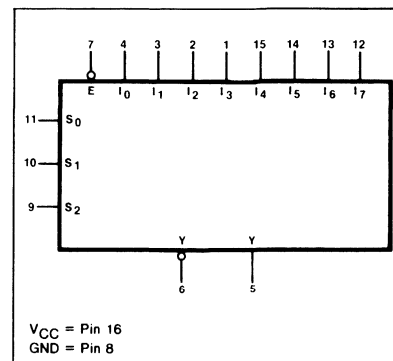
DESCRIPTION

The "151" is a high speed 8-input multiplexer providing, in one package, the ability to select one bit of data from up to eight sources. The device can be used as a universal function generator to generate any logic function of four variables.

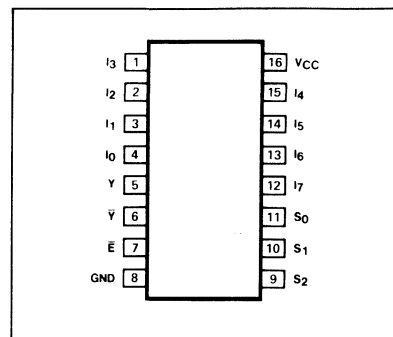
FEATURES

- Multifunction capability
- Complementary outputs
- See "251" for 3-state version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74151N • N74LS151N	
Ceramic DIP	N74151F • N74LS151F	S54151F • S54LS151F
Flatpak		S54151W • S54LS151W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S ₀ -S ₂	Select inputs	I _H (μA)	40	50	20
		I _L (mA)	-1.6	-2.0	-0.4
\bar{E}	Enable (active LOW) input	I _H (μA)	40	50	20
		I _L (mA)	-1.6	-2.0	-0.4
I ₀ -I ₇	Multiplexer inputs	I _H (μA)	40	50	20
		I _L (mA)	-1.6	-2.0	-0.4
Y	Multiplexer output	I _{OH} (μA)	-800	-1000	-400
		I _{OL} (mA)	16	20	4/8(a)
\bar{Y}	Complementary Multiplexer output	I _{OH} (μA)	-800	-1000	-400
		I _{OL} (mA)	16	20	4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "151" is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three select inputs, S₀, S₁, S₂. True (Y) and complement (\bar{Y}) outputs are both provided. The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH the \bar{Y} output is HIGH and the Y output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Y = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

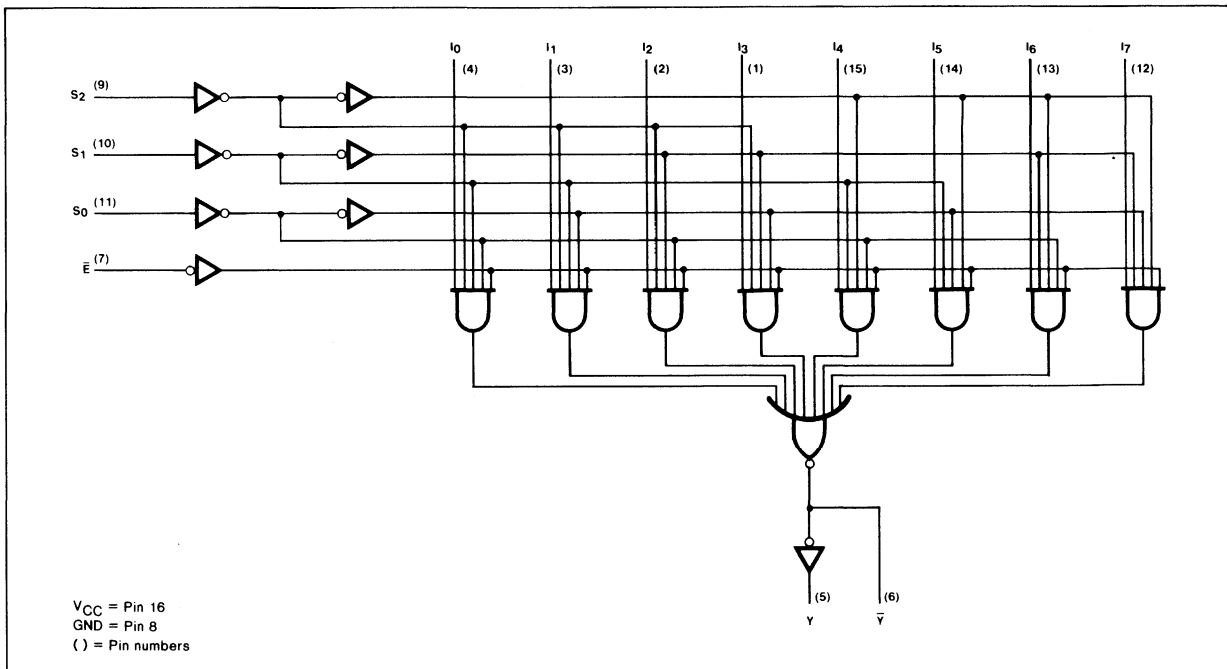
In one package the "151" provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

TRUTH TABLES

				INPUTS								OUTPUTS	
\bar{E}	S ₂	S ₁	S ₀	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	\bar{Y}	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage level
 L = LOW Voltage level
 X = Don't care

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		48		70		10	mA

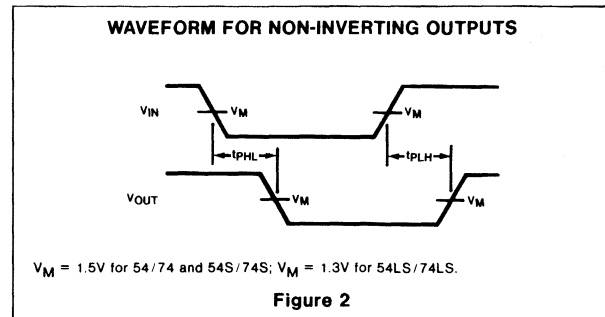
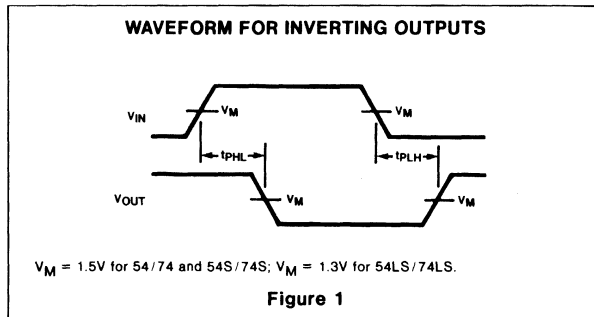
AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Select to Y output		52 30		18 18		30 26	ns
t _{PLH} t _{PHL}	Propagation delay Select to \bar{Y} output		35 33		15 13.5		20 20	ns
t _{PLH} t _{PHL}	Propagation delay Enable to Y output		52 30		16.5 18		30 20	ns
t _{PLH} t _{PHL}	Propagation delay Enable to \bar{Y} output		24 30		13 12		17 20	ns
t _{PLH} t _{PHL}	Propagation delay Data to Y output		29 24		12 12		24 17	ns
t _{PLH} t _{PHL}	Propagation delay Data to \bar{Y} output		20 14		7.0 7.0		15 15	ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54/74152

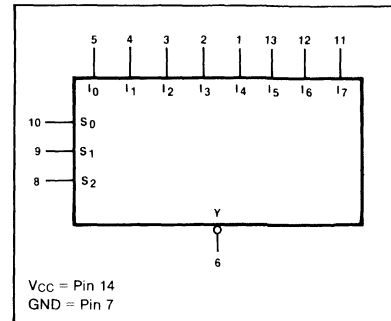
DESCRIPTION

The "152" is a high speed 8-Input Digital Multiplexer providing, in one package, the ability to select one bit of data from up to eight sources. The device can be used as a universal function generator to generate any logic function of four variables.

FEATURES

- 14-pin Flat Pack only
- Use "151" for enable or non-inverting output version

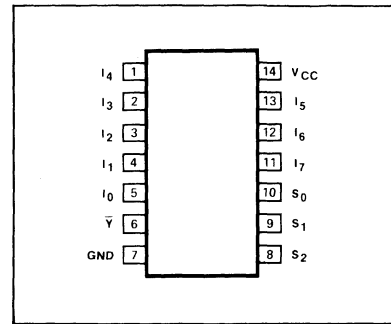
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP		
Ceramic DIP		
Flatpak		S54152W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
$S_0 - S_2$	Select inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		
$I_0 - I_7$	Data inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		
\bar{Y}	Complimentary multiplexer output	$I_{OH} (\mu A)$ $I_{OL} (mA)$	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "152" is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S₀, S₁, S₂. The logic function provided at the output is:

$$Y = I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2$$

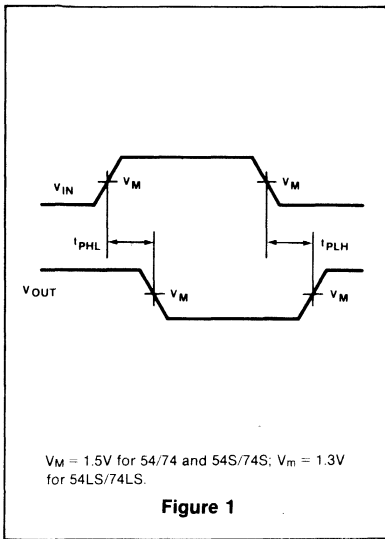
The "152" provides, in one package, the ability to select from eight sources of data or control information.

TRUTH TABLE

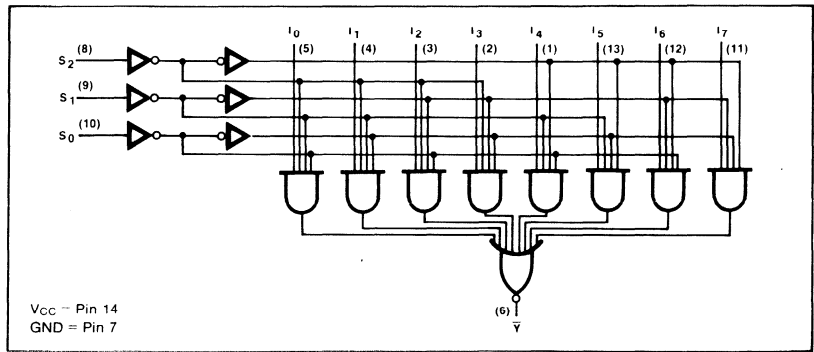
S ₂	S ₁	S ₀	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	Y
L	L	L	L	X	X	X	X	X	X	X	H
L	L	L	H	X	X	X	X	X	X	X	L
L	L	H	X	L	X	X	X	X	X	X	H
L	L	H	X	H	X	X	X	X	X	X	L
L	H	L	X	X	L	X	X	X	X	X	H
L	H	L	X	X	H	X	X	X	X	X	L
L	H	H	X	X	X	L	X	X	X	X	H
L	H	H	X	X	X	H	X	X	X	X	L
H	L	L	X	X	X	X	L	X	X	X	H
H	L	L	X	X	X	X	H	X	X	X	L
H	L	H	X	X	X	X	X	L	X	X	H
H	L	H	X	X	X	X	X	H	X	X	L
H	H	L	X	X	X	X	X	X	L	X	H
H	H	L	X	X	X	X	X	X	H	X	L
H	H	H	X	X	X	X	X	X	X	L	H
H	H	H	X	X	X	X	X	X	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

AC WAVEFORMS



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{OS} Output short circuit current	V _{CC} = Max	Mil	-20	-55				mA
	V _{OUT} = 0V	Com	-18	-55				mA
I _{CC} Supply current	V _{CC} = Max		43					mA

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay Select to Y output	Figure 1	C _L = 15pF R _L = 400Ω						ns
			35					ns
t _{PLH} Propagation delay Data to Y output	Figure 1	C _L = 15pF R _L = 400Ω						ns
			20					ns
t _{PHL} Propagation delay Select to Y output	Figure 1	C _L = 15pF R _L = 400Ω						ns
			33					ns
t _{PHL} Propagation delay Data to Y output	Figure 1	C _L = 15pF R _L = 400Ω						ns
			14					ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

54/74153
54S/74S153
54LS/74LS153

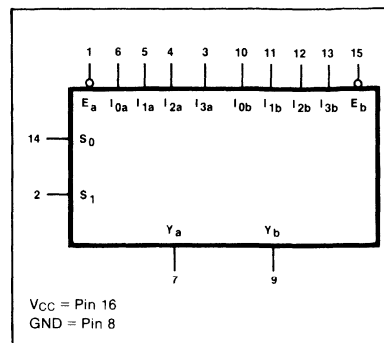
DESCRIPTION

The "153" is a high speed Dual 4-Input Multiplexer with common Select inputs and individual Enable inputs for each section. The device can select two bits of data from four sources. The two buffered outputs present data in the non-inverted (true) form. The "153" can generate any two functions of three variables in addition to multiplexer operation.

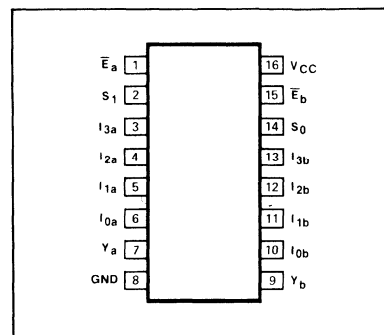
FEATURES

- Non-inverting outputs
- Separate Enable for each section
- Common Select inputs
- See "253" for 3-State version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	N74153N N74S153N • N74LS153N	
Ceramic DIP	N74153F N74S153F • N74LS153F	S54153F S54S153F • S54LS153F
Flatpak		S54153W S54S153W • S54LS153W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S ₀ , S ₁	Common Select inputs	I _{IH} (μA)	40	50	20
		I _{IL} (mA)	-1.6	-2.0	-0.4
E _a , E _b	Enable (Active LOW) inputs	I _{IH} (μA)	40	50	20
		I _{IL} (mA)	-1.6	-2.0	-0.4
I _{0a} - I _{3a}	Data inputs from multiplexer "a"	I _{IH} (μA)	40	50	20
		I _{IL} (mA)	-1.6	-2.0	-0.4
I _{0b} - I _{3b}	Data inputs from multiplexer "b"	I _{IH} (μA)	40	50	20
		I _{IL} (mA)	-1.6	-2.0	-0.4
Y	Multiplexer outputs	I _{OH} (μA)	-800	-1000	-400
		I _{OL} (mA)	16	20	4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "153" is a Dual 4-input Multiplexer that can select two bits of data from up to four sources under control of the common Select inputs (S₀, S₁). The two 4-input multiplexer circuits have individual active LOW Enables (E_a, E_b) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced LOW when the corresponding Enables (E_a, E_b) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Y_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

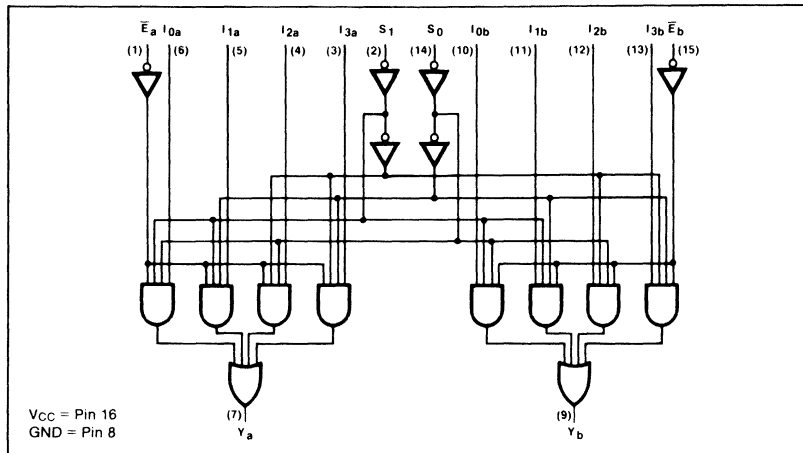
The "153" can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		E	INPUTS (a or b)				OUTPUT
S ₀	S ₁		I ₀	I ₁	I ₂	I ₃	
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max		
I _{CC} Supply current	V _{CC} = Max	Mil		52		70		10	mA
		Com		60		70		10	

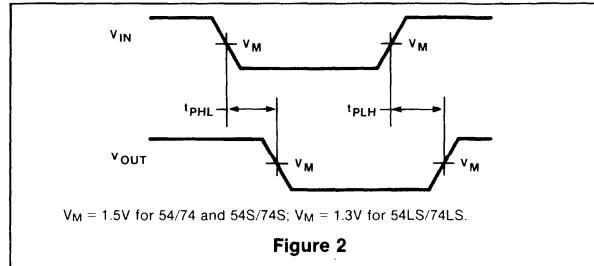
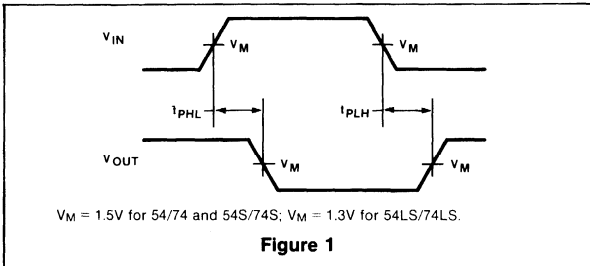
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 30\text{pF}$ $R_L = 400\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to output		34 34		18 18		29 38	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output		30 23		15 13.5		24 32	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output		18 23		9.0 9.0		15 26	ns ns

AC WAVEFORMS



54/74154
54LS/74LS154

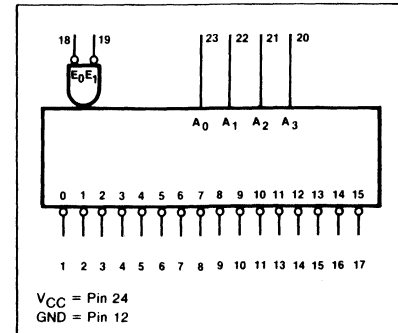
DESCRIPTION

The "154" is a 4-line to 16-line Decoder/Demultiplexer with a 2-input enable gate. It is designed to accept 4-bits of binary data and provide 1-of-16 mutually exclusive active LOW outputs. The enable can be used as a data input to demultiplex up to 16-bits of serial data.

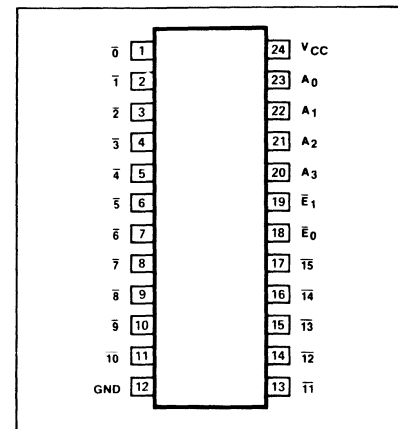
FEATURES

- 16-line demultiplexing capability
- Mutually exclusive outputs
- 2-input enable gate for strobing or expansion

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74154N • N74LS154N	
Ceramic DIP	N74154F • N74LS154F	S54154F • S54LS154F
Flatpak		S54154W • S54LS154W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
$A_0 - A_3$	Address inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.36
\bar{E}_0, \bar{E}_1	Enable (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.36
$\bar{O} - \bar{15}$	Active LOW outputs	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

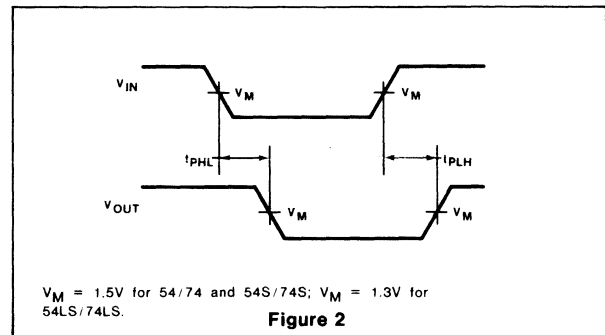
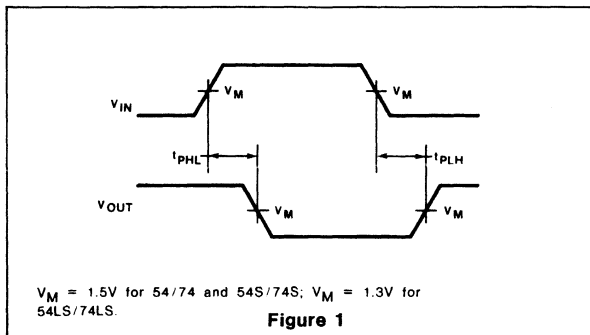
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil		49			14	mA
		Com		56			14	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for test circuits and conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay	Figure 1		36				36	ns
t _{PHL} Address to output			33				33	ns
t _{PLH} Propagation delay	Figure 2		30				30	ns
t _{PHL} Enable to output			27				27	ns

AC WAVEFORMS



NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54LS/74LS specification.

54/74155
54LS/74LS155

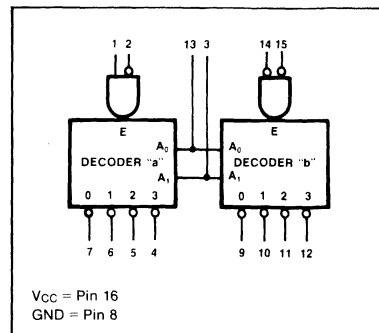
DESCRIPTION

The "155" is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device features common binary-address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs.

FEATURES

- Common address inputs
- True or complement data demultiplexing
- Dual 1-of-4 or 1-of-8 decoding
- Function generator applications
- (See "156" for details.)

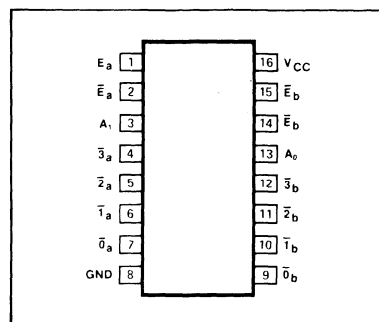
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N74155N	• N74LS155N	
Ceramic DIP	N74155F	• N74LS155F	S54155F	• S54LS155F
Flatpak			S54155W	• S54LS155W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_0, A_1	Address inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		20 -0.4
\bar{E}_a, \bar{E}_b	Enable (Active LOW) inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		20 -0.4
E_a	Enable (Active HIGH) input	$I_{IH} (\mu A)$ $I_{IL} (mA)$	40 -1.6		20 -0.4
$\bar{0} - \bar{3}$	Active LOW outputs	$I_{OH} (\mu A)$ $I_{OL} (mA)$	-800 16		-400 4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil		35			10	mA
		Com		40			10	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

FUNCTIONAL DESCRIPTION

The "155" is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address input (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\bar{0}-\bar{3}$). When the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

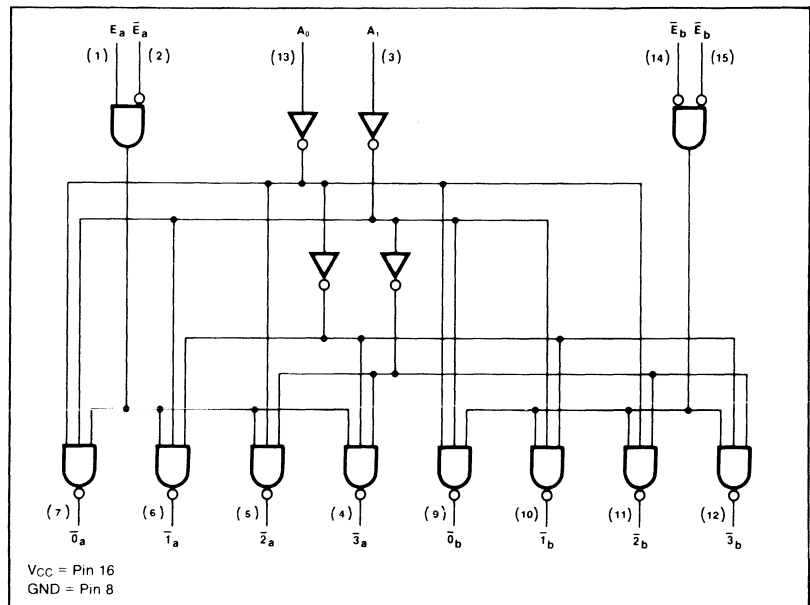
Both decoder sections have a 2-input enable gate. For Decoder "a" the enable gate requires one active HIGH input and one active LOW input ($E_a \bullet \bar{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the \bar{E}_a or E_a inputs respectively. The Decoder "b" enable gate requires two active LOW inputs ($\bar{E}_b \bullet \bar{E}_b$). The device can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to \bar{E}_b and relabeling the common connection as address (A_2); forming the common enable by connecting the remaining \bar{E}_b and \bar{E}_a .

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	\bar{E}_a	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	\bar{E}_b	\bar{E}_b	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care.

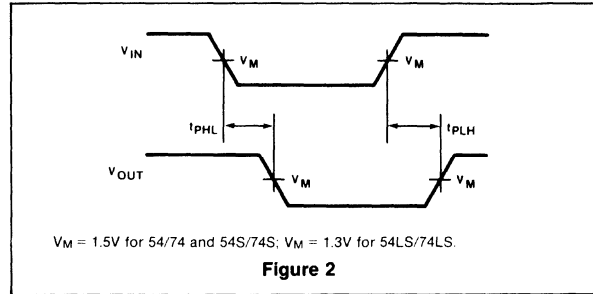
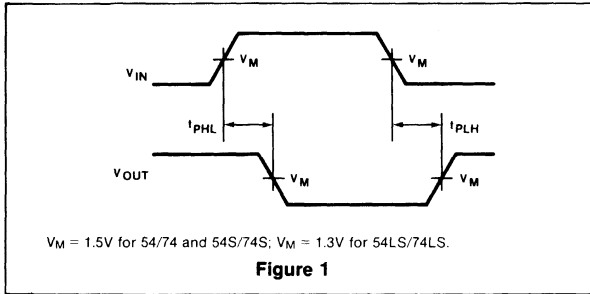
LOGIC DIAGRAM



AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{ pF}$ $R_L = 400\ \Omega$				$C_L = 15\text{ pF}$ $R_L = 2\text{ k}\ \Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output		32 32				26 30	ns ns
t_{PLH} t_{PHL}	Propagation delay \bar{E}_a or \bar{E}_b to output		20 27				15 30	ns ns
t_{PLH} t_{PHL}	Propagation delay E_a to output		24 30				27 27	ns ns

AC WAVEFORMS



**54/74156
54LS/74LS156**

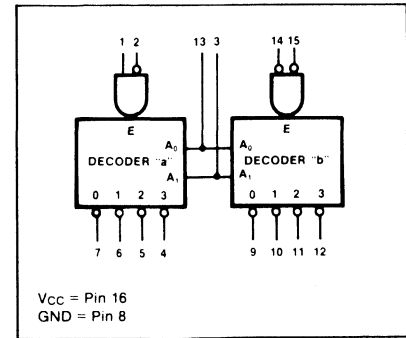
DESCRIPTION

The "156" is a high speed Dual 1-of-4 Decoder/Demultiplexer with open collector outputs featuring common binary-address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. Wired-OR (Dot-AND) decoding and function generator applications are available through the open collector outputs of the "156."

FEATURES

- Common address inputs
- True or complement data demultiplexing
- Dual 1-of-4 or 1-of-8 decoding
- Function generator applications
- Outputs can be tied together

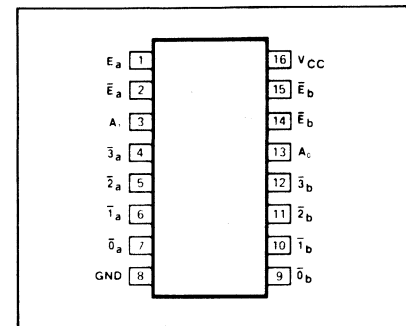
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	V _{CC} =5V ± 5%; T _A =0°C to +70°C		V _{CC} =5V ± 10%; T _A =-55°C to +125°C	
Plastic DIP	N74156N	•	N74LS156N	
Ceramic DIP	N74156F	•	N74LS156F	S54156F • S54LS156F
Flatpak				S54156W • S54LS156W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A ₀ , A ₁	Address inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
E _a , E _b	Enable (active LOW) inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
E _a	Enable (active HIGH) inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
O ₀₋₃	Active LOW open collector outputs	I _{OH} (μA) I _{OL} (mA)	+250 16		+100 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "156" is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\bar{0}-\bar{3}$). When the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Both decoder sections have a 2-input enable gate. For Decoder "a" the enable gate requires one active HIGH input and one active LOW input ($E_a \cdot \bar{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the \bar{E}_a or E_a inputs respectively. The Decoder "b" enable gate requires two active LOW inputs ($\bar{E}_b \cdot \bar{E}_b$). The device can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to \bar{E}_b and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining \bar{E}_b and \bar{E}_a .

The "156" can be used to generate all 4 minterms of 2 variables. The 4 minterms are useful to replace multiple gate functions in some applications. A further advantage of the "156" is being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown in the formula below.

$$f = (E + A_0 + A_1) \cdot (E + \bar{A}_0 + A_1) \cdot (E + A_0 + \bar{A}_1) \cdot (E + \bar{A}_0 + \bar{A}_1)$$

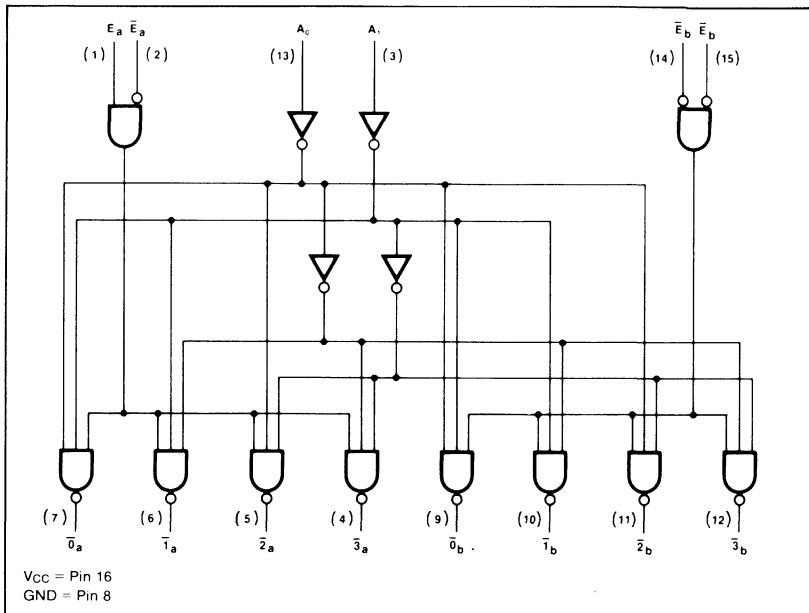
where $E = E_a + E_a$; $E = E_b + E_b$

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	\bar{E}_a	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	\bar{E}_b	\bar{E}_b	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
L	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care.

LOGIC DIAGRAM



Vcc = Pin 16
 GND = Pin 8

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current	V _{CC} = Max	Mil	35				10	mA	
			Com	40				10	mA	

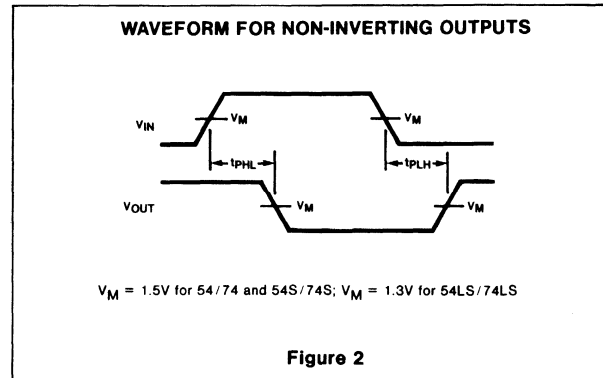
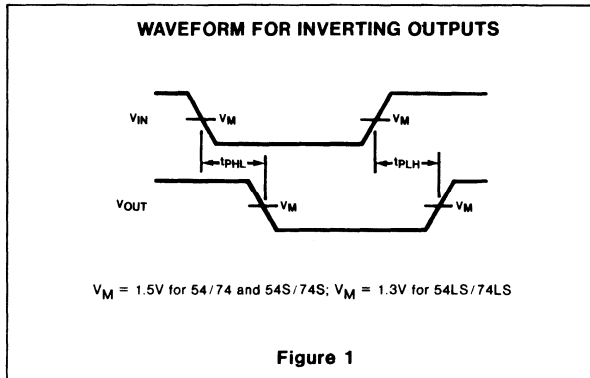
AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2kΩ		
				Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation delay	Figure 1		34				46	ns	
t _{PHL}	Address to output			34				51	ns	
t _{PLH}	Propagation delay	Figure 2		23				40	ns	
t _{PHL}	E _a or E _b to output			30				51	ns	
t _{PLH}	Propagation delay	Figure 1		27				48	ns	
t _{PHL}	E _a to output			33				48	ns	

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



**54/74157
54S/74S157
54LS/74LS157**

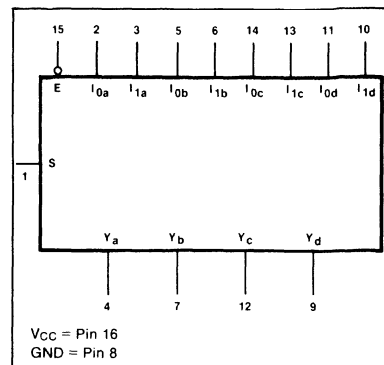
DESCRIPTION

The "157" is a high speed Quad 2-Input Multiplexer that can select 4-bits of data from two sources using the common Select and Enable inputs. The "157" presents true (non-inverted) data and can be used to generate any four of the 16 different functions of two variables.

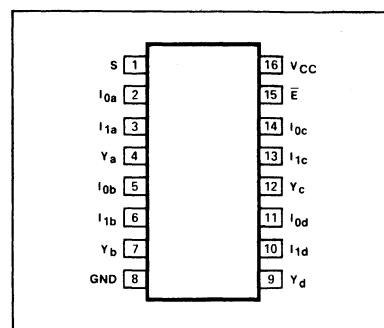
FEATURES

- Multifunction capability
- Non-inverting data path
- Direct replacement for 9322 and 93L22
- See "257" for 3-State version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	N74157N N74S157N • N74LS157N	
Ceramic DIP	N74157F N74S157F • N74LS157F	S54157F S54S157F • S54LS157F
Flatpak		S54157W S54S157W • S54LS157W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S	Select input	I_{IH} (μA)	40	100	40
		I_{IL} (mA)	-1.6	-4.0	-0.8
\bar{E}	Enable (Active LOW) input	I_{IH} (μA)	40	100	40
		I_{IL} (mA)	-1.6	-4.0	-0.8
$I_{0a} - I_{0d}$	Data inputs from Source 0	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
$I_{1a} - I_{1d}$	Data inputs from Source 1	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
$Y_a - Y_d$	Multiplexer outputs	I_{OH} (μA)	-800	-1000	-400
		I_{OL} (mA)	16	20	4/8 (a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current		48		78		16	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

FUNCTIONAL DESCRIPTION

The "157" is a Quad 2-Input Multiplexer which selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the "157." The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Y_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Y_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

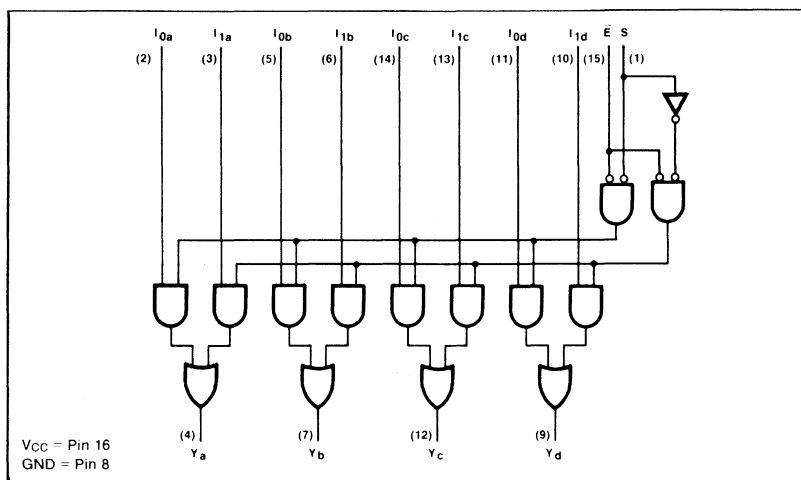
$$Y_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
\bar{E}	S	I ₀	I ₁	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

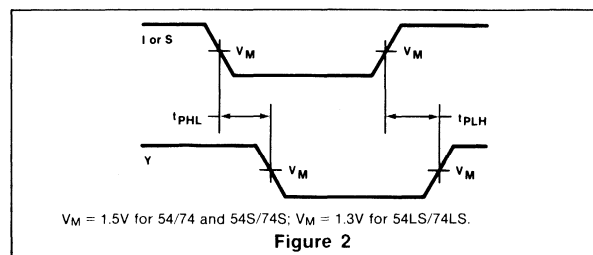
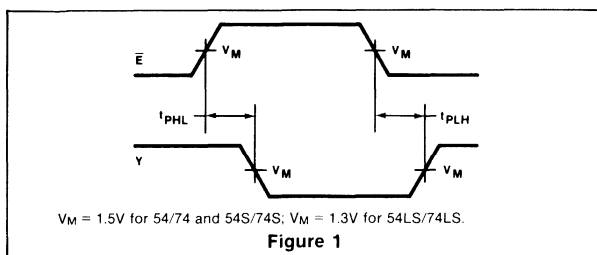
LOGIC DIAGRAM



AC CHARACTERISTICS T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pf R _L = 400Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Data to output	Figure 2		14	7.5	14	14	ns
t _{PLH} t _{PHL}	Propagation delay Enable to output	Figure 1		20	12.5	20	21	ns
t _{PLH} t _{PHL}	Propagation delay Select to output	Figure 2		23	15	23	27	ns

AC WAVEFORMS



**54/74158
54S/74S158
54LS/74LS158**

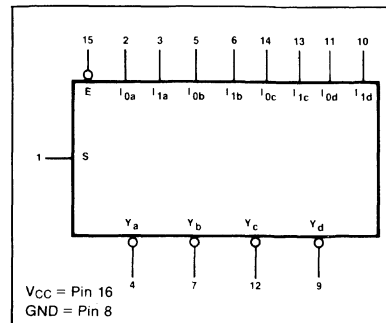
DESCRIPTION

The "158" is a high speed Quad 2-Input Multiplexer that selects 4-bits of data from two sources using the common Select and Enable inputs. The "158" presents inverted data. It can be used to generate any four of the 16 different functions of two variables.

FEATURES

- Multifunction capability
- Inverting data path
- See "258" for 3-State version
- See "157" for non-inverting version

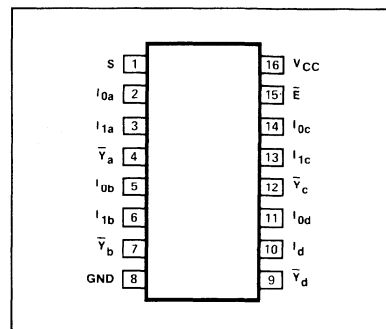
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	N74158N N74S158N • N74LS158N	
Ceramic DIP	N74158F N74S158F • N74LS158F	S54158F S54S158F • S54LS158F
Flatpak		S54158W S54S158W • S54LS158W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S	Select input	I_{IH} (μA) I_{IL} (mA)	40 -1.6	100 -4.0	40 -0.8
\bar{E}	Enable (Active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6	100 -4.0	40 -0.8
$I_{0a} - I_{0d}$	Data inputs from Source 0	I_{IH} (μA) I_{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
$I_{1a} - I_{1d}$	Data inputs from Source 1	I_{IH} (μA) I_{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
$\bar{Y}_a - \bar{Y}_d$	Multiplexer outputs	I_{OH} (μA) I_{OL} (mA)	-800 16	-1000 20	-400 4/8 (a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC}	Supply current		48		61		8.0	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

FUNCTIONAL DESCRIPTION

The "158" is a Quad 2-Input Multiplexer which selects four bits of data from two sources under the control of a common Select input (S), presenting the data in inverted form at the four outputs (\bar{Y}). The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (\bar{Y}) are forced HIGH regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the "158." The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing gating functions by generating any four functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. Logic equations are shown below:

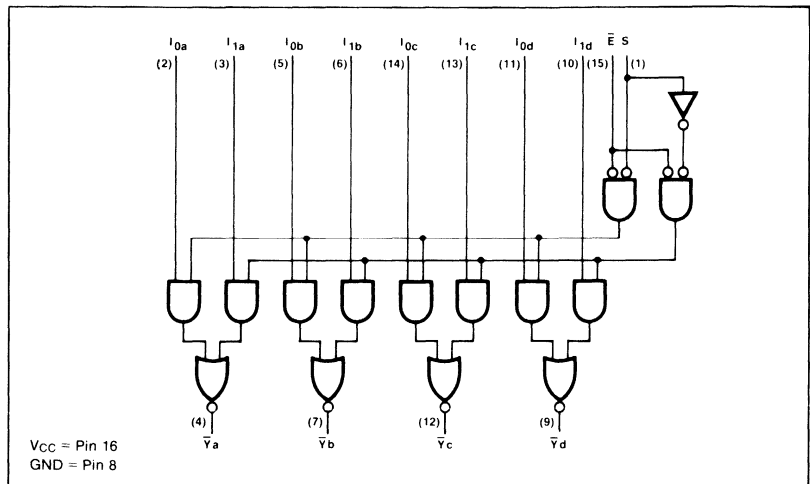
$$\begin{aligned} \bar{Y}_a &= \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ \bar{Y}_b &= \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ \bar{Y}_c &= \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ \bar{Y}_d &= \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

TRUTH TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
		I ₀	I ₁	
\bar{E}	S	I ₀	I ₁	\bar{Y}
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

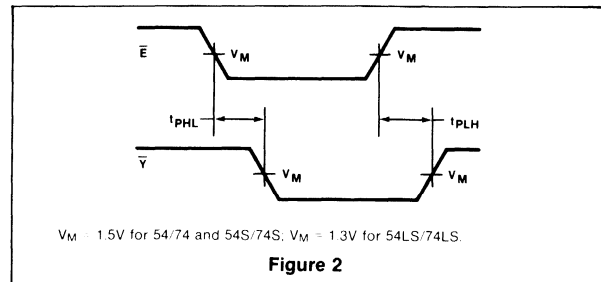
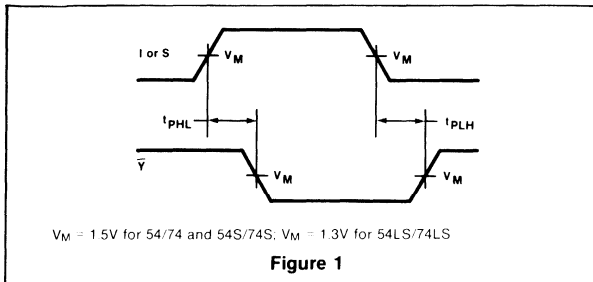
LOGIC DIAGRAM



AC CHARACTERISTICS T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Data to output	Figure 1		14	6.0	12	12	ns
t _{PLH} t _{PHL}	Propagation delay Enable to output	Figure 2		20	11.5	17	18	ns
t _{PLH} t _{PHL}	Propagation delay Select to output	Figure 1		23	12	20	24	ns

WAVEFORMS



54/74159

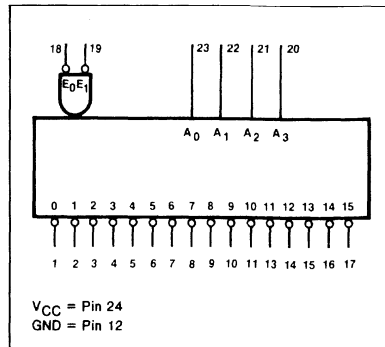
DESCRIPTION

The "159" is a 4-line to 16-line Decoder/Demultiplexer with open collector outputs and with a 2-input enable gate. It is designed to accept 4-bits of binary data and provide 1-of-16 mutually exclusive active LOW outputs. The enable can be used as a data input to demultiplex up to 16-bits of serial data. The outputs can be wired together to simplify function generation and provide output bussing.

FEATURES

- 16-line demultiplexing capability
- Mutually exclusive open collector outputs
- 2-input enable gate for strobing or expansion

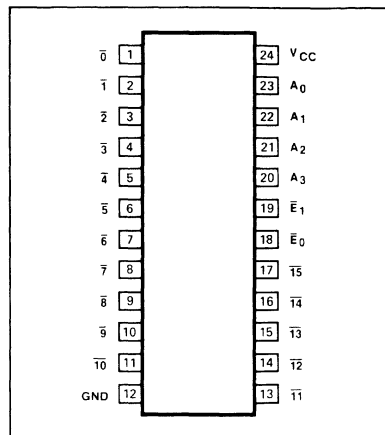
LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74159N	
Ceramic DIP	N74159F	S54159F
Flatpak		S54159W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A ₀ -A ₃	Address inputs	I _H (μA) I _L (mA)	40 -1.6		
\bar{E}_0, \bar{E}_1	Enable (active LOW) inputs	I _H (μA) I _L (mA)	40 -1.6		
$\bar{O}-\bar{15}$	Active LOW open collector outputs	I _{OH} (μA) I _{OL} (mA)	+50 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "159" decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The "159" can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

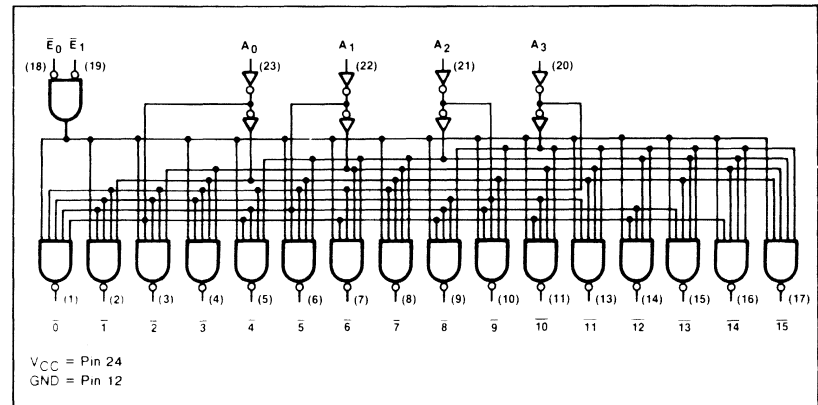
The open collector outputs can be wired together to provide a means of generating any combination of the 16 minterms of four variables applied to the A₀-A₃ inputs.

TRUTH TABLE

INPUTS					OUTPUTS																	
\bar{E}_0	\bar{E}_1	A ₃	A ₂	A ₁	A ₀	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$	$\bar{10}$	$\bar{11}$	$\bar{12}$	$\bar{13}$	$\bar{14}$	$\bar{15}$	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

LOGIC DIAGRAM



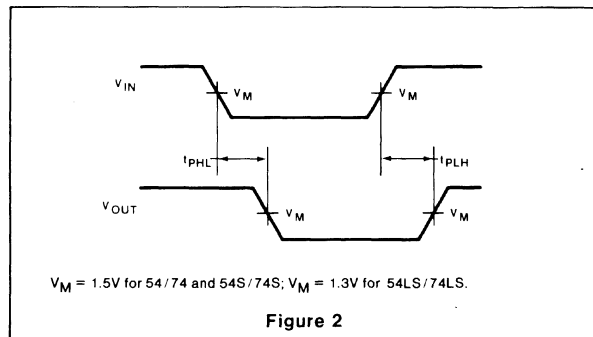
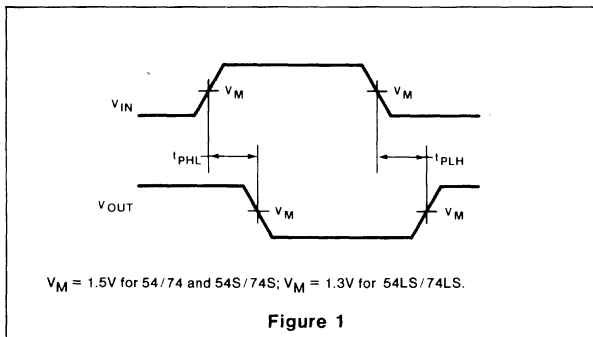
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE ^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		56					mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for test circuits and conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω						
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Address to output	Figure 1		36					ns ns
t _{PLH} Propagation delay t _{PHL} Enable to output	Figure 2		25 36					ns ns

AC WAVEFORMS



NOTE

b For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54LS/74LS specification.

54/74160
54LS/74LS160A

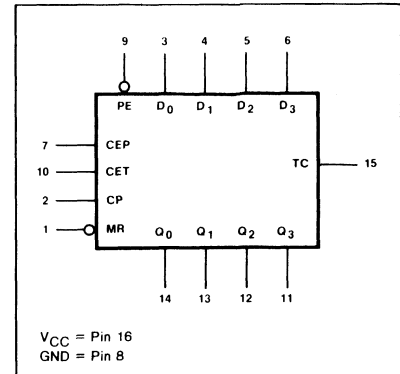
DESCRIPTION

The "160" is a high-speed BCD decade counter. The counters are positive edge-triggered, synchronously presettable and are easily cascaded to n-bit synchronous applications without additional gating. A Terminal Count output is provided which detects a count of HLLH. The Master Reset asynchronously clears all flip-flops.

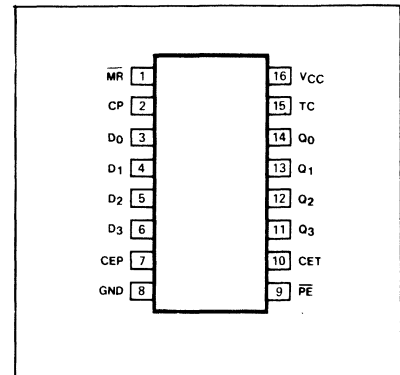
FEATURES

- Synchronous Counting and Loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Hysteresis on clock input (LS160 only)
- All inputs have fan-in of one (LS160 only)

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N74160N	• N74LS160AN	
Ceramic DIP	N74160F	• N74LS160AF	S54160F	• S54LS160AF
Flatpak			S54160W	• S54LS160AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		20 -0.4
D ₀ -D ₃	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
\overline{PE}	Parallel Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
CEP	Count Enable Parallel input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
CET	Count Enable Trickle input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		20 -0.4
\overline{MR}	Master Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
Q ₀ -Q ₃	Counter outputs	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)
TC	Terminal Count output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)

NOTE
a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "160" is a synchronous presettable BCD decade counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock. The clock input on the LS160 features about 400mV of hysteresis to reduce false triggering caused by noise on the clock line or by slowly rising clock edges.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function for the "160" is asynchronous. A LOW level on the Master Reset (\overline{MR}) input sets all four of the flip-flop outputs LOW, regardless of the levels of the CP, \overline{PE} , CET, and CEP inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET • CEP) and a Terminal Count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This HIGH level TC pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

All "changes" of the Q outputs (except due to the asynchronous Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the Clock input (CP). As long as the setup time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs. However, for conventional operation of the 54/74160 the following transitions should be avoided:

1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is LOW, if the count enables are HIGH at or before the transition.

For some applications, the designer may want to change those inputs while the clock is LOW. In this case, the 54/74160 will behave in a predictable manner. For example:

If \overline{PE} goes HIGH while the clock is LOW, and Count Enable is not active during the re-

maining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW-to-HIGH clock transition will change $Q_0 - Q_3$ to the $D_0 - D_3$ data that existed at the setup time before the rising edge of \overline{PE} .

If \overline{PE} goes HIGH while the clock is LOW, and Count Enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 54/74160 will perform a mixture of counting and loading. On the LOW-to-HIGH clock transition, outputs $Q_0 - Q_3$ will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and are also reloaded with their present value stay constant.

If Count Enable is active (i.e. CEP and CET are HIGH) during some portion of the clock LOW period, and \overline{PE} is HIGH (inactive) during the entire clock LOW period, the subsequent LOW-to-HIGH clock transition will change $Q_0 - Q_3$ to the next count value.

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(b)
Count	H	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	H	X	l(c)	X	h(d)	X	q_n	(b)
	H	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Don't care.

q = Lower case letters indicate the state of the referenced output prior to the LOW-to-

HIGH clock transition.

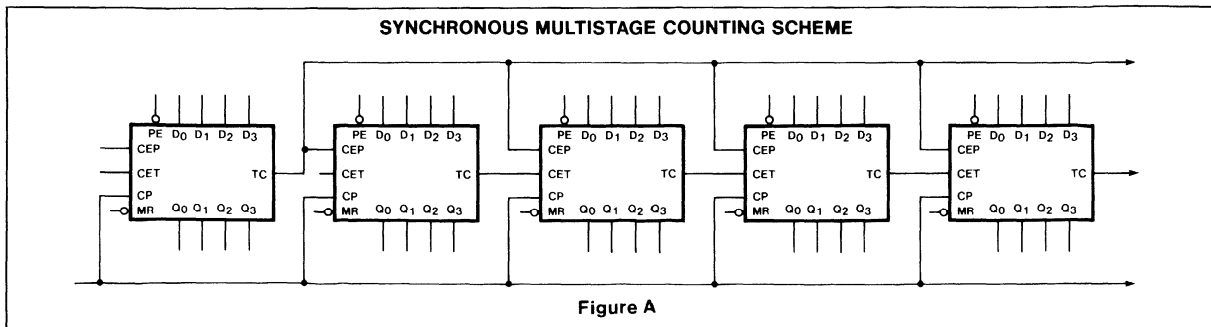
↑ = LOW-to-HIGH clock transition.

NOTES

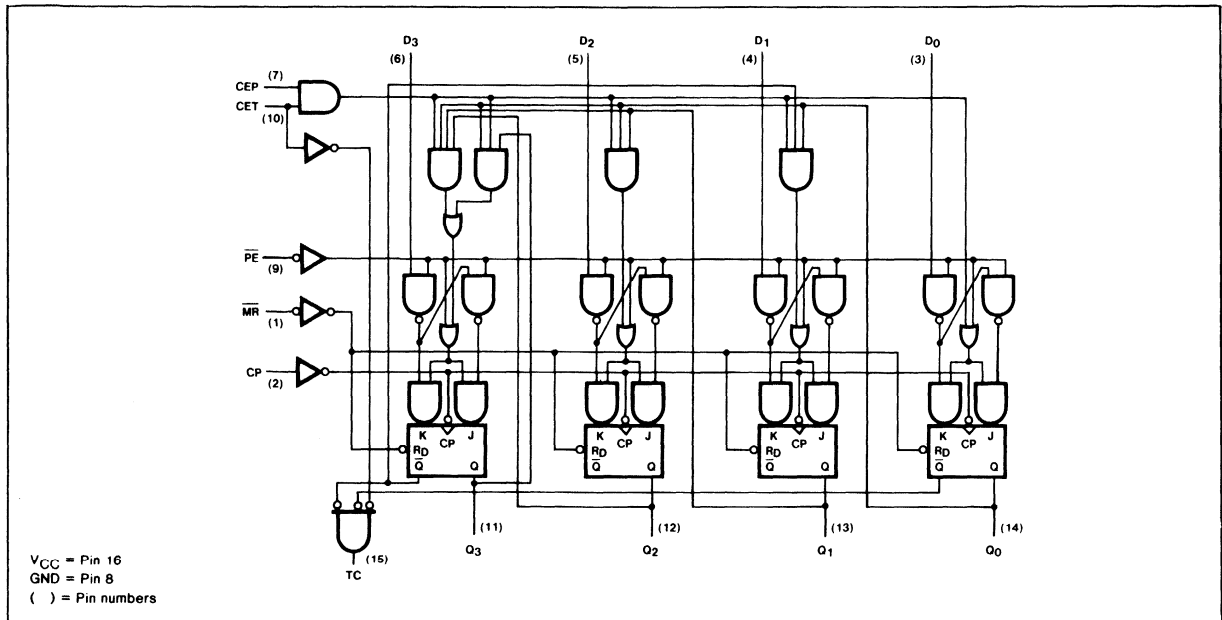
(b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for "160").

(c) The HIGH-to-LOW transition of CEP or CET on the 54/74160 should only occur while CP is HIGH for conventional operation.

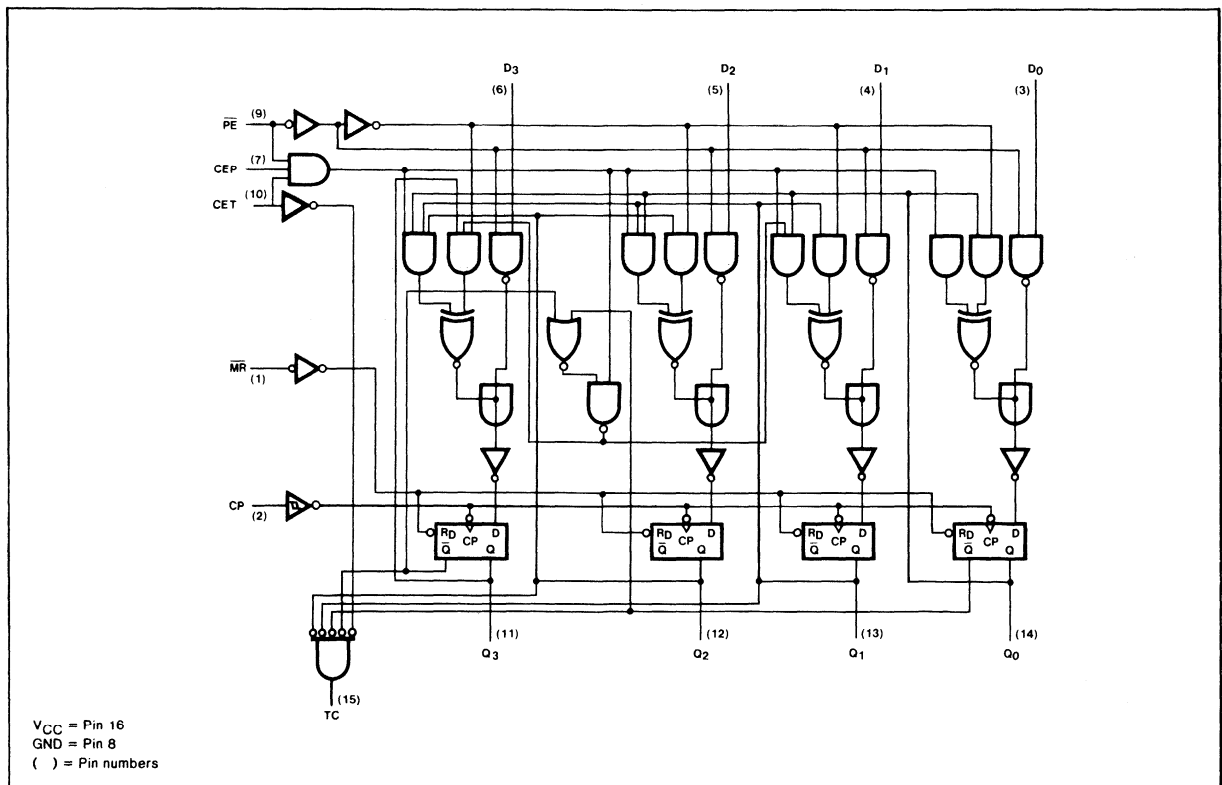
(d) The LOW-to-HIGH transition of \overline{PE} on the 54/74160 should only occur while CP is HIGH for conventional operation.



LOGIC DIAGRAM 54/74160



LOGIC DIAGRAM 54LS/74LS160A



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(e)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CCH} Supply current	V _{CC} = Max	Mil	85				31	mA
	All outputs=HIGH	Com	94				31	mA
I _{CCL} Supply current	V _{CC} = Max	Mil	91				32	mA
	All outputs=LOW	Com	101				32	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2KΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1	25				25		MHz
t _{PLH} Propagation delay t _{PHL} Clock to Terminal Count	Figure 1		35 35				20 27	ns ns
t _{PLH} Propagation delay t _{PHL} Clock to Q outputs	Figure 1, \overline{PE} = HIGH		20 23				21 27	ns ns
t _{PLH} Propagation delay t _{PHL} Clock to Q outputs	Figure 1, \overline{PE} = LOW		25 29				21 27	ns ns
t _{PLH} Propagation delay t _{PHL} CET input to TC output	Figure 2		16 16				16 25	ns ns
t _{PHL} Propagation delay \overline{MR} to Q outputs	Figure 3		38				28	ns

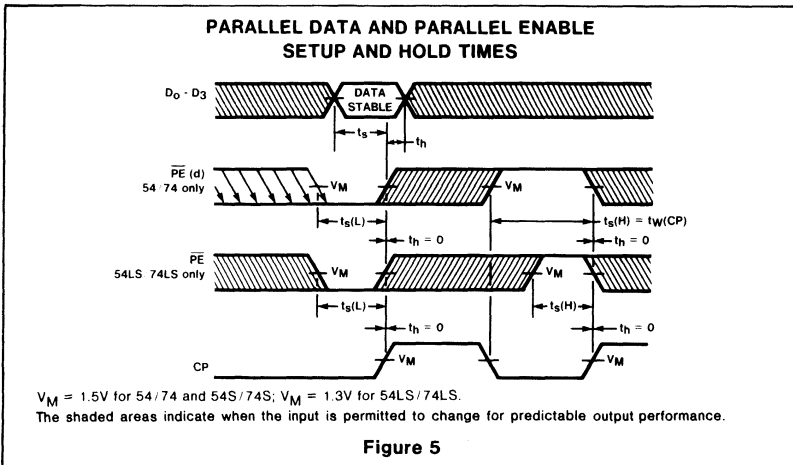
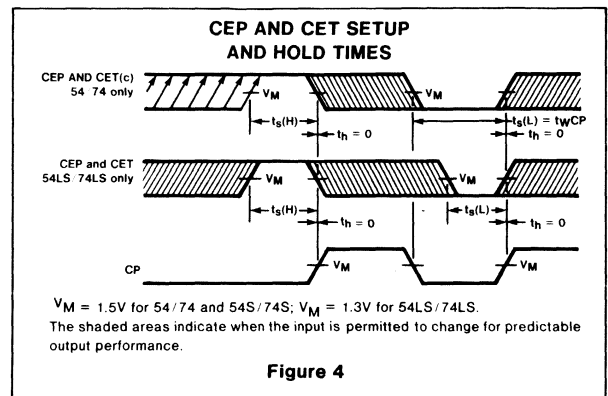
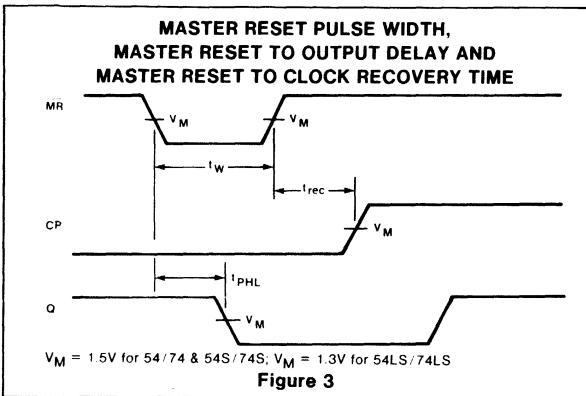
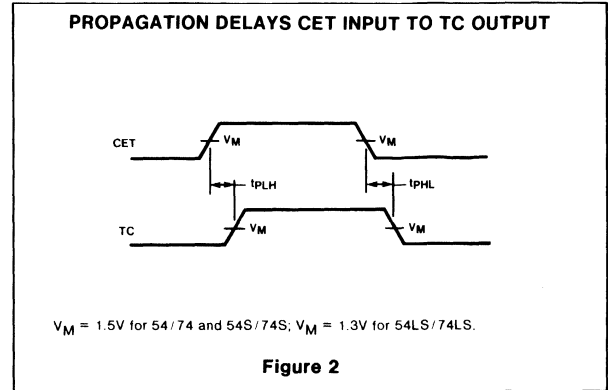
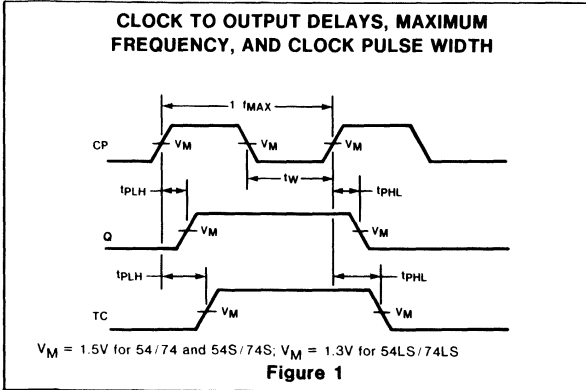
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _{W(L)} Clock pulse width (LOW)	Figure 1	25				25		ns
t _W Master Reset pulse width	Figure 3	20				15		ns
t _s Setup time Data to Clock	Figure 5	20				12		ns
t _h Hold time Data to Clock	Figure 5	0				3.0		ns
t _s Setup time CEP or CET to Clock	Figure 4	20				20		ns
t _h Hold time CEP or CET to Clock	Figure 4	0				0		ns
t _s Setup time \overline{PE} to Clock	Figure 5	25				17		ns
t _h Hold time \overline{PE} to Clock	Figure 5	0				0		ns
t _{rec} Recovery time \overline{MR} to CP	Figure 3	25				15		ns

NOTE

e. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54/74161
54LS/74LS161A

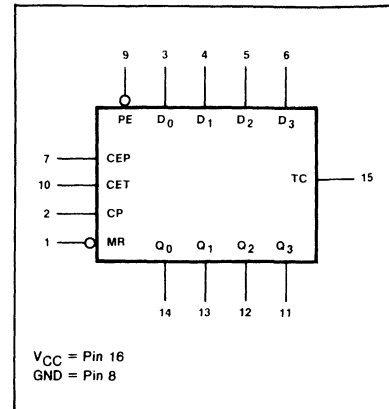
DESCRIPTION

The "161" is a high-speed 4-bit binary counter. The counters are positive edge-triggered, synchronously presettable and are easily cascaded to n-bit synchronous applications without additional gating. A Terminal Count output is provided which detects a count of HHHH. The Master Reset asynchronously clears all flip-flops.

FEATURES

- Synchronous Counting and Loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Hysteresis on clock input (LS161 only)
- All inputs have fan-in of one (LS161 only)

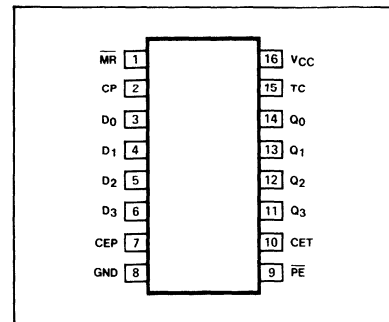
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74161N • N74LS161AN	
Ceramic DIP	N74161F • N74LS161AF	S54161F • S54LS161AF
Flatpak		S54161W • S54LS161AW

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	80 -3.2		20 -0.4
D ₀ -D ₃	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
\overline{PE}	Parallel Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
CEP	Count Enable Parallel input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
CET	Count Enable Trickle input	I _{IH} (μA) I _{IL} (mA)	80 -3.2		20 -0.4
\overline{MR}	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
Q ₀ -Q ₃	Counter outputs	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8(a)
TC	Terminal Count output	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8(a)

NOTE
a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "161" is a synchronous presettable 4-bit binary counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock. The clock input on the LS161 features about 400mV of hysteresis to reduce false triggering caused by noise on the clock line or by slowly rising clock edges.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function for the "161" is asynchronous. A LOW level on the Master Reset (\overline{MR}) input sets all four of the flip-flop outputs LOW, regardless of the levels of the CP, \overline{PE} , CET, and CEP inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET • CEP) and a Terminal Count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This HIGH level TC pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

All "changes" of the Q outputs (except due to the asynchronous Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the Clock input (CP). As long as the setup time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs. However, for conventional operation of the 54/74161 the following transitions should be avoided:

1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is LOW, if the count enables are HIGH at or before the transition.

For some applications, the designer may want to change those inputs while the clock is LOW. In this case, the 54/74161 will behave in a predictable manner. For example:

If \overline{PE} goes HIGH while the clock is LOW, and Count Enable is not active during the re-

maining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW-to-HIGH clock transition will change $Q_0 - Q_3$ to the $D_0 - D_3$ data that existed at the setup time before the rising edge of \overline{PE} .

If \overline{PE} goes HIGH while the clock is LOW, and Count Enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 54/74161 will perform a mixture of counting and loading. On the LOW-to-HIGH clock transition, outputs $Q_0 - Q_3$ will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and are also reloaded with their present value stay constant.

If Count Enable is active (i.e. CEP and CET are HIGH) during some portion of the clock LOW period, and \overline{PE} is HIGH (inactive) during the entire clock LOW period, the subsequent LOW-to-HIGH clock transition will change $Q_0 - Q_3$ to the next count value.

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	\uparrow	X	X	l	l	L	L
	H	\uparrow	X	X	l	h	H	(b)
Count	H	\uparrow	h	h	h(d)	X	count	(b)
Hold (do nothing)	H	X	l(c)	X	h(d)	X	q_n	(b)
	H	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
 \uparrow = LOW-to-HIGH clock transition.

NOTES

- (b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for "161").
- (c) The HIGH-to-LOW transition of CEP or CET on the 54/74161 should only occur while CP is HIGH for conventional operation.
- (d) The LOW to HIGH transition of \overline{PE} on the 54/74161 should only occur while CP is HIGH for conventional operation.

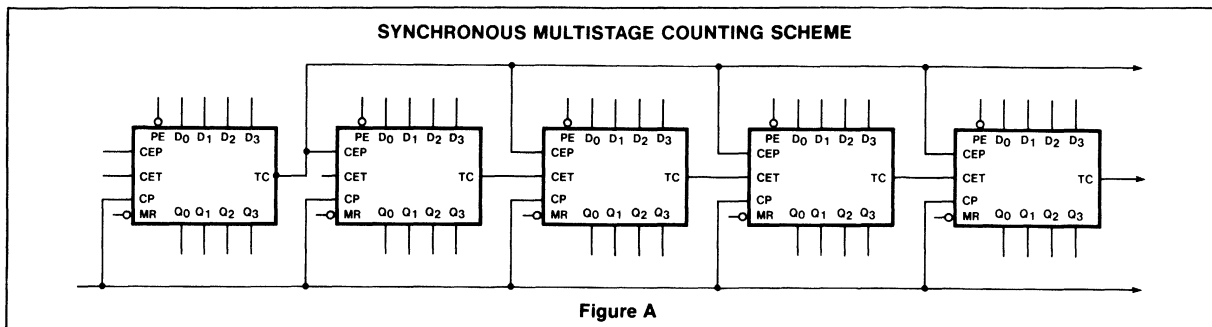
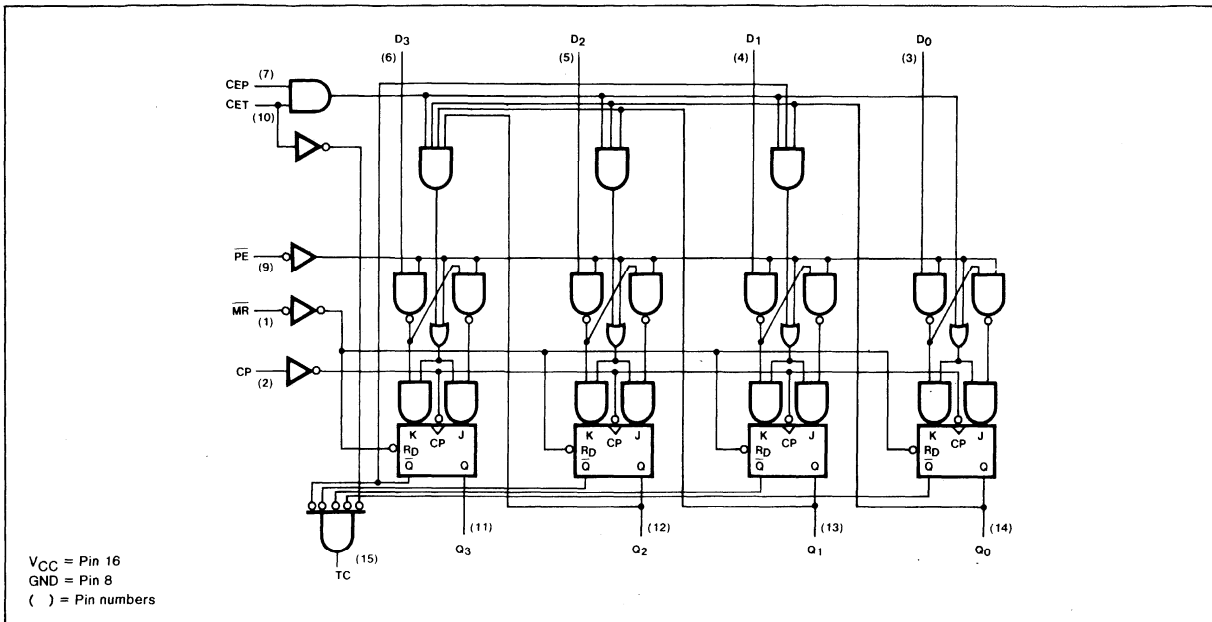
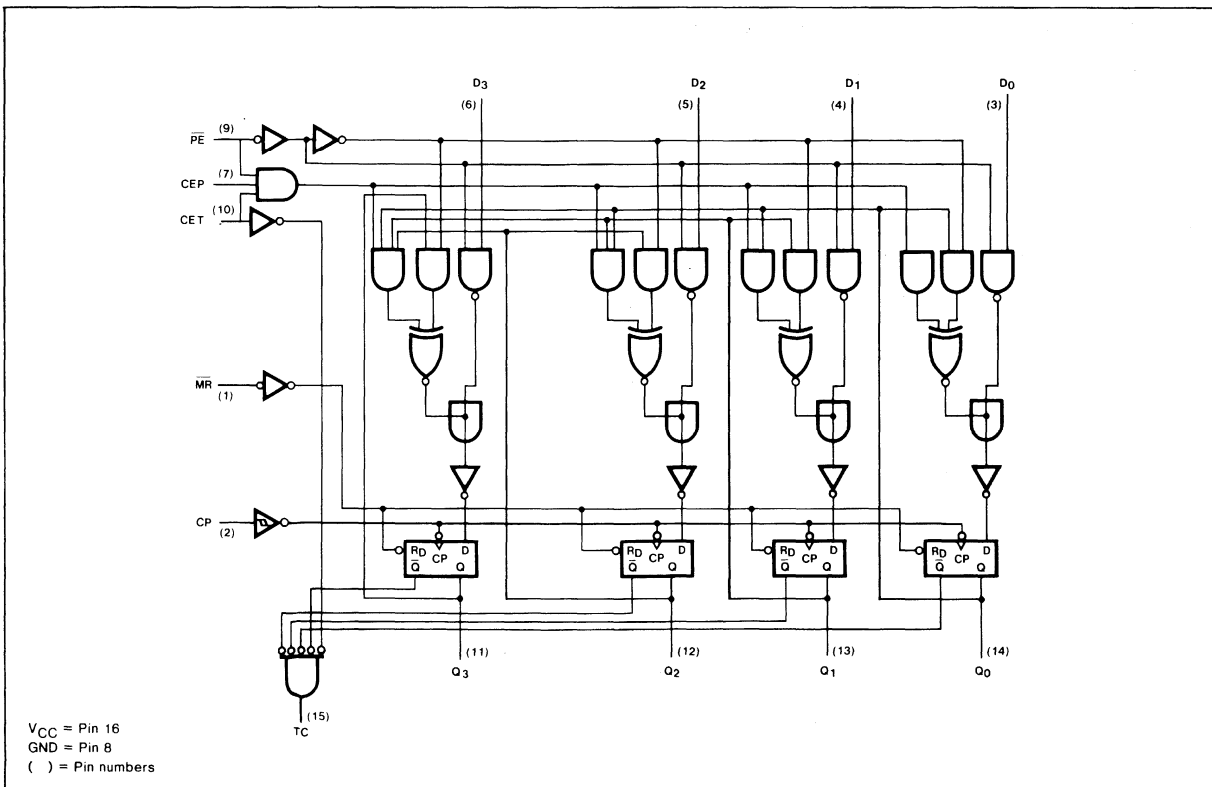


Figure A

LOGIC DIAGRAM 54/74161



LOGIC DIAGRAM 54LS/74LS161A



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(e)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I _{CCH}	Supply current	V _{CC} = Max All outputs=HIGH	Mil	85				31	mA	
			Com	94				31		
I _{CCL}	Supply current	V _{CC} = Max All outputs=LOW	Mil	91				32	mA	
			COm	101				32		

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2KΩ		
				Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Figure 1		25				35		MHz
t _{PLH}	Propagation delay	Figure 1			35				20	ns
t _{PHL}	Clock to Terminal Count				35				27	
t _{PLH}	Propagation delay	Figure 1, \overline{PE} = HIGH			20				21	ns
t _{PHL}	Clock to Q outputs				23				27	
t _{PLH}	Propagation delay	Figure 1, \overline{PE} = LOW			25				21	ns
t _{PHL}	Clock to Q outputs				29				27	
t _{PLH}	Propagation delay	Figure 2			16				16	ns
t _{PHL}	CET input to TC output				16				25	
t _{PHL}	Propagation delay \overline{MR} to Q outputs	Figure 3			38				28	ns

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

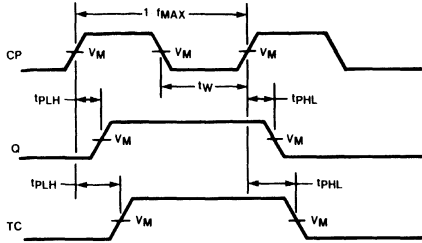
PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
t _{W(L)}	Clock pulse width (LOW)	Figure 1		25				16		ns
t _W	Master Reset pulse width	Figure 3		20				15		ns
t _S	Setup time Data to Clock	Figure 5		20				12		ns
t _H	Hold time Data to Clock	Figure 5		0				3.0		ns
t _S	Setup time CEP or CET to Clock	Figure 4		20				17		ns
t _H	Hold time CEP or CET to Clock	Figure 4		0				0		ns
t _S	Setup time \overline{PE} to Clock	Figure 5		25				17		ns
t _H	Hold time \overline{PE} to Clock	Figure 5		0				0		ns
t _{rec}	Recovery time \overline{MR} to CP	Figure 3		25				15		ns

NOTE

e. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS

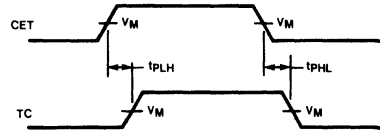
CLOCK TO OUTPUT DELAYS, MAXIMUM FREQUENCY, AND CLOCK PULSE WIDTH



$V_M = 1.5V$ for 54/74 & 54S/74S; $V_M = 1.3V$ for 54LS/74LS

Figure 1

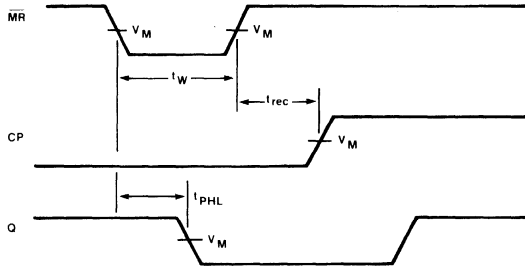
PROPAGATION DELAYS CET INPUT TO TC OUTPUT



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

Figure 2

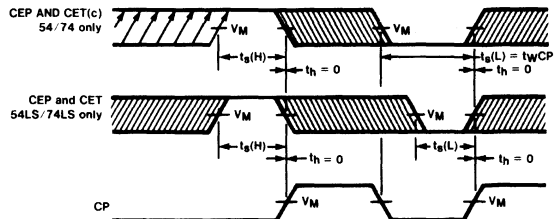
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



$V_M = 1.5V$ for 54/74 & 54S/74S; $V_M = 1.3V$ for 54LS/74LS

Figure 3

CEP AND CET SETUP AND HOLD TIMES

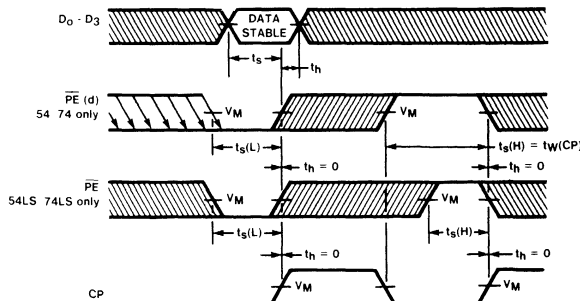


$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 4

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5

54/74162
54LS/74LS162A

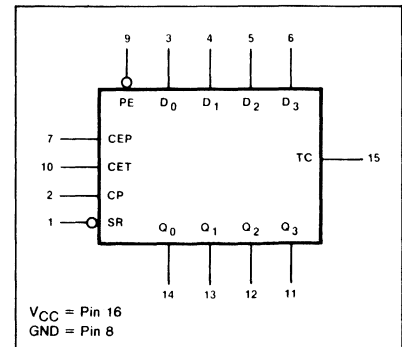
DESCRIPTION

The "162" is a high-speed BCD decade counter. The counters are positive edge-triggered, synchronously presettable and are easily cascaded to n-bit synchronous applications without additional gating. A Terminal Count output is provided which detects a count of HLLH. The Synchronous Reset is edge-triggered. It overrides all control inputs; but is active only during the rising clock edge.

FEATURES

- Synchronous Counting and Loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Hysteresis on clock input (LS162 only)
- All inputs have fan-in of one (LS162 only)

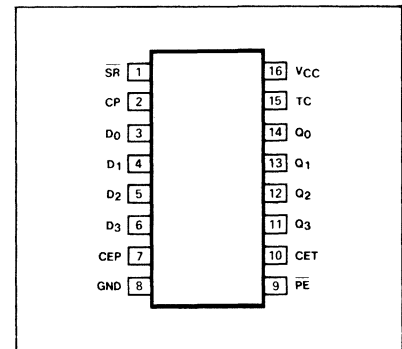
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N74162N	•	N74LS162AN
Ceramic DIP	N74162F	•	N74LS162AF	S54162F • S54LS162AF
Flatpak				S54162W • S54LS162AW

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		20 -0.4
D ₀ -D ₃	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
\overline{PE}	Parallel Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
CEP	Count Enable Parallel input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
CET	Count Enable Trickle input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		20 -0.4
\overline{SR}	Synchronous Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
Q ₀ -Q ₃	Counter outputs	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8 ^(a)
TC	Terminal Count output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "162" is a synchronous presettable BCD decade counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock. The clock input on the LS162 features about 400mV of hysteresis to reduce false triggering caused by noise on the clock line or by slowly rising clock edges.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function for the "162" is synchronous with the clock. The Synchronous Reset (\overline{SR}), when LOW one setup time before the LOW-to-HIGH transition of the clock, overrides the CEP, CET, and \overline{PE} inputs, and causes the outputs to go LOW coincident with the positive clock transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET • CEP) and a Terminal Count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This HIGH level TC pulse is used to enable successive cascaded stages.

See Figure A for the fast synchronous multistage counting connections.

All "changes" of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the Clock input (CP). As long as the setup time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs. However, for conventional operation of the 54/74162 the following transitions should be avoided:

1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is \overline{LOW} , if the count enables and \overline{SR} are HIGH at or before the transition.
3. LOW-to-HIGH transition on the \overline{SR} input when clock is LOW, if the enable and \overline{PE} inputs are HIGH at or before the transition.

For some applications, the designer may want to change those inputs while the clock is LOW. In this case, the 54/74162 will be-

have in a predictable manner. For example:

If \overline{PE} goes HIGH while the clock is LOW, and Count Enable is not active during the remaining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW-to-HIGH clock transition will change $Q_0 - Q_3$ to the $D_0 - D_3$ data that existed at the setup time before the rising edge of \overline{PE} .

If \overline{PE} goes HIGH while the clock is LOW, and Count Enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 54/74162 will perform a mixture of counting and loading. On the LOW-to-HIGH clock transition, outputs $Q_0 - Q_3$ will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and are also reloaded with their present value stay constant.

If Count Enable is active (i.e. CEP and CET are HIGH) during some portion of the clock LOW period, and \overline{PE} is HIGH (inactive) during the entire clock LOW period, the subsequent LOW-to-HIGH clock transition will change $Q_0 - Q_3$ to the next count value.

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{SR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (Clear)	l	\uparrow	X	X	X	X	L	L
Parallel Load	h(d)	\uparrow	X	X	l	l	L	L
	h(d)	\uparrow	X	X	l	h	H	(b)
Count	h(d)	\uparrow	h	h	h(d)	X	count	(b)
Hold (do nothing)	h(d)	X	l(c)	X	h(d)	X	q_n	(b)
	h(d)	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Don't care.

q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.

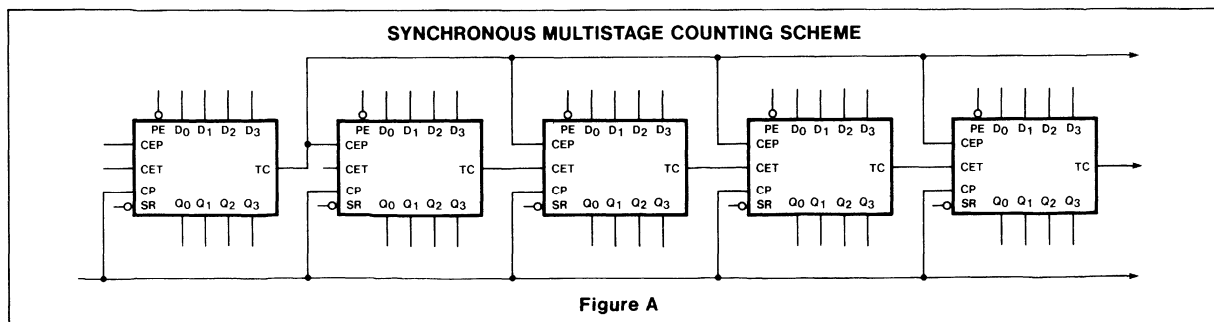
\uparrow = LOW-to-HIGH clock transition.

NOTES

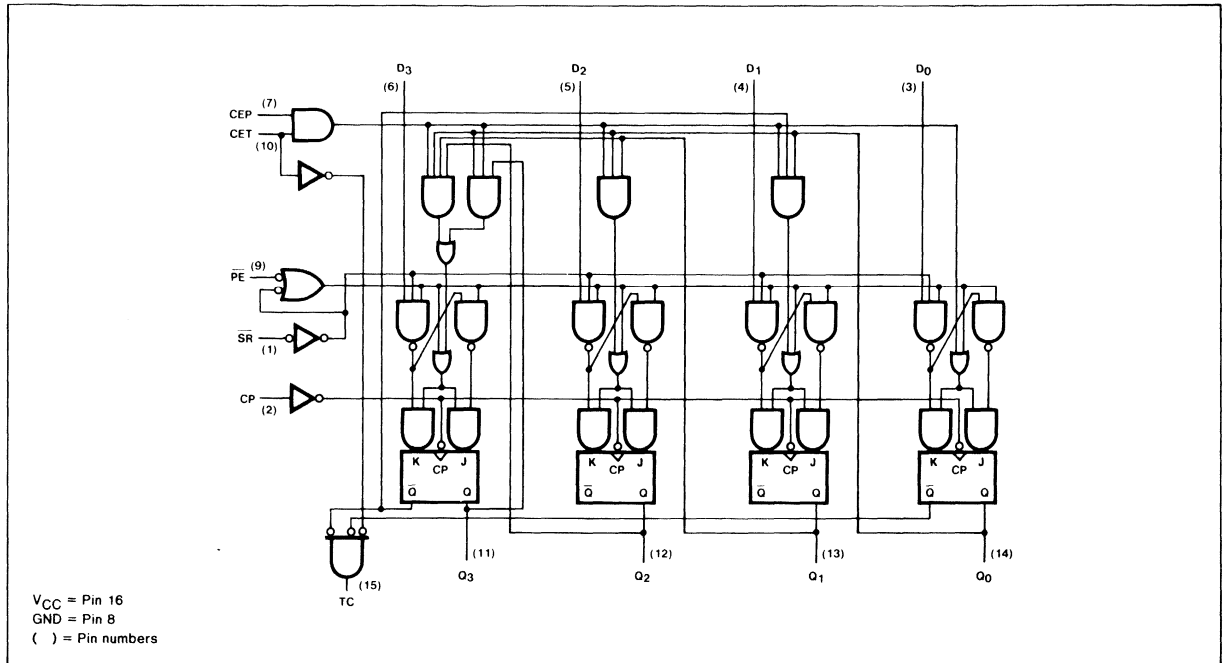
(b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for "162").

(c) The HIGH-to-LOW transition of CEP or CET on the 54/74162 should only occur while CP is HIGH for conventional operation.

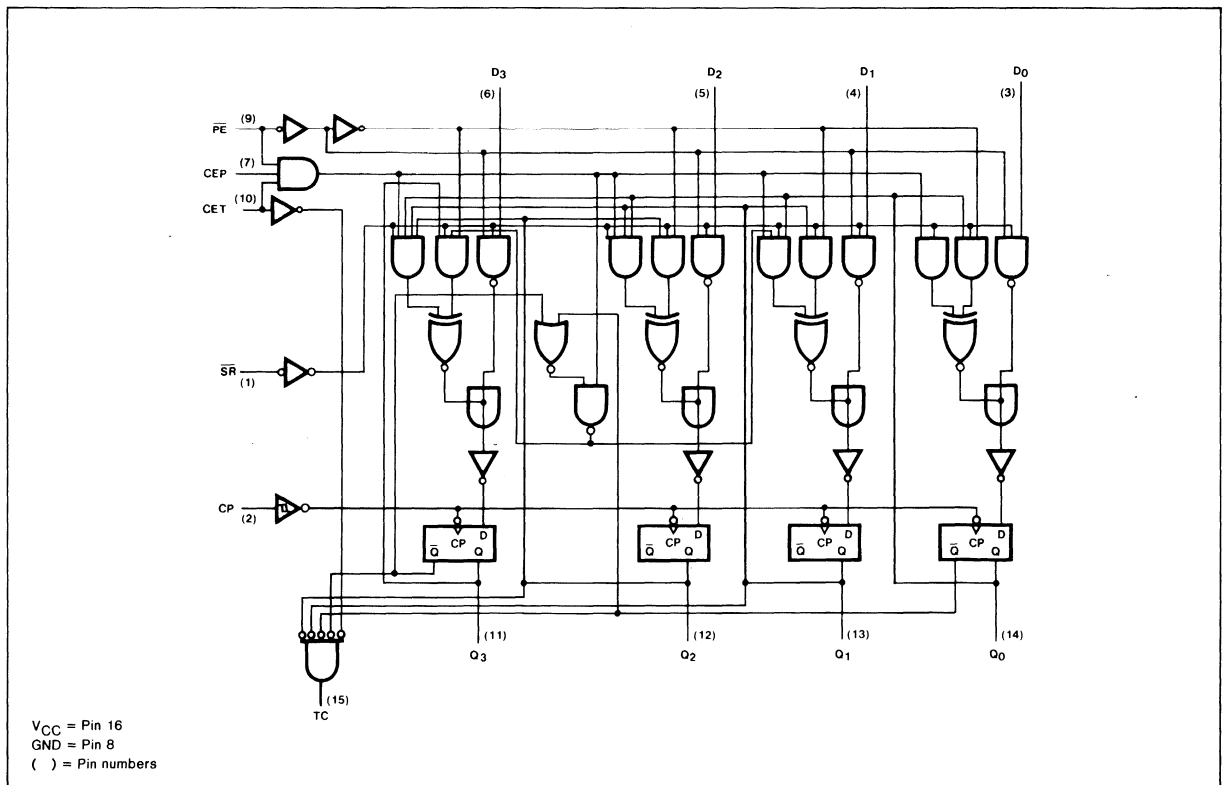
(d) The LOW-to-HIGH transition of \overline{PE} or \overline{SR} on the 54/74162 should only occur while CP is HIGH for conventional operation.



LOGIC DIAGRAM 54/74162



LOGIC DIAGRAM 54LS/74LS162A



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(e)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I _{CCH}	Supply current	V _{CC} = Max All outputs = HIGH	Mil	85				31	mA	
			Com	94				31	mA	
I _{CCL}	Supply current	V _{CC} = Max All outputs = LOW	Mil	91				32	mA	
			Com	101				32	mA	

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2KΩ		
				Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Figure 1		25				25		MHz
t _{PLH}	Propagation delay	Figure 1			35				20	ns
t _{PHL}	Clock to Terminal Count				35				27	ns
t _{PLH}	Propagation delay	Figure 1, \overline{PE} = HIGH			20				21	ns
t _{PHL}	Clock to Q outputs				23				27	ns
t _{PLH}	Propagation delay	Figure 1, \overline{PE} = LOW			25				21	ns
t _{PHL}	Clock to Q outputs				29				27	ns
t _{PLH}	Propagation delay	Figure 2			16				16	ns
t _{PHL}	CET input to TC output				16				25	ns

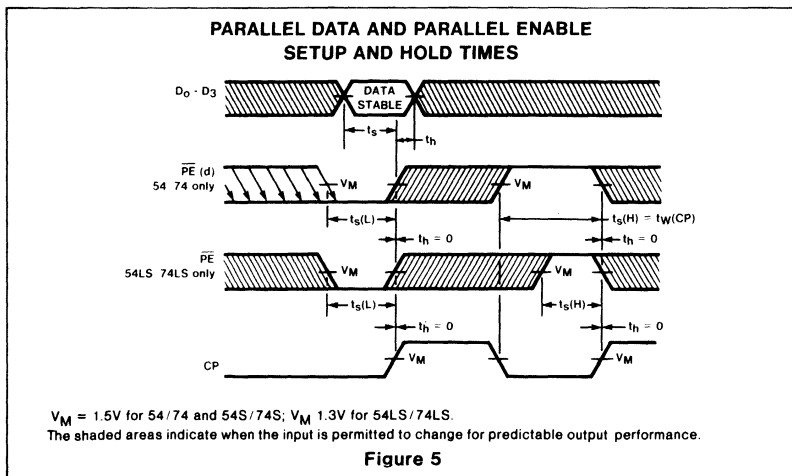
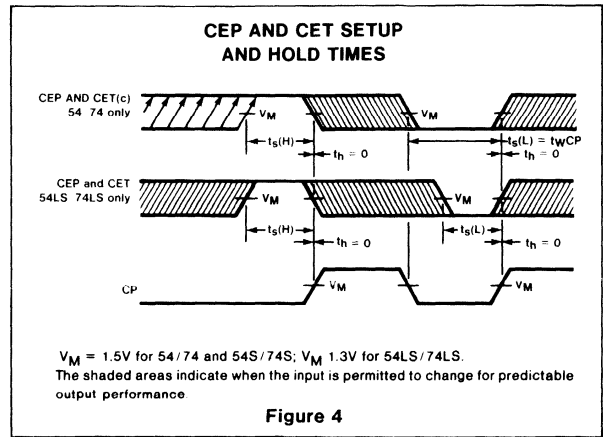
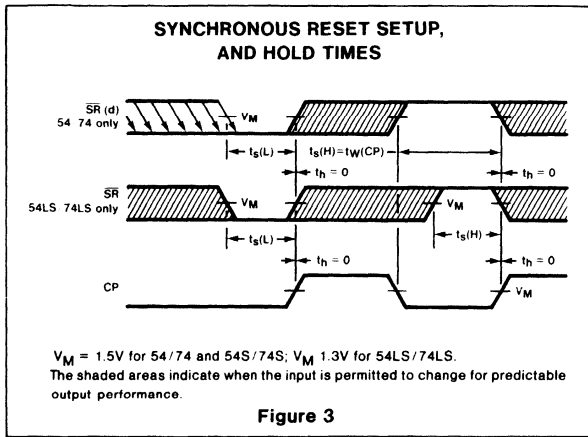
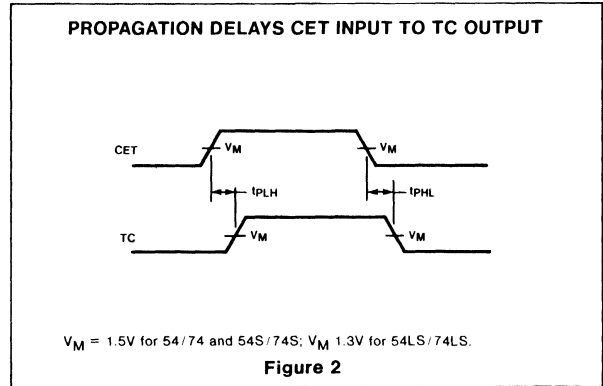
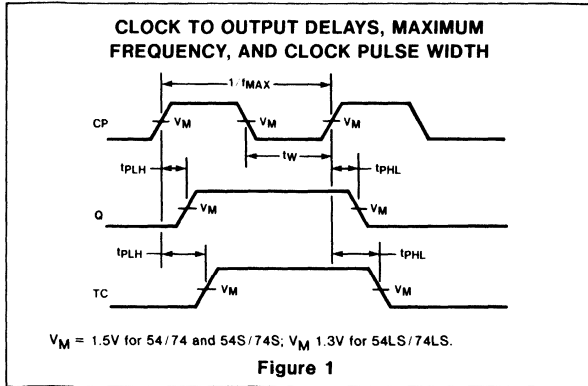
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
t _{W(L)}	Clock pulse width (LOW)	Figure 1		25				25		ns
t _W	Master Reset pulse width	Figure 3		20				15		ns
t _s	Setup time Data to Clock	Figure 5		20				12		ns
t _h	Hold time Data to Clock	Figure 5		0				3.0		ns
t _s	Setup time CEP or CET to Clock	Figure 4		20				20		ns
t _h	Hold time CEP or CET to Clock	Figure 4		0				0		ns
t _s	Setup time \overline{PE} to Clock	Figure 5		25				17		ns
t _h	Hold time \overline{PE} to Clock	Figure 5		0				0		ns
t _s	Setup time \overline{SR} to Clock	Figure 3		20				20		ns
t _h	Hold time \overline{SR} to Clock	Figure 3		0				0		ns

NOTE

e. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54/74163
54LS/74LS163A

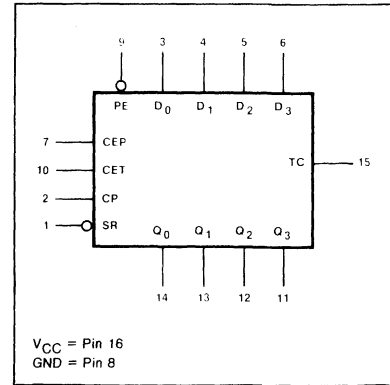
DESCRIPTION

The "163" is a high-speed 4-bit binary counter. The counters are positive edge-triggered, synchronously presettable and are easily cascaded to n-bit synchronous applications without additional gating. A Terminal Count output is provided which detects a count of HHHH. The Synchronous Reset is edge-triggered. It overrides all other control inputs; but is active only during the rising clock edge.

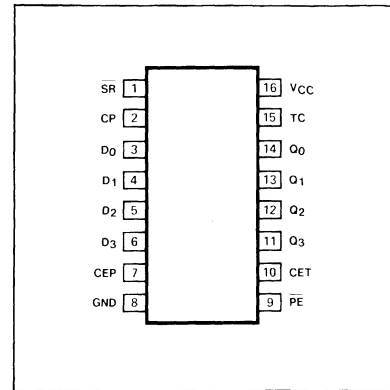
FEATURES

- Synchronous Counting and Loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Hysteresis on clock input (LS163 only)
- All inputs have fan-in of one (LS163 only)

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C		MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C	
	Plastic DIP	N74163N	• N74LS163AN	
Ceramic DIP	N74163F	• N74LS163AF	S54163F	• S54LS163AF
Flatpak			S54163W	• S54LS163AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	80 -3.2		20 -0.4
D ₀ -D ₃	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
\overline{PE}	Parallel Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
CEP	Count Enable Parallel input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
CET	Count Enable Trickle input	I _{IH} (μA) I _{IL} (mA)	80 -3.2		20 -0.4
\overline{SR}	Synchronous Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
Q ₀ -Q ₃	Counter outputs	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8(a)
TC	Terminal Count output	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "163" is a synchronous presettable 4-bit binary counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock. The clock input on the LS163 features about 400mV of hysteresis to reduce false triggering caused by noise on the clock line or by slowly rising clock edges.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function for the "163" is synchronous with the clock. The Synchronous Reset (\overline{SR}), when LOW one setup time before the LOW-to-HIGH transition of the clock, overrides the CEP, CET, and \overline{PE} inputs, and causes the outputs to go LOW coincident with the positive clock transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET • CEP) and a Terminal Count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This HIGH level TC pulse is used to enable successive cascaded stages.

See Figure A for the fast synchronous multistage counting connections.

All "changes" of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the Clock input (CP). As long as the setup time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs. However, for conventional operation of the 54/74163 the following transitions should be avoided:

1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is LOW, if the count enables and \overline{SR} are HIGH at or before the transition.
3. LOW-to-HIGH transition on the \overline{SR} input when the clock is LOW, if the enable and \overline{PE} inputs are HIGH at or before the transition.

For some applications, the designer may want to change those inputs while the clock is LOW. In this case, the 54/74163 will be-

have in a predictable manner. For example:

If \overline{PE} goes HIGH while the clock is LOW, and Count Enable is not active during the remaining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW-to-HIGH clock transition will change $Q_0 - Q_3$ to the $D_0 - D_3$ data that existed at the setup time before the rising edge of \overline{PE} .

If \overline{PE} goes HIGH while the clock is LOW, and Count Enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 54/74163 will perform a mixture of counting and loading. On the LOW-to-HIGH clock transition, outputs $Q_0 - Q_3$ will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and are also reloaded with their present value stay constant.

If Count Enable is active (i.e. CEP and CET are HIGH) during some portion of the clock LOW period, and \overline{PE} is HIGH (inactive) during the entire clock LOW period, the subsequent LOW-to-HIGH clock transition will change $Q_0 - Q_3$ to the next count value.

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{SR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (Clear)	1	↑	X	X	X	X	L	L
Parallel Load	h(d)	↑	X	X	1	1	L	L
	h(d)	↑	X	X	1	h	H	(b)
Count	h(d)	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	h(d)	X	l(c)	X	h(d)	X	q_n	(b)
	h(d)	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
 ↑ = LOW-to-HIGH clock transition.

NOTES

- (b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for "163").
- (c) The HIGH-to-LOW transition of CEP or CET on the 54/74163 should only occur while CP is HIGH for conventional operation.
- (d) The LOW-to-HIGH transition of \overline{PE} or \overline{SR} on the 54/74163 should only occur while CP is HIGH for conventional operation.

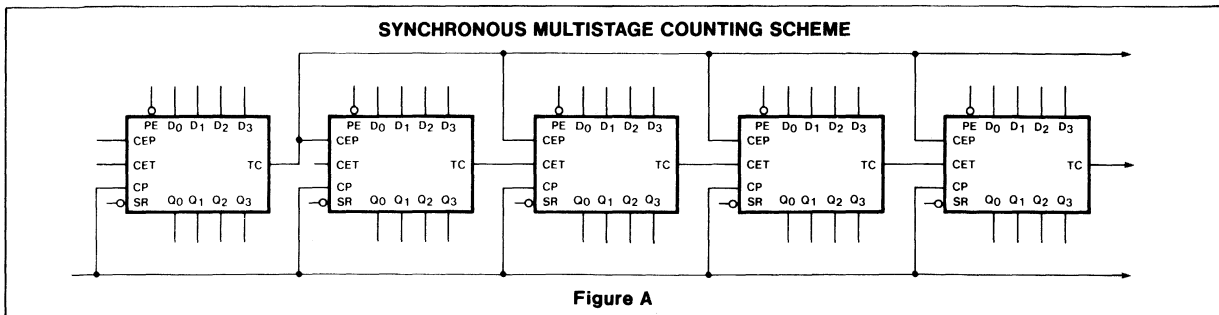
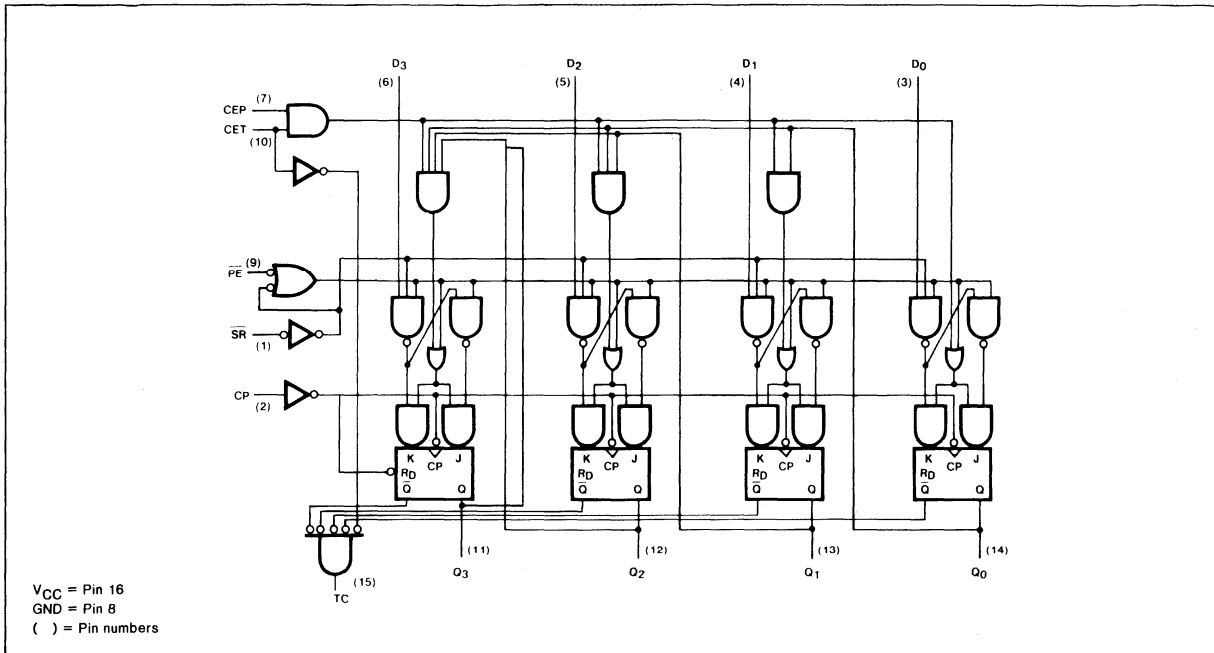
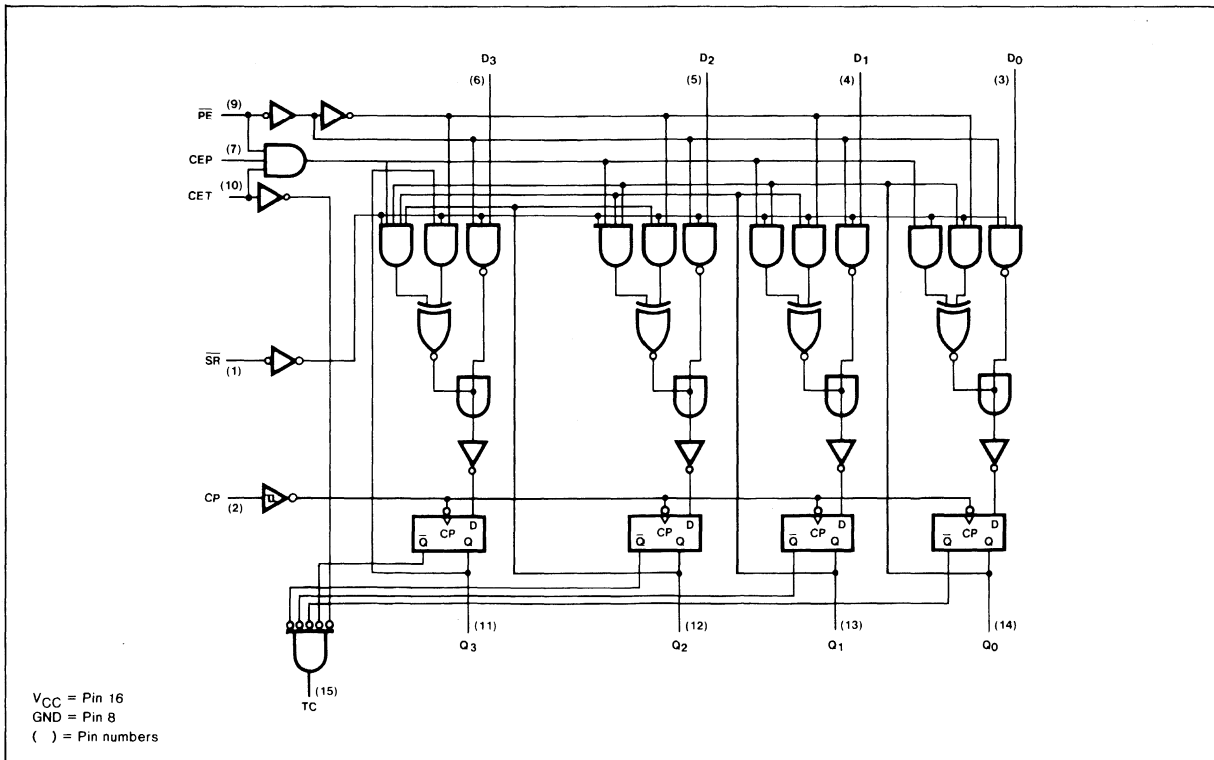


Figure A

LOGIC DIAGRAM 54/74163



LOGIC DIAGRAM 54LS/74LS163A



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(e)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I _{CCH}	Supply current	V _{CC} = Max All outputs=HIGH	Mil	85				31	mA	
			Com	94				31	mA	
I _{CCL}	Supply current	V _{CC} = Max All outputs=LOW	Mil	91				32	mA	
			COm	101				32	mA	

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

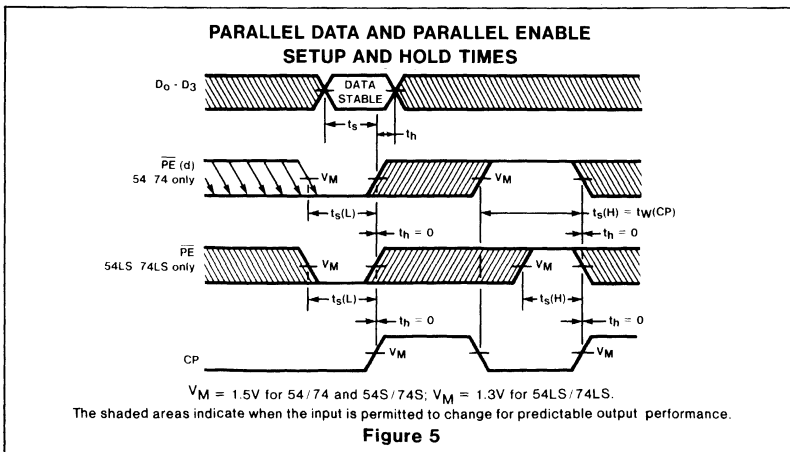
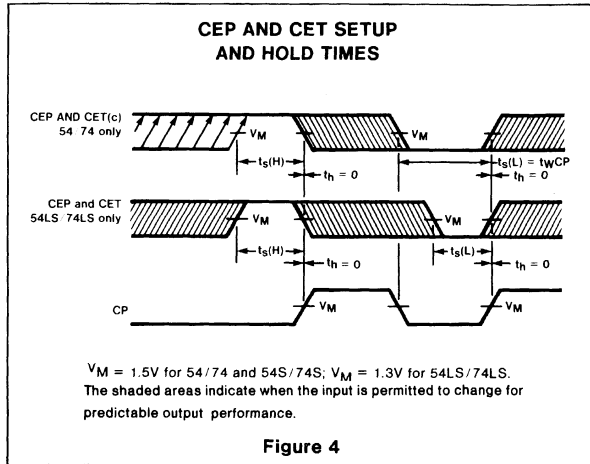
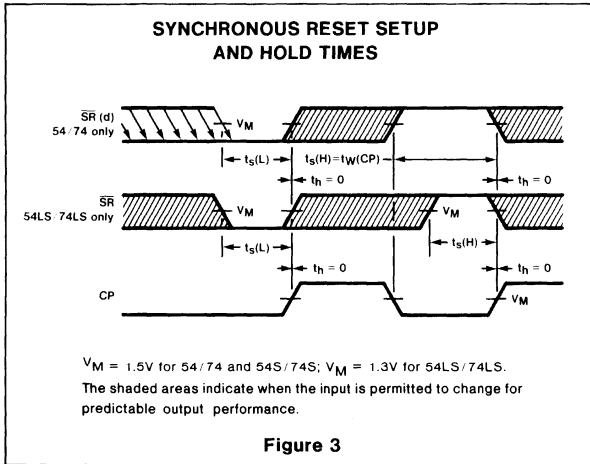
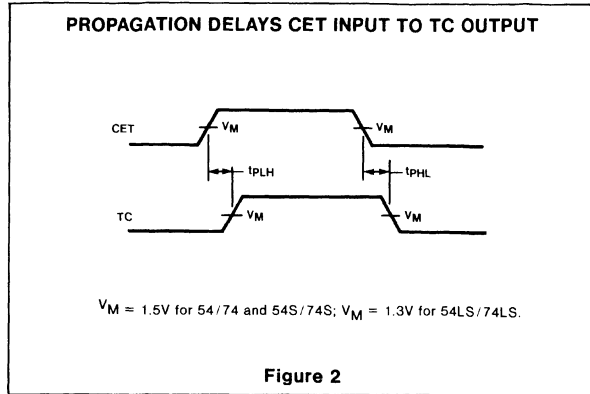
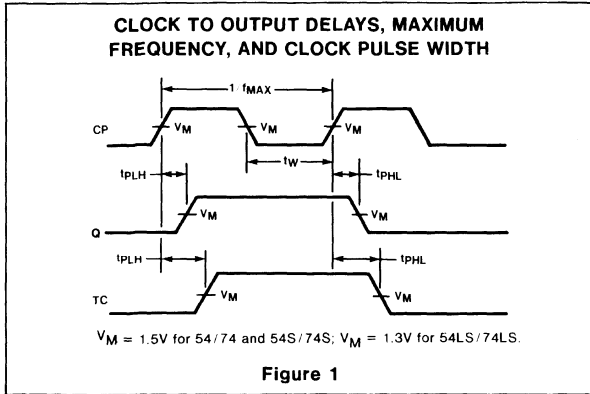
PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				C _L =15pF R _L =400Ω				C _L =15pF R _L =2kΩ		
				Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Figure 1		25				35		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to Terminal Count	Figure 1			35 35				20 27	ns ns
t _{PLH} t _{PHL}	Propagation delay Clock to Q outputs	Figure 1, \overline{PE} = HIGH			20 23				21 27	ns ns
t _{PLH} t _{PHL}	Propagation delay Clock to Q outputs	Figure 1, \overline{PE} = LOW			25 29				21 27	ns ns
t _{PLH} t _{PHL}	Propagation delay CET input to TC output	Figure 2			16 16				16 25	ns ns

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
t _{W(L)}	Clock pulse width (LOW)	Figure 1		25				16		ns
t _W	Master Reset pulse width	Figure 3		20				15		ns
t _s	Setup time Data to Clock	Figure 5		20				12		ns
t _h	Hold time Data to Clock	Figure 5		0				3.0		ns
t _s	Setup time CEP or CET to Clock	Figure 4		20				17		ns
t _h	Hold time CEP or CET to Clock	Figure 4		0				0		ns
t _s	Setup time \overline{PE} to Clock	Figure 5		25				17		ns
t _h	Hold time \overline{PE} to Clock	Figure 5		0				0		ns
t _s	Setup time \overline{SR} to Clock	Figure 3		20 ^(d)				20		ns
t _h	Hold time \overline{SR} to Clock	Figure 3		0				0		ns

NOTE
e. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54/74164
54LS/74LS164

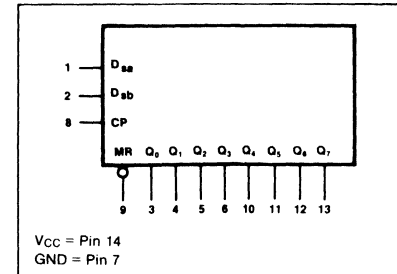
DESCRIPTION

The "164" is a high speed 8-Bit Serial-In, Parallel-Out Shift Register featuring gated serial inputs and an asynchronous Master Reset. Serial data is entered through a 2-Input AND gate synchronously with the LOW to HIGH clock transition. An asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock, is featured.

FEATURES

- Gated serial data inputs
- Typical shift frequency of 36MHz
- Asynchronous master reset
- Fully buffered clock and data inputs

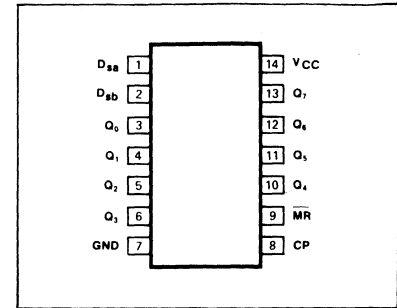
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to +70°C	V _{CC} = 5V ± 10%; T _A = -55°C to +125°C
Plastic DIP	N74164N • N74LS164N	
Ceramic DIP	N74164F • N74LS164F	S54164F • S54LS164F
Flatpak		S54LS164W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D _{sa} , D _{sb}	Serial Data inputs	I _{IH} (μA)	40		20
		I _{IL} (mA)	-1.6		-0.4
CP	Clock (Active HIGH going edge) input	I _{IH} (μA)	40		20
		I _{IL} (mA)	-1.6		-0.4
MR	Master Reset (Active LOW) input	I _{IH} (μA)	40		20
		I _{IL} (mA)	-1.6		-0.4
Q ₀ - Q ₇	Register outputs	I _{OH} (μA)	-400		-400
		I _{OL} (mA)	8.0		4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "164" is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

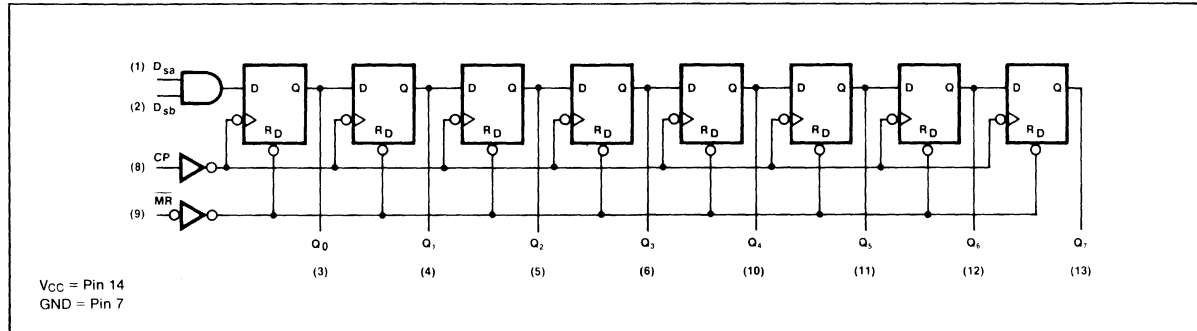
Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two data inputs ($D_{sa} \bullet D_{sb}$) that existed one setup time before the rising clock edge. A LOW level on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	MR	CP	D_{sa}	D_{sb}	Q_0	Q_1	-	Q_7
Reset (Clear)	L	X	X	X	L	L	-	L
Shift	H	↑	l	l	L	q_0	-	q_6
	H	↑	l	h	L	q_0	-	q_6
	H	↑	h	l	L	q_0	-	q_6
	H	↑	h	h	H	q_0	-	q_6

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 x = Don't care.
 ↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max		
I_{os} Output short circuit current	$V_{cc} = \text{Max}$ $V_{out} = 0V$	Mil	-10	-27.5			-15	-100	mA
		Com	-9	-27.5			-15	-100	mA
I_{cc} Supply current	$V_{cc} = \text{Max}$		54				27	mA	

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

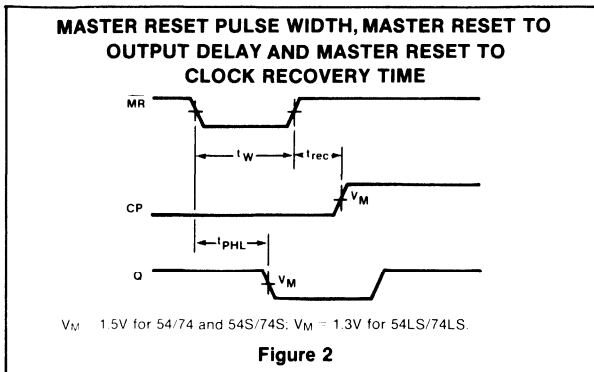
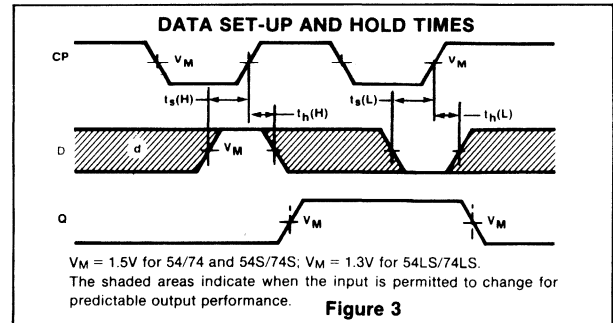
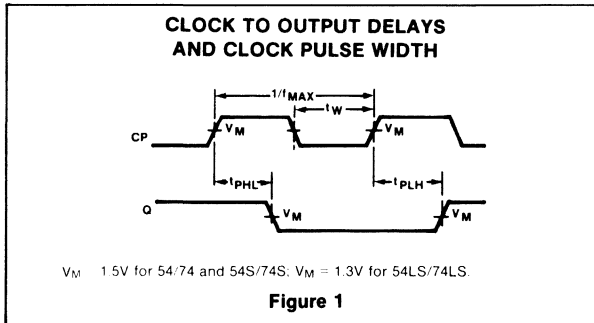
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 800\Omega$				$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum shift frequency	Figure 1	25				25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Figure 1		27 32				27 32	ns ns
t_{PHL} Propagation delay MR to output	Figure 2		36				36	ns
t_{PLH} Propagation delay t_{PHL} Clock to output	Figure 1	$C_L = 50\text{pF}$ for these parameters	30					ns
t_{PHL} Propagation delay MR to output			Figure 2	42				ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w Clock pulse width	Figure 1	20				20		ns
t_w MR pulse width	Figure 2	20				20		ns
t_s Setup time data to clock	Figure 3	15				15		ns
t_h Hold time data to clock	Figure 3	5.0				5.0		ns
t_{rec} MR to clock recovery time	Figure 2	30				20		ns

AC WAVEFORMS



54/74165

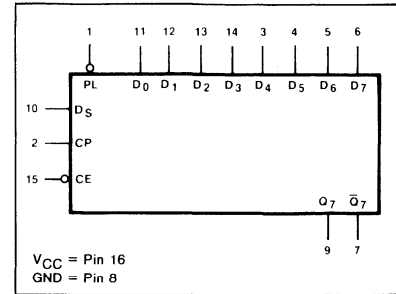
DESCRIPTION

The "165" is an 8-bit Serial-in or Parallel-in Shift Register with complementary serial outputs primarily used as a parallel to serial converter. The Serial Data entry is synchronous with the LOW-to-HIGH transition of the Clock, but the Parallel Load is asynchronous overriding the Clock and loading the eight Parallel Data bits directly into the register. An active LOW Clock Enable is also provided.

FEATURES

- Asynchronous 8-bit parallel load
- Synchronous serial input
- Clock Enable for "do nothing" mode
- See 74166 for fully synchronous operation

LOGIC SYMBOL

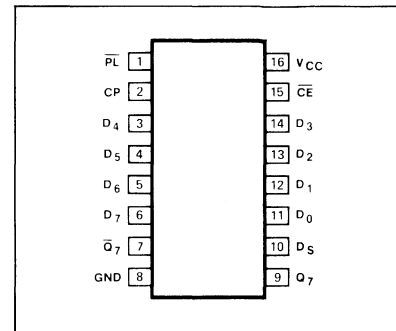


V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74165N	
Ceramic DIP	N74165F	S54165F
Flatpak		S54165W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D _S	Serial Data input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
D ₀ - D ₇	Parallel Data input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
\overline{PL}	Parallel Load (Active LOW) input	I _{IH} (μA) I _{IL} (mA)	80 -3.2		
CP	Clock (Active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
\overline{CE}	Clock Enable (Active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
Q ₇ and \overline{Q}_7	Complementary outputs	I _{OH} (μA) I _{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "165" is an 8-bit parallel load or Serial-in shift register with complementary serial outputs (Q_7 and \bar{Q}_7) available from the last stage. When the Parallel Load (\overline{PL}) input is LOW, parallel data from the $D_0 - D_7$ inputs are loaded into the register asynchronously. When the \overline{PL} input is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$ etc.) with each positive-going clock transition. This feature allows parallel to serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

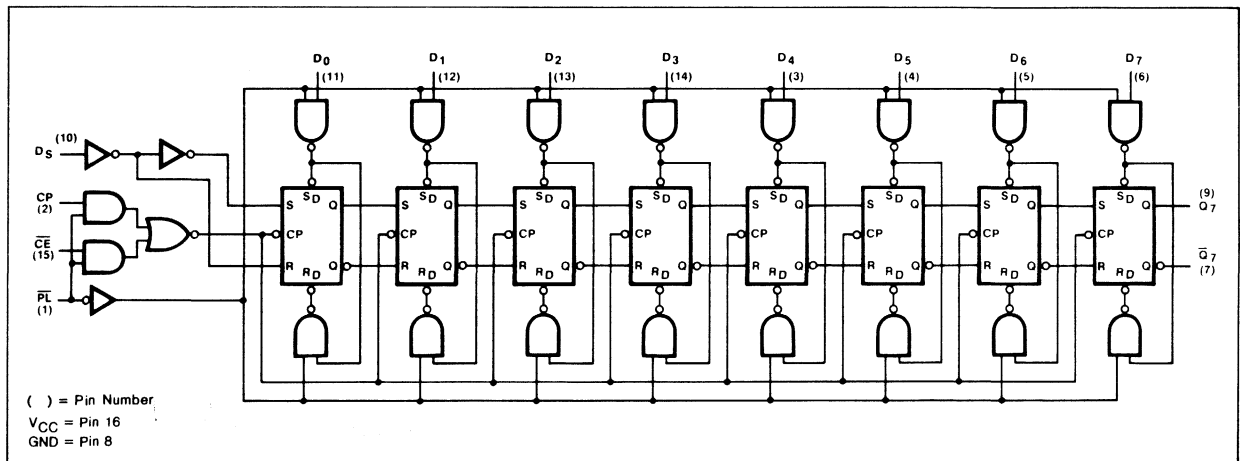
The Clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of \overline{CE} input should only take place while the CP is HIGH for predictable operation. Also, the CP and \overline{CE} inputs should be LOW before the LOW-to-HIGH transition of \overline{PL} to prevent shifting the data when \overline{PL} is released.

MODE SELECT - FUNCTION TABLE

OPERATING MODES	INPUTS					Q _n REGISTER		OUTPUTS	
	\overline{PL}	\overline{CE}	CP	D _S	D ₀ - D ₇	Q ₀	Q ₁ - Q ₆	Q ₇	\bar{Q}_7
Parallel Load	L	X	X	X	L	L	L - L	L	H
	L	X	X	X	H	H	H - H	H	L
Serial Shift	H	L	↑	l	X	L	q ₀ - q ₅	q ₆	\bar{q}_6
	H	L	↑	h	X	H	q ₀ - q ₅	q ₆	\bar{q}_6
Hold "Do Nothing"	H	H	X	X	X	q ₀	q ₁ - q ₆	q ₇	\bar{q}_7

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		63					mA

NOTE
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

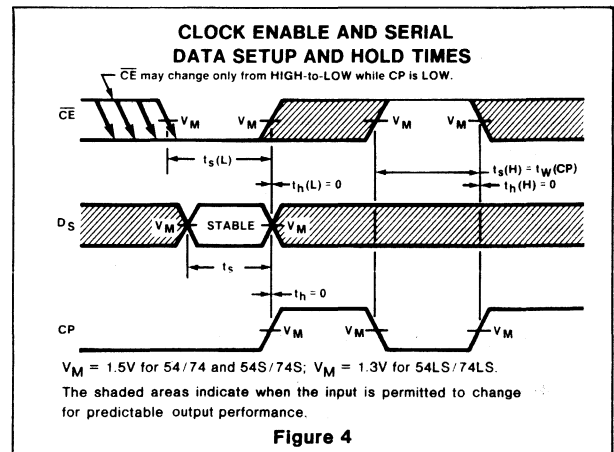
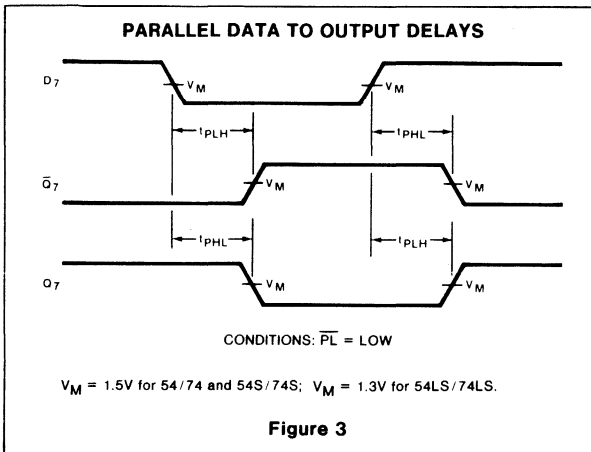
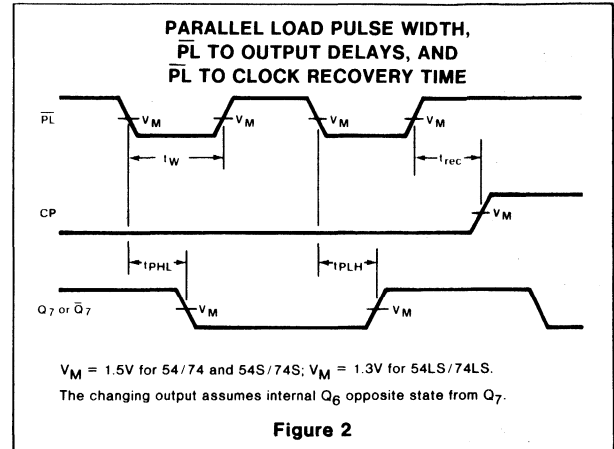
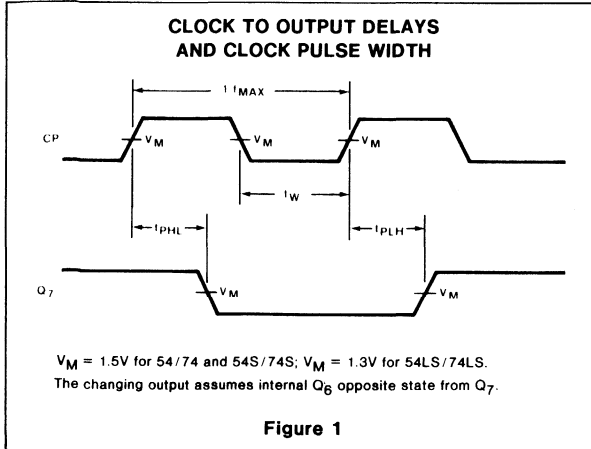
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum shift frequency	Figure 1	20						MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Figure 1		24 31					ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{PL}}$ to output	Figure 2		31 40					ns ns
t_{PLH} Propagation delay t_{PHL} D_7 to Q_7	Figure 3		17 36					ns ns
t_{PLH} Propagation delay t_{PHL} D_7 to \overline{Q}_7	Figure 3		27 27					ns ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w Clock pulse width	Figure 1	25						ns
t_w $\overline{\text{PL}}$ pulse width	Figure 2	15						ns
t_s Setup time D_S to clock	Figure 4	20						ns
t_h Hold time D_S to clock	Figure 4	0						ns
$t_s(L)$ Setup time LOW $\overline{\text{CE}}$ to clock	Figure 4	30						ns
t_h Hold time $\overline{\text{CE}}$ to clock	Figure 4	0						ns
t_{rec} $\overline{\text{PL}}$ Recovery time to clock	Figure 2	10						ns

AC WAVEFORMS



54/74166

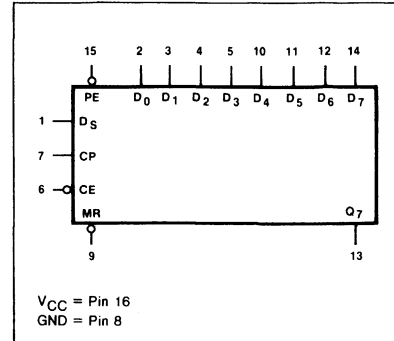
DESCRIPTION

The "166" is a fully synchronous 8-bit serial or parallel-in, serial-out shift register. The Data and Parallel Enable inputs are edge triggered, and must be stable only one setup time before the LOW-to-HIGH transition of the clock. A gated clock is provided allowing one input to be used as a Clock Enable. The Master Reset is asynchronous and clears the register when LOW.

FEATURES

- Synchronous parallel to serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous Master Reset
- See "165" for asynchronous parallel data load

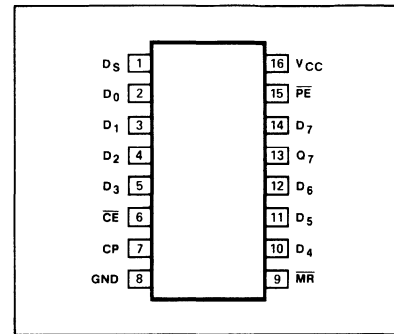
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74166N	
Ceramic DIP	N74166F	S54166F
Flatpak		S54166W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
DS	Serial Data input	I_{IH} (μA)	40		
		I_{IL} (mA)	-1.6		
D0-D7	Parallel Data inputs	I_{IH} (μA)	40		
		I_{IL} (mA)	-1.6		
\overline{PE}	Parallel Enable (Active LOW) input	I_{IH} (μA)	40		
		I_{IL} (mA)	-1.6		
CP	Clock (Active HIGH going edge) input	I_{IH} (μA)	40		
		I_{IL} (mA)	-1.6		
\overline{CE}	Clock Enable (Active LOW) input	I_{IH} (μA)	40		
		I_{IL} (mA)	-1.6		
Q7	Register output	I_{OH} (μA)	-800		
		I_{OL} (mA)	16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "166" is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable (\overline{PE}) input. When the \overline{PE} is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When \overline{PE} is HIGH, data is entered into internal bit position Q_0 from Serial Data input (D_S), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$ etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_S input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of \overline{CE} input should only take place while the CP is HIGH for predictable operation.

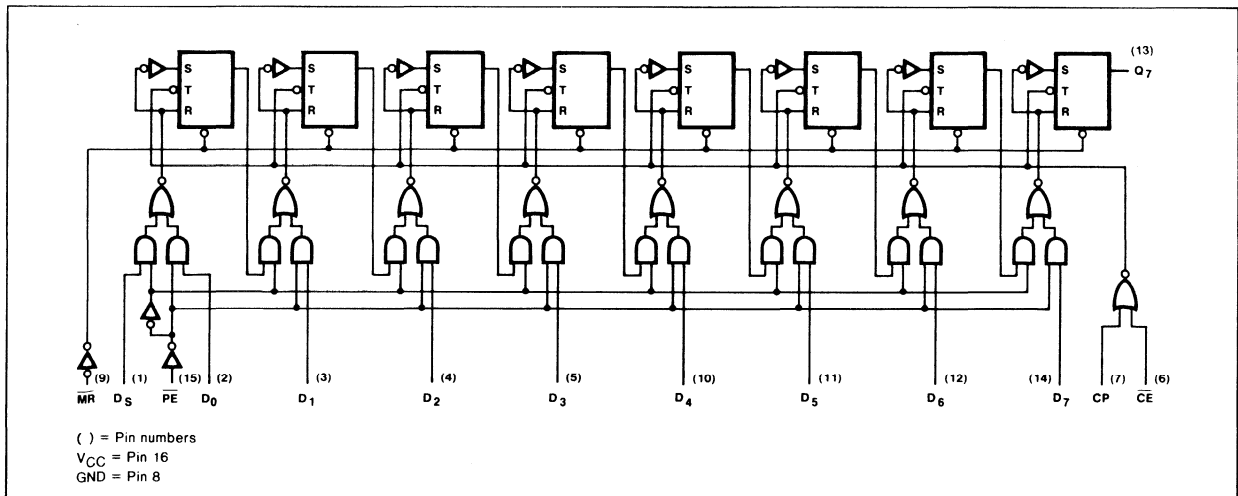
A LOW on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

MODE SELECT-FUNCTION TABLE

OPERATING MODES	INPUTS					Q _n REGISTER		OUTPUT
	\overline{PE}	\overline{CE}	CP	D _S	D ₀ -D ₇	Q ₀	Q ₁ -Q ₆	Q ₇
Parallel Load	l	l	↑	X	l - l	L	L - L	L
	l	l	↑	X	h - h	H	H - H	H
Serial Shift	h	l	↑	l	X - X	L	q ₀ - q ₅	q ₆
	h	l	↑	h	X - X	H	q ₀ - q ₅	q ₆
Hold (do nothing)	X	h	X	X	X - X	q ₀	q ₁ - q ₆	q ₇

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 q_n = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW to HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil	104					mA
		Com	116					mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω						
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1	25						MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Figure 1		26 30					ns ns
t _{PHL} Propagation delay \overline{MR} to output	Figure 2		35					ns

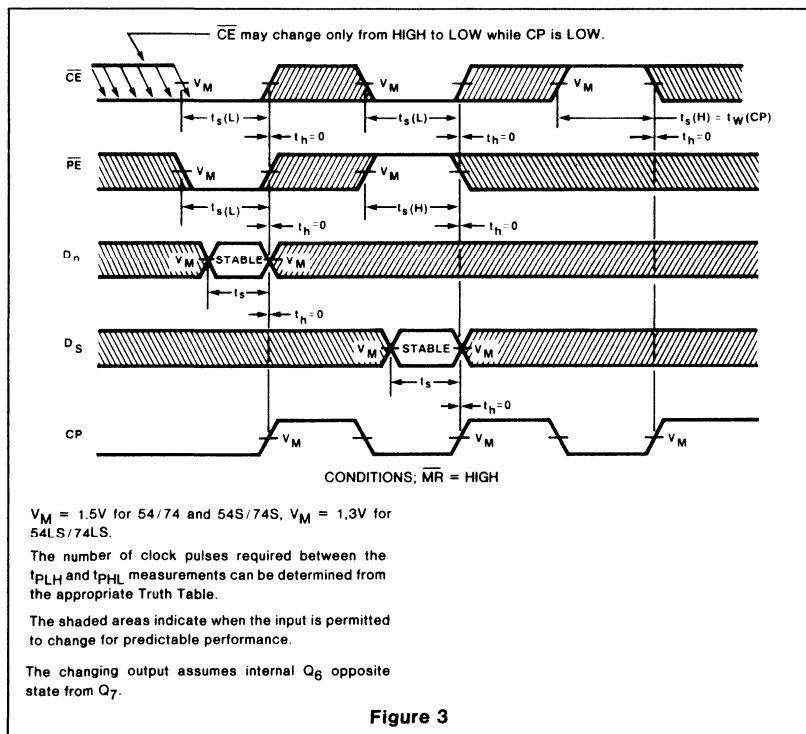
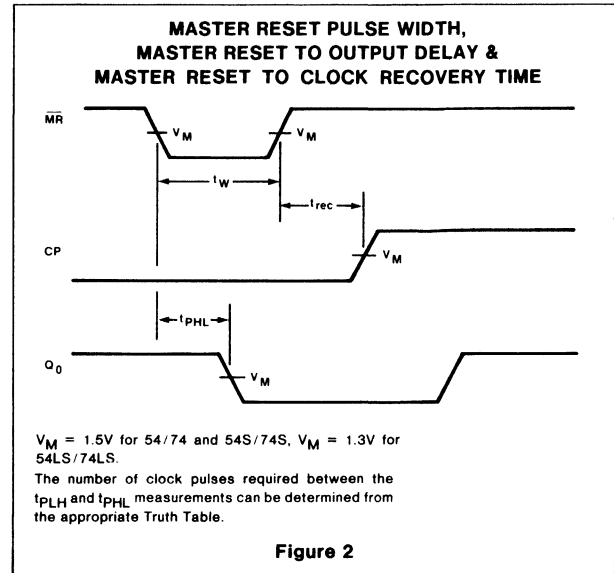
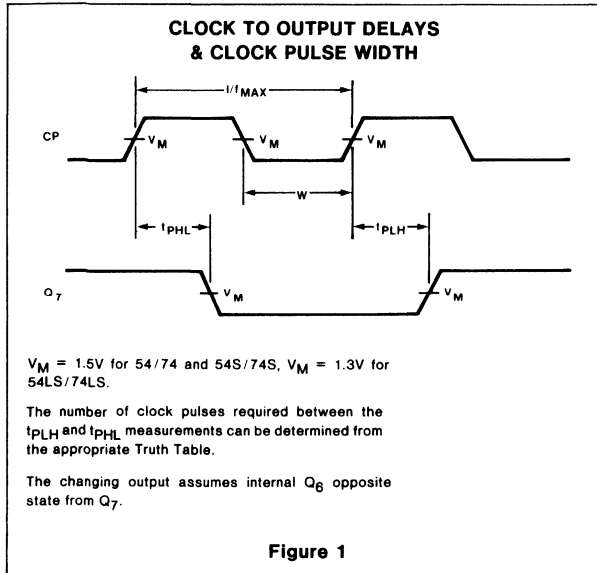
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _W Clock pulse width	Figure 1	20						ns
t _W \overline{MR} pulse width	Figure 2	20						ns
t _S Setup time data to clock	Figure 3	20						ns
t _H Hold time data to clock	Figure 3	0						ns
t _S Setup time \overline{CE} to clock	Figure 3	30						ns
t _H Hold time \overline{CE} to clock	Figure 3	0						ns
t _S Setup time \overline{PE} to clock	Figure 3	30						ns
t _H Hold time \overline{PE} to clock	Figure 3	0						ns
t _{rec} Recovery time \overline{MR} to clock	Figure 2	30						ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54LS/74LS168A (Preliminary data)

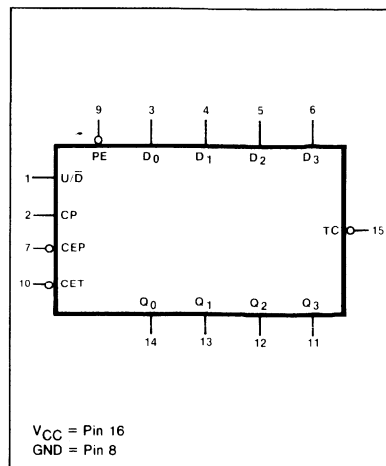
DESCRIPTION

The "168" is a synchronous 4-stage BCD decade (8, 4, 2, 1) UP/DOWN counter featuring preset capability for programmable operation, carry look-ahead for easy cascading and U/ \bar{D} input to control the direction of counting. All state changes while counting or loading are initiated by the LOW-to-HIGH transition of the clock.

FEATURES

- Synchronous counting and loading
- UP/DOWN counting
- BCD Decade counter
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock

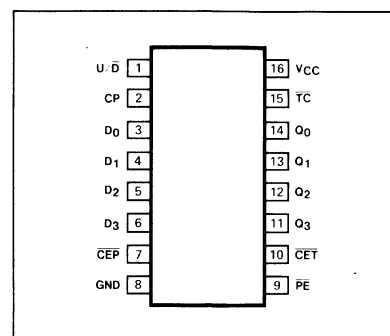
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N74LS168AN	
Ceramic DIP	N74LS168AF	S54LS168AF
Flatpak		S54LS168AW

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
$\bar{P}E$	Parallel Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			40 -0.8
$\bar{C}EP$	Count Enable Parallel (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
$\bar{C}ET$	Count Enable Trickle (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
U/ \bar{D}	UP/DOWN Control Input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D ₀ -D ₃	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q ₀ -Q ₃	Counter outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)
$\bar{T}C$	Terminal Count (active LOW) output	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "168" is a synchronous presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be present to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (PE) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the Up/Down (U/D) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs ($\overline{CET} \bullet \overline{CEP}$) and a Terminal Count (TC) output. Both count enable inputs must be LOW to count. The \overline{CET}

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/D	CEP	CET	PE	D _n	Q _n	TC
Parallel Load	↑	X	X	X	l	l	L	(b)
	↑	X	X	X	l	h	H	(b)
Count Up	↑	h	l	l	h	X	Count Up	(b)
Count Down	↑	l	l	l	h	X	Count Down	(b)
Hold (do nothing)	↑	X	h	X	h	X	q _n	(b)
	↑	X	X	h	h	X	q _n	H

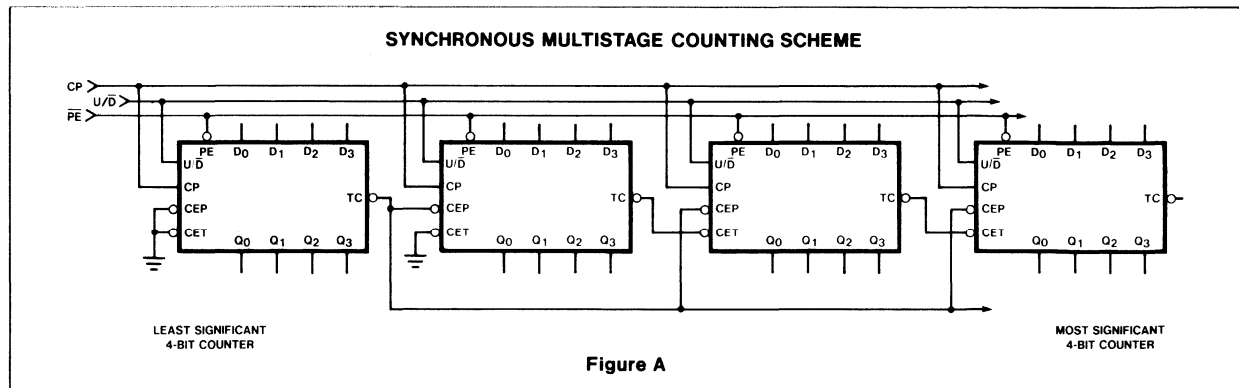
H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
 ↑ = LOW-to-HIGH clock transition.

NOTE

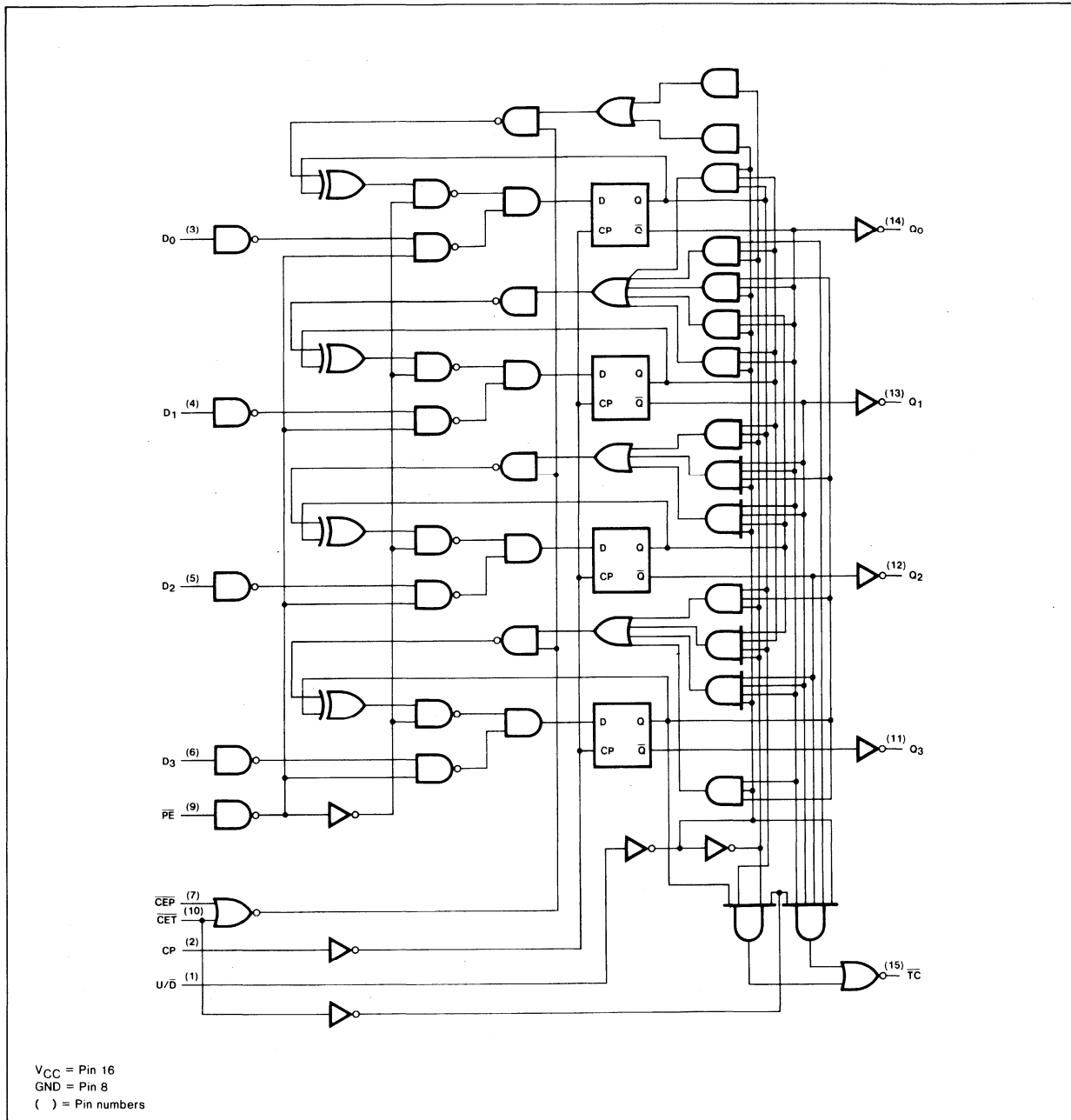
b. The TC is LOW when \overline{CET} is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH), and Terminal Count Down is (LLLL).

input is fed forward to enable the TC output. The TC output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the

Q₀ output. This LOW level TC pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						34	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1					25		MHz
t _{PLH} Propagation delay t _{PHL} Clock to Q output	Figure 1 Figure 1						20 23	ns ns
t _{PLH} Propagation delay t _{PHL} Clock to \overline{TC}	Figure 1						35 35	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CET} to \overline{TC}	Figure 2						14 14	ns ns
t _{PLH} Propagation delay t _{PHL} U/ \overline{D} control to \overline{TC}	Figure 3						25 29	ns ns

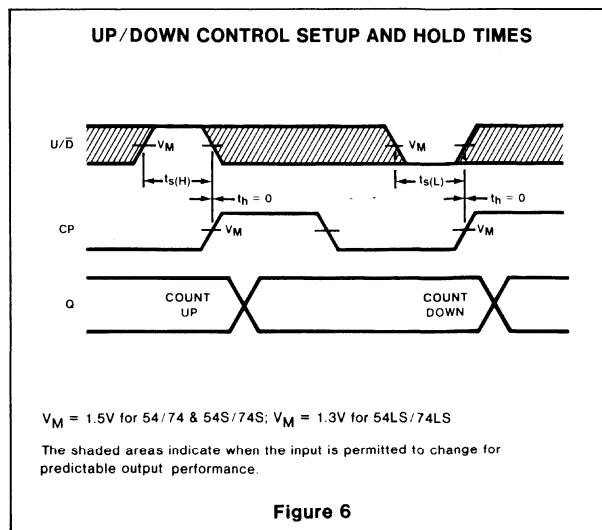
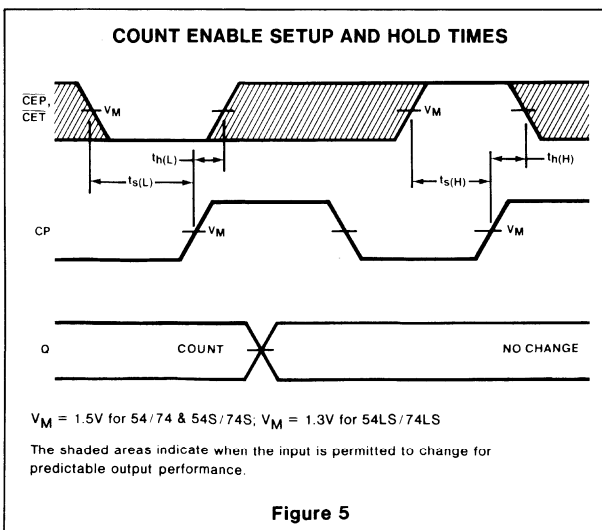
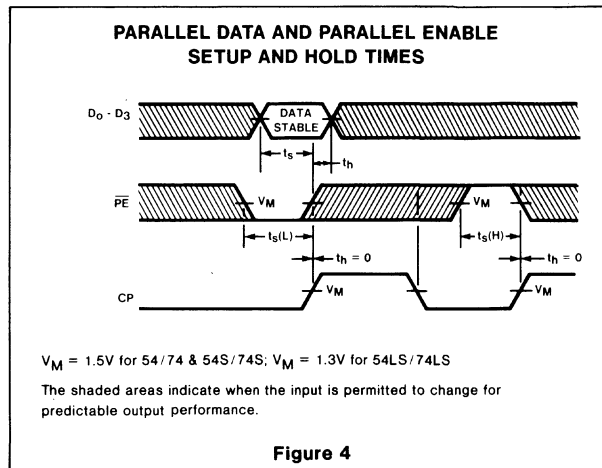
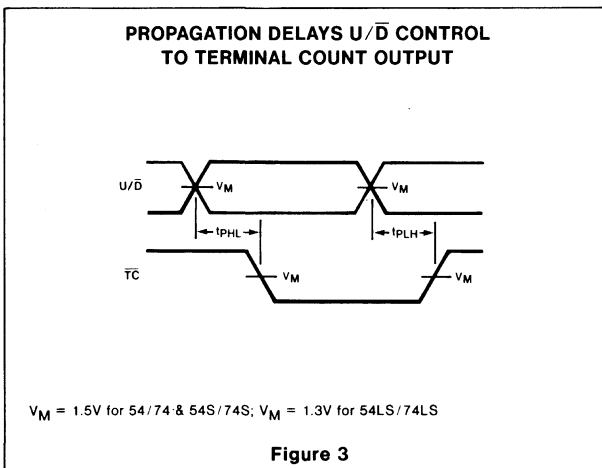
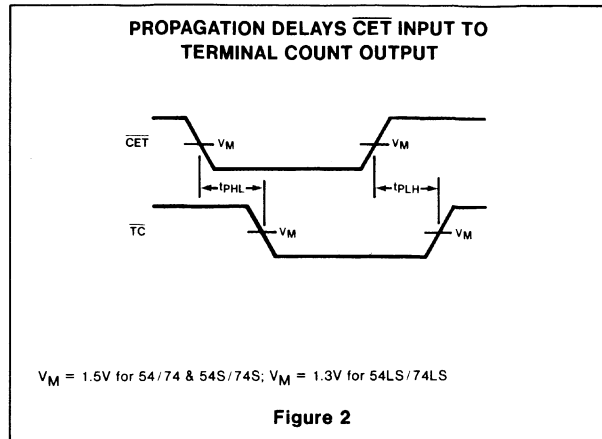
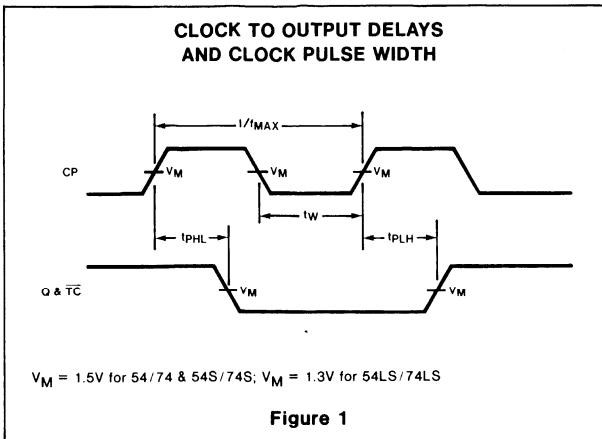
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Clock pulse width	Figure 1					20		ns
t _s Setup time data to clock	Figure 4					20		ns
t _h Hold time data to clock	Figure 4					0		ns
t _s Setup time \overline{PE} to clock	Figure 4					25		ns
t _h Hold time \overline{PE} to clock	Figure 4					0		ns
t _s Setup time \overline{CEP} & \overline{CET} to clock	Figure 5					20		ns
t _h Hold time \overline{CEP} & \overline{CET} to clock	Figure 5					0		ns
t _s Setup time U/ \overline{D} to clock	Figure 6					30		ns
t _h Hold time U/ \overline{D} to clock	Figure 6					0		ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54LS/74LS169A (Preliminary data)

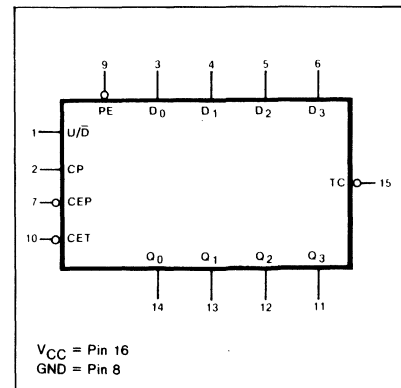
DESCRIPTION

The "169" is a synchronous 4-stage Modulo 16 binary UP/DOWN counter featuring preset capability for programmable operation, carry look-ahead for easy cascading and U/D input to control the direction of counting. All state changes while counting or loading are initiated by the LOW-to-HIGH transition of the clock.

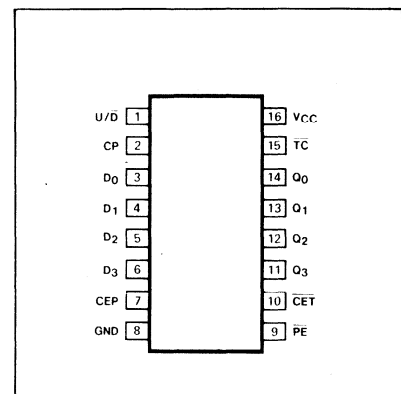
FEATURES

- Synchronous counting and loading
- UP/DOWN counting
- Modulo 16 Binary counter
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N74LS169AN	
Ceramic DIP	N74LS169AF	S54LS169AF
Flatpak		S54LS169AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{PE}	Parallel Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			40 -0.8
\overline{CEP}	Count Enable Parallel (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{CET}	Count Enable Trickle (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
U/ \overline{D}	UP/DOWN Control input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D ₀ -D ₃	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q ₀ -Q ₃	Counter Outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)
\overline{TC}	Terminal Count (active LOW) output	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "169" is a synchronous presettable Modulo 16 binary UP/DOWN counter featuring an internal carry look-ahead for applications in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the UP/DOWN (U/\overline{D}) input, a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs ($\overline{CET} = \overline{CEP}$) and a Terminal Count (\overline{TC}) output. Both count enable inputs must be LOW to count. The \overline{CET} input is fed forward to enable the \overline{TC} output. The \overline{TC} output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level \overline{TC} pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/D	\overline{CEP}	\overline{CET}	\overline{PE}	D_n	Q_n	\overline{TC}
Parallel Load	↑	X	X	X	l	l	L	(b)
	↑	X	X	X	l	h	H	(b)
Count Up	↑	h	l	l	h	X	Count Up	(b)
Count Down	↑	l	l	l	h	X	Count Down	(b)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(b)
	↑	X	X	h	h	X	q_n	H

- H = HIGH voltage level steady state
- L = LOW voltage level steady state
- h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
- l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
- X = Don't care
- q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
- ↑ = LOW-to-HIGH clock transition

NOTE

- b. The \overline{TC} is LOW when \overline{CET} is LOW and the counter is at Terminal Count. Terminal Count up is (HHHH) and Terminal Count Down is (LLLL).

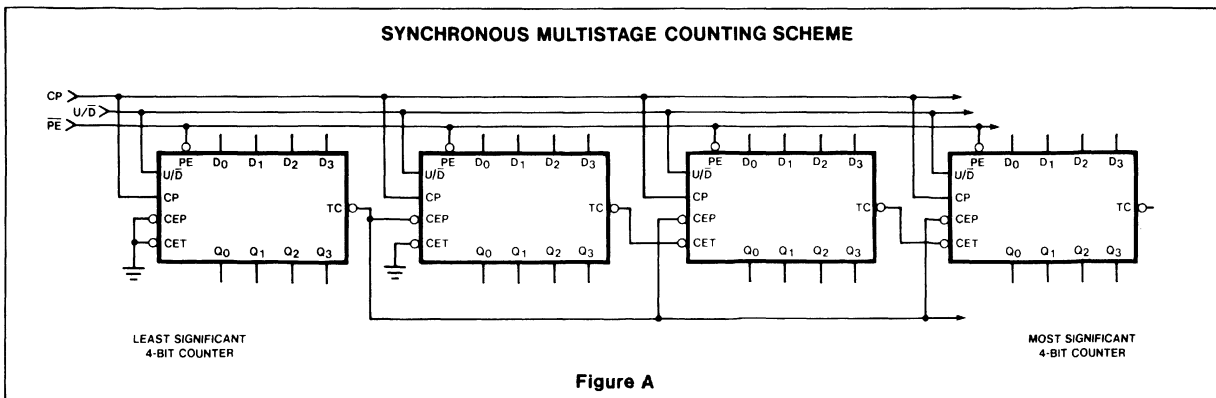
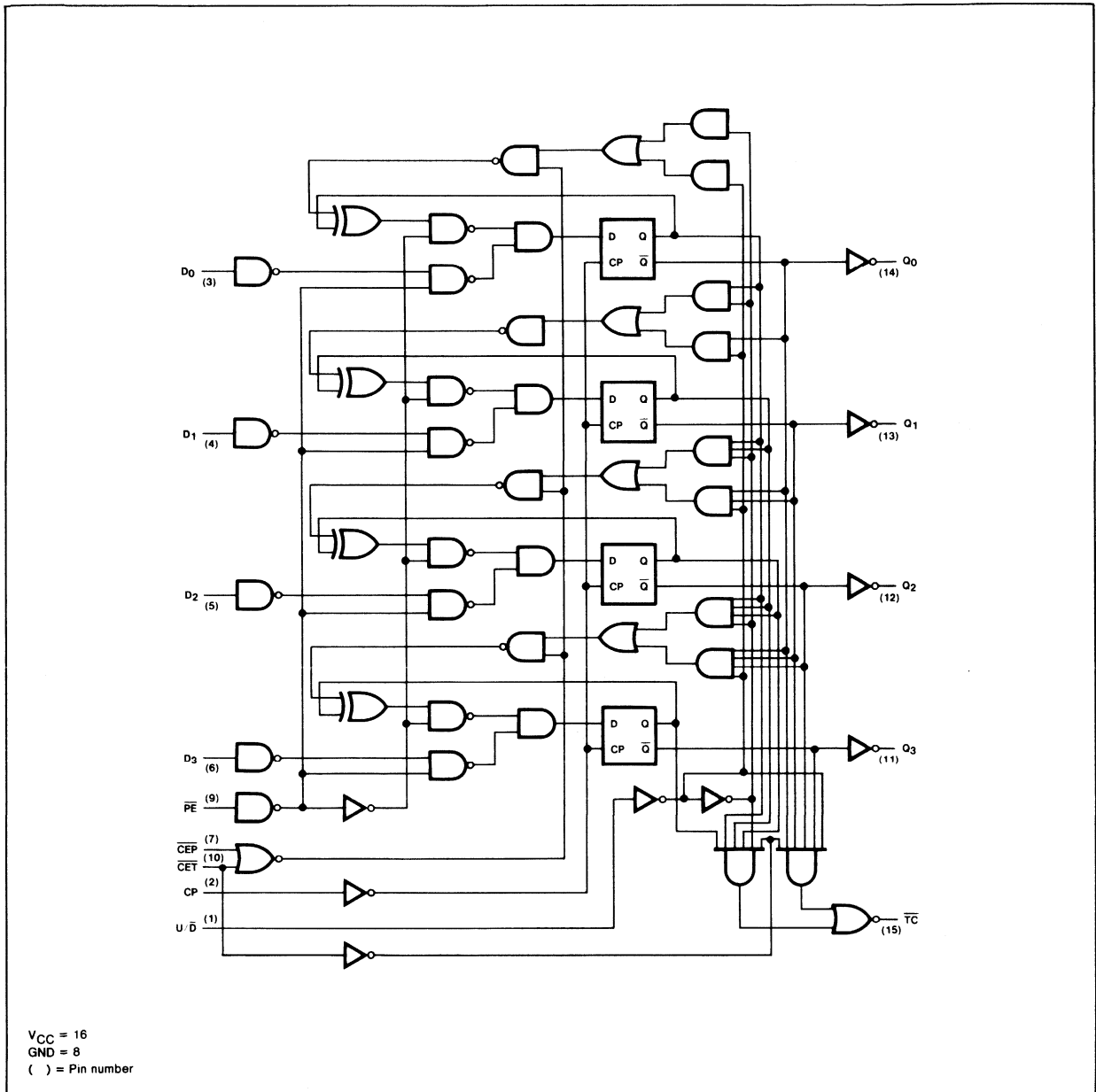


Figure A

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(c)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						34	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

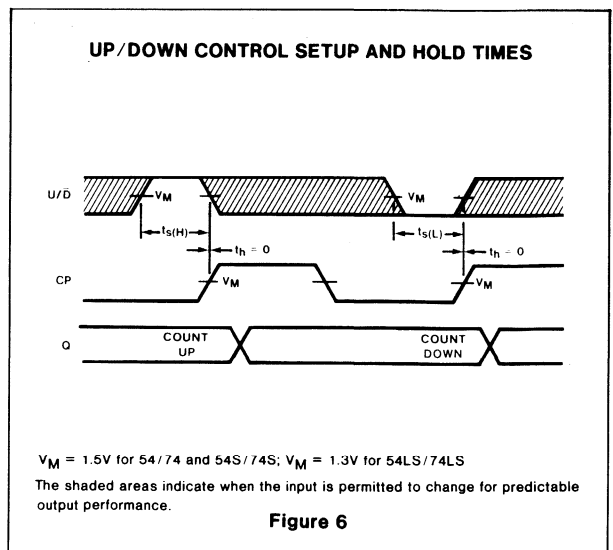
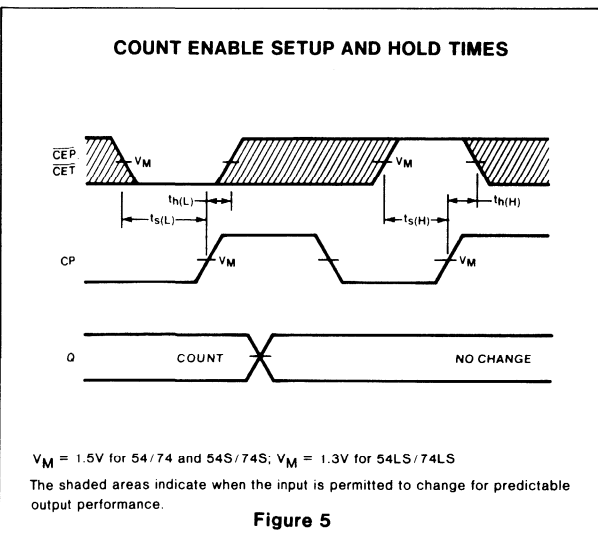
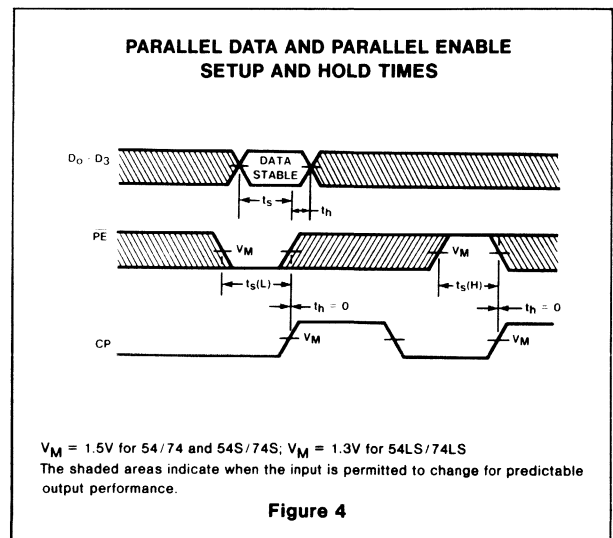
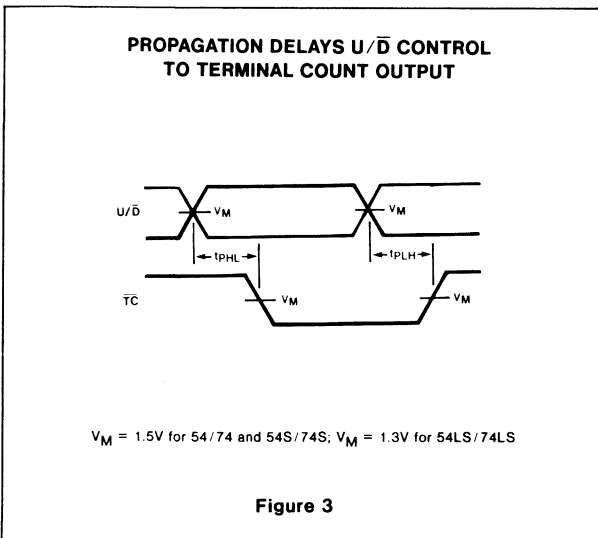
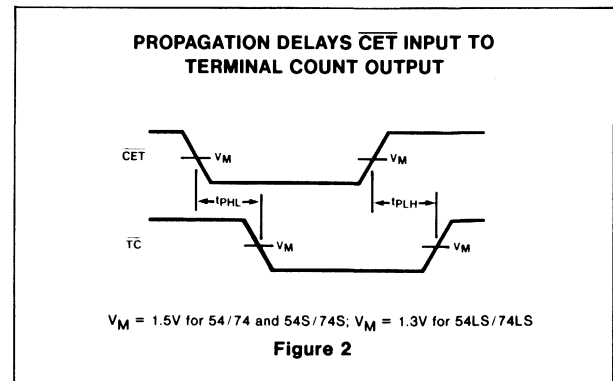
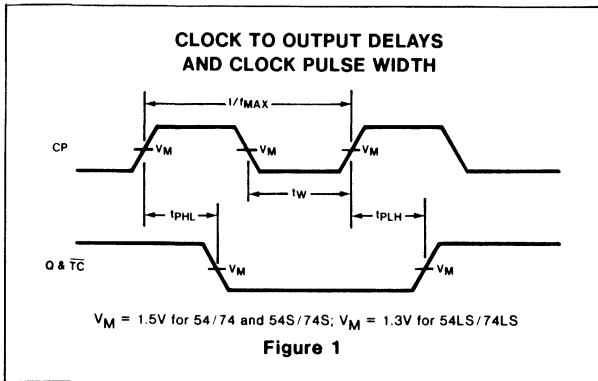
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 2kΩ						
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1					25		MHz
t _{PLH} Propagation delay t _{PHL} Clock to Q output	Figure 1 Figure 1						20 23	ns ns
t _{PLH} Propagation delay t _{PHL} Clock to \overline{TC}	Figure 1						35 35	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CET} to TC	Figure 2						14 14	ns ns
t _{PLH} Propagation delay t _{PHL} U/ \overline{D} control to \overline{TC}	Figure 3						25 29	ns ns

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Clock pulse width	Figure 1					20		ns
t _s Setup time data to clock	Figure 4					20		ns
t _h Hold time data to clock	Figure 4					0		ns
t _s Setup time \overline{PE} to clock	Figure 4					25		ns
t _h Hold time \overline{PE} to clock	Figure 4					0		ns
t _s Setup time \overline{CEP} & \overline{CET} to clock	Figure 5					20		ns
t _h Hold time \overline{CEP} & \overline{CET} to clock	Figure 5					0		ns
t _s Setup time U/ \overline{D} to clock	Figure 6					30		ns
t _h Hold time U/ \overline{D} to clock	Figure 6					0		ns

NOTE

c. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.



54/74170
54LS/74LS170

DESCRIPTION

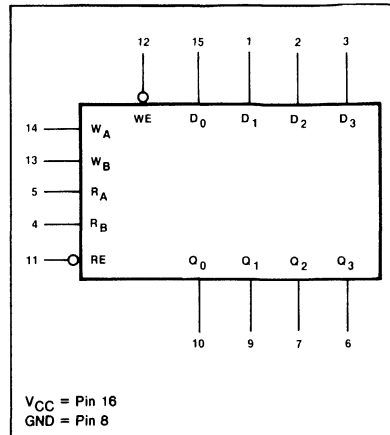
The "170" is a 4-by-4 Register File organized as 4-words of 4-bits. Simultaneous read and write operation is allowed by separate read and write inputs, both address and enable.

Up to 256 outputs in a wired-AND configuration increases the word capacity up to 1024 words with the open collector outputs. Any number of these devices can be operated in parallel to generate an n-bit word.

FEATURES

- Simultaneous and Independent Read and Write operations
- Expandable to 1024 words by n-bits
- Open collector outputs for wired-AND expansion
- See "670" for 3-state output version

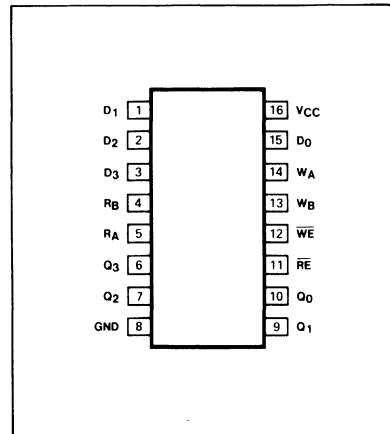
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N74170N	• N74LS170N	
Ceramic DIP	N74170F	• N74LS170F	S54170F	• S54LS170F
Flatpak			S54170W	• S54LS170W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D ₀ -D ₃	Data inputs	I_{IH} (μA)	40		20
		I_{IL} (mA)	-1.6		-0.4
W _A , W _B	Write address inputs	I_{IH} (μA)	40		20
		I_{IL} (mA)	-1.6		-0.4
WE	Write Enable (active LOW) input	I_{IH} (μA)	40		40
		I_{IL} (mA)	-1.6		-0.8
R _A , R _B	Read address inputs	I_{IH} (μA)	40		20
		I_{IL} (mA)	-1.6		-0.4
RE	Read Enable (active LOW) input	I_{IH} (μA)	40		40
		I_{IL} (mA)	-1.6		-0.8
Q ₀ -Q ₃	Outputs	I_{OH} (μA)	+30		+20
		I_{OL} (mA)	16		4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "170" is a 16-bit Register File organized as 4-words of 4-bits each; permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable (WE) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the \overline{WE} is LOW. Data supplied at the inputs will be read out in true (non-inverting) form. Data and Write Address inputs are inhibited when \overline{WE} is HIGH.

Direct acquisition of data stored in any of

the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable (\overline{RE}) is LOW. Data outputs are inhibited and remain HIGH when the Read Enable input is HIGH. This permits simultaneous reading and writing, eliminates recovery times, and is limited in speed only by the read time and the write time.

Up to 256 devices can be stacked to increase the word size to 1024 locations by tying the open collector outputs together. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES(b)
	WE	D_n	
Write Data	L L	L H	L H
Data Latched	H	X	no change

NOTE

b. The Write Address (W_A & W_B) to the "internal latches" must be stable while WE is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	\overline{RE}	INPUTS		OUTPUTS Q_n
		INTERNAL LATCHES(c)		
Read	L	L	L	L
	L	H	H	H
Disabled	H	X	X	H

NOTE

c. The Read Address (R_A & R_B) changes to select the "internal latches" are not constrained by WE or \overline{RE} operation.

H = HIGH voltage level

L = LOW voltage level

X = Don't care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil	140				40	mA
		Com	150				40	mA

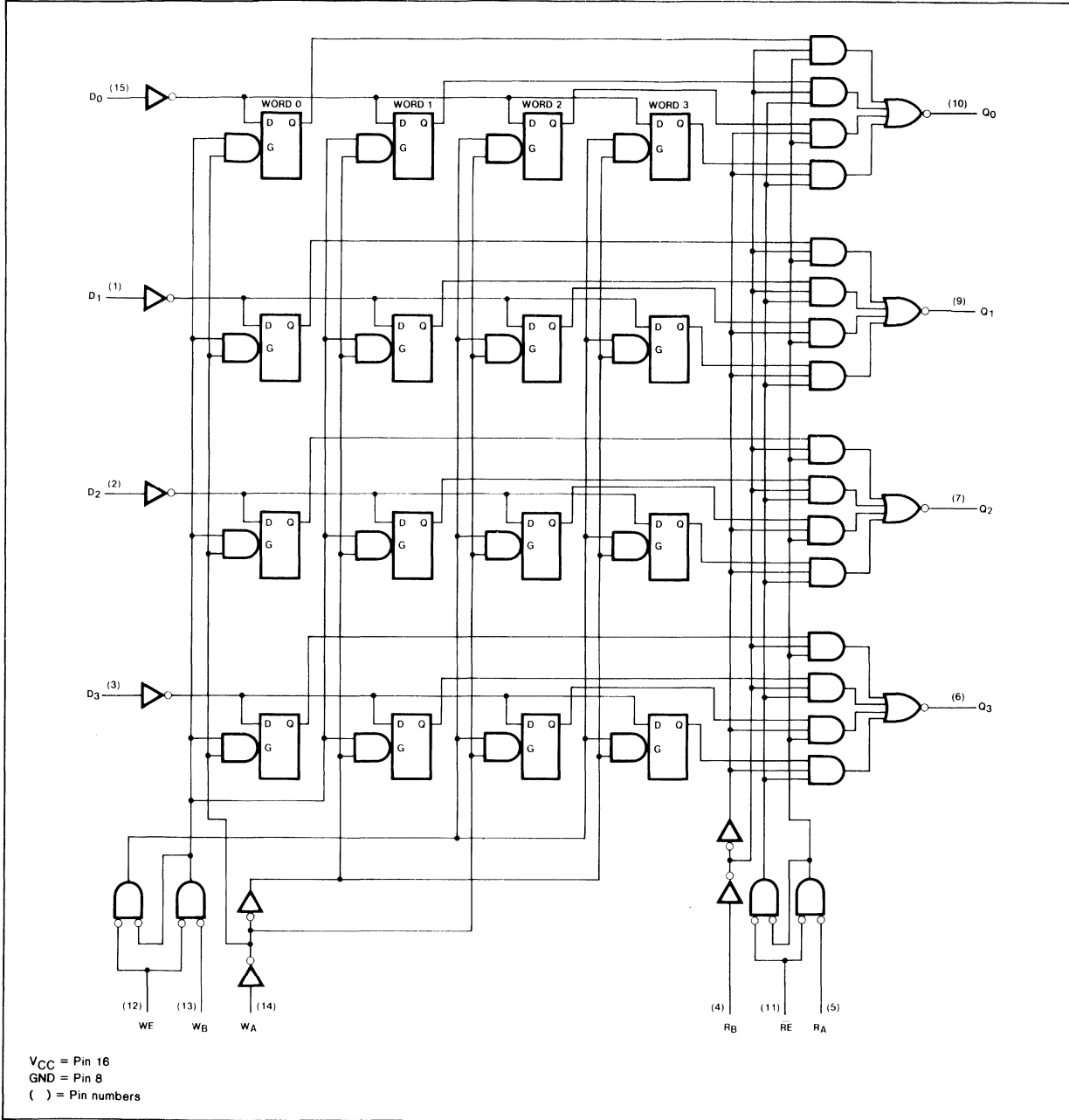
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$				$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Figure 1		15				30	ns
t_{PHL} Read Enable to output			30				30	ns
t_{PLH} Propagation delay	Figure 2		35				40	ns
t_{PHL} Read Address to output			40				40	ns
t_{PLH} Propagation delay	Figure 1		40				45	ns
t_{PHL} Write Enable to output			45				40	ns
t_{PLH} Propagation delay	Figure 1		30				45	ns
t_{PHL} Data to output			45				35	ns

NOTE

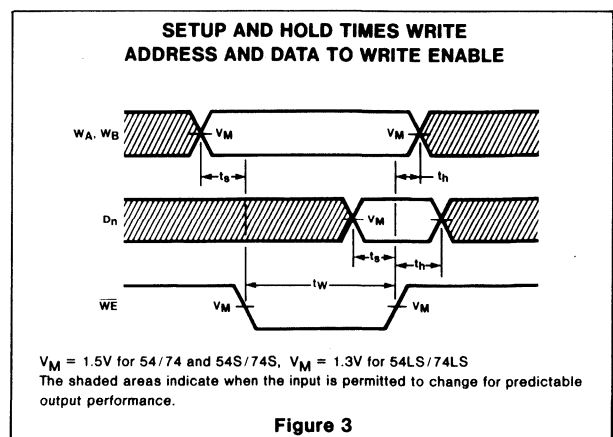
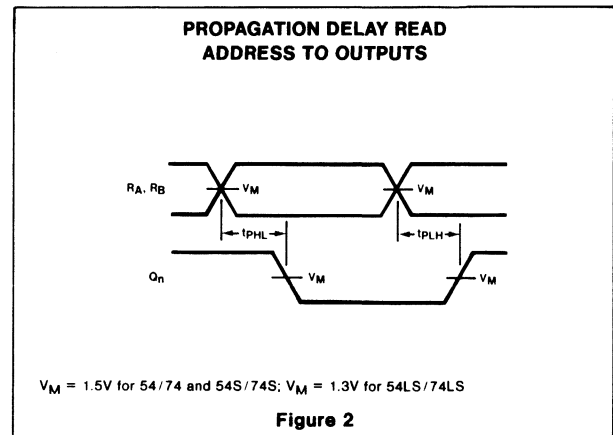
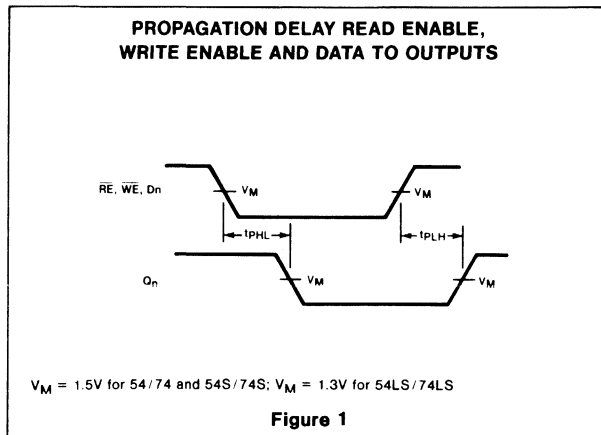
b. For family dc characteristics, see inside front cover for 54/74, and see inside back cover for 54S/74S and 54LS/74LS specifications.

LOGIC DIAGRAM



AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w Write Enable pulse width	Figure 3	25				25		ns
t_s Setup time Data to positive going \overline{WE}	Figure 3	10				10		ns
t_h Hold time Data to positive going \overline{WE}	Figure 3	15				15		ns
t_s Setup time Read Address to negative going \overline{WE}	Figure 3	15				15		ns
t_h Hold time Read Address to positive going \overline{WE}	Figure 3	5.0				5.0		ns



74S172

DESCRIPTION

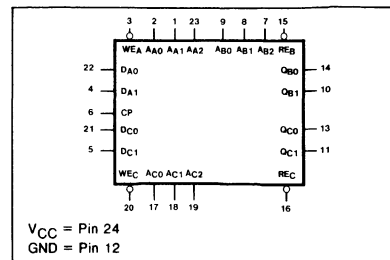
The "172" is a 16-Bit Multiple Port Register File organized as eight words of two bits each. Independent, simultaneous read and write operations are performed using the two 2-bit input ports and two 2-bit output ports. One input and one output port are completely independent, while the other input and output ports share common address inputs.

The 3-state outputs facilitate expansion up to 128 devices for 1024 words. Any number of these devices can be operated in parallel to generate an n-bit word.

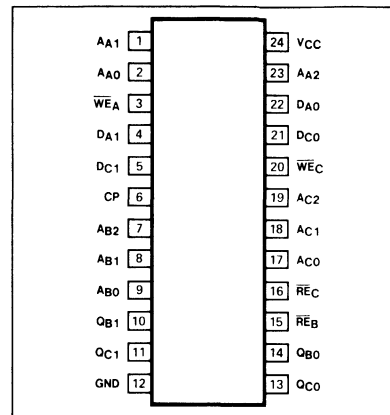
FEATURES

- Simultaneous and independent Read and Write operations
- Expandable to 1024 words on n-bits
- 3-State outputs

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74S172N	
Ceramic DIP	N74S172F	
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)		40 -1.6	
WE _A	Write Enable (active LOW) input for Port "A"	I _{IH} (μA) I _{IL} (mA)		40 -1.6	
AA ₀ , AA ₁ , AA ₂	Address inputs for Port "A"	I _{IH} (μA) I _{IL} (mA)		40 -0.8	
DA ₀ , DA ₁	Data inputs for Port "A"	I _{IH} (μA) I _{IL} (mA)		40 -0.8	
RE _B	Read Enable (active LOW) input for Port "B"	I _{IH} (μA) I _{IL} (mA)		40 -0.8	
AB ₀ , AB ₁ , AB ₂	Address inputs for Port "B"	I _{IH} (μA) I _{IL} (mA)		40 -0.8	
QB ₀ , QB ₁	Data outputs from Port "B"	I _{OH} (mA) I _{OL} (mA)		-5.2 16	
WE _C	Write Enable (active LOW) input for Port "C"	I _{IH} (μA) I _{IL} (mA)		40 -1.6	
AC ₀ , AC ₁ , AC ₂	Address inputs for Port "C"	I _{IH} (μA) I _{IL} (mA)		40 -1.6	
DC ₀ , DC ₁	Data inputs for Port "C"	I _{IH} (μA) I _{IL} (mA)		40 -0.8	
RE _C	Read Enable (active LOW) input for Port "C"	I _{IH} (μA) I _{IL} (mA)		40 -0.8	
QC ₀ , QC ₁	Data outputs from Port "C"	I _{OH} (μA) I _{OL} (mA)		-5.2 16	

NOTE

a. The slashed numbers indicate a different parametric values for Military / Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "172" is a high performance 16-bit multiport register file with 3-state outputs organized as eight words of two bits each. Multiple address decoding circuitry is used so that the read and write operation can be performed independently on up to three word locations. Data can be written into two word locations through input Port "A" or input Port "C" while data is simultaneously read from both output Port "B" and output Port "C".

Port "A" is an input port which can be used to write two bits of data (DA₀, DA₁) into one of eight register locations selected by the address inputs (AA₀, AA₁, AA₂). When the Write Enable (WE_A) input is LOW one setup time prior to the Clock (CP) input, the data is written into the selected location.

Port "B" is an output port which can be used to read two bits of data from one of eight register locations selected by the address inputs (AB₀, AB₁, AB₂). When the Read Enable (RE_B) is LOW, the selected 2-bit word appears on outputs QB₀ and QB₁. When RE_B is HIGH, the QB₀ and QB₁ outputs are in the high impedance "off" state. The read operation is independent of the clock.

Port "C" is a read/write port that has separate data input and data output sections, but common address inputs (AC₀, AC₁, AC₂). Data can be simultaneously written into and read from the same register location. Port "C" can be used to write data into one location while Port "A" is writing into a different location, but data cannot be written reliably into the same location simultaneously.

If both Ports "A" & "C" are enabled for writing into the same location during the same clock cycle, the LOW data will predominate if there is a conflict.

The register operation is essentially a master-slave flip-flop. Each master acts as a transparent D latch when selected by the "A" or "C" address and the clock and applicable write enable are LOW. The data in the master is transferred to the slave (or output section) following the LOW-to-HIGH transition of the Clock (CP). The address inputs must be stable while the clock and write enable inputs are LOW to ensure retention of data previously written into the other locations. Any number of masters can be altered while the clock and write enable are LOW, but the new data will not be loaded into the slaves, or be available at the outputs, until the clock goes HIGH.

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS			ADDRESSED REGISTER
	CP	WE	D _n	
Write Data ^(b)	↑ ↑	l l	l h	L H
Hold ^(c)	↓	h	X	no change

READ MODE SELECT TABLE

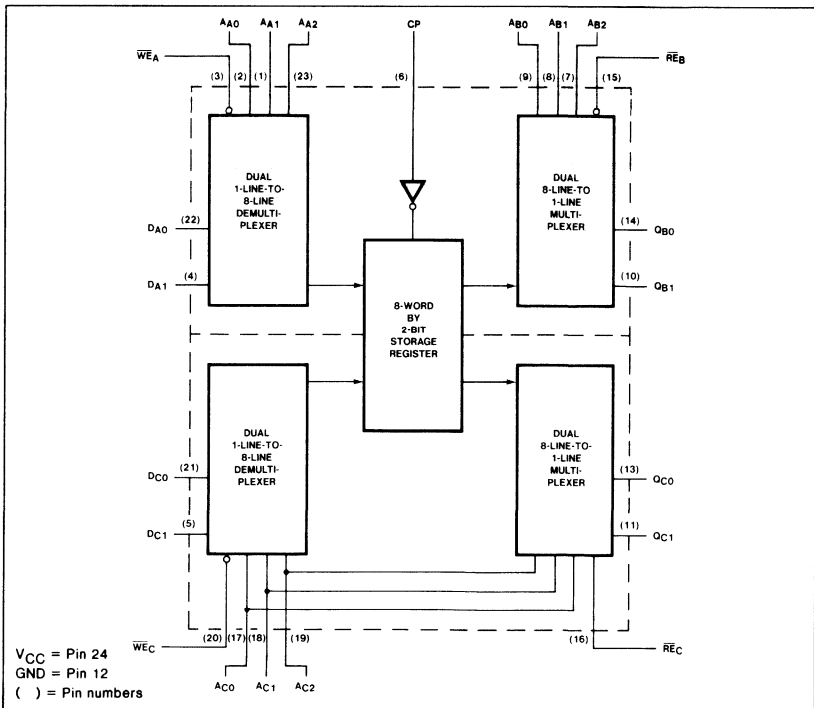
OPERATING MODE	INPUTS		OUTPUTS
	RE	ADDRESSED REGISTER	
Read	L L	L H	L H
Disabled	H	X	(Z)

H = HIGH voltage level steady state
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH or HIGH-to-LOW clock transition.
 L = LOW voltage level steady state
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 (Z) = High impedance "off" state
 ↑ = LOW-to-HIGH clock transition
 ↓ = HIGH-to-LOW clock transition

NOTE

- b. The Write Address (A_A & A_C) to the "internal register" must be stable while WE and CP are LOW for conventional operation.
- c. The Write Enable must be HIGH before the HIGH-to-LOW Clock transition to ensure that the data in the register is not changed.

BLOCK DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER		TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = Min I _{OH} = -5.2mA			2.4				V
V _{OL}	Output LOW voltage	V _{CC} = Min I _{OL} = 16mA				0.4			V
I _{OS}	Output short circuit current	V _{CC} = Max V _{OUT} = OV			-18	-55			mA
I _{CC}	Supply current	V _{CC} = Max				170			mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Figure 1			20				MHz
t _{PLH} t _{PHL}	Propagation delay Address (B or C) to output	Figure 2				30 30			ns ns
t _{PLH} t _{PHL}	Propagation delay Clock to output	Figure 1				38 38			ns ns
t _{PZH}	Read enable time to HIGH	Figure 3				30			ns
t _{PZL}	Read enable time to LOW	Figure 4				30			ns
t _{PHZ}	Disable time from HIGH	Figure 3, C _L = 5pF				20			ns
t _{PLZ}	Disable time from LOW	Figure 4, C _L = 5pF				20			ns

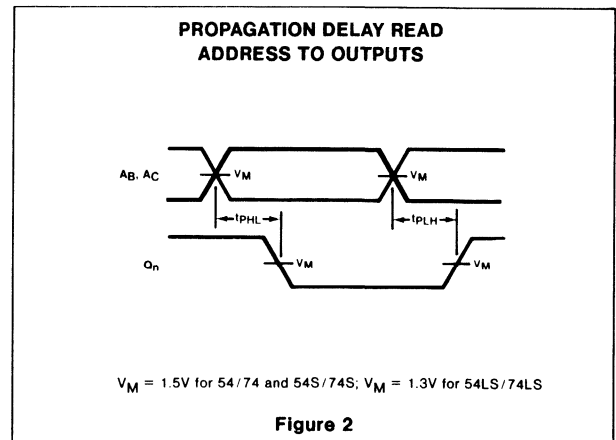
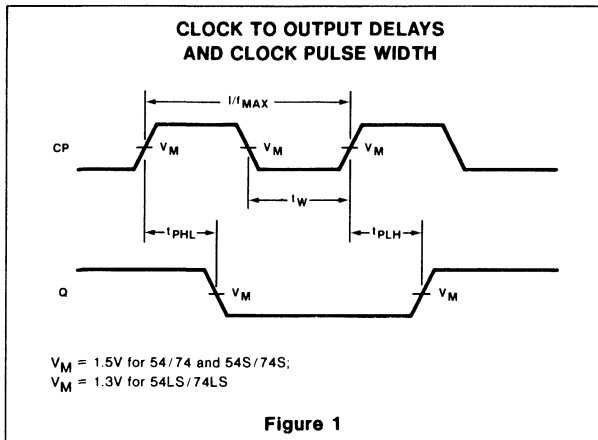
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

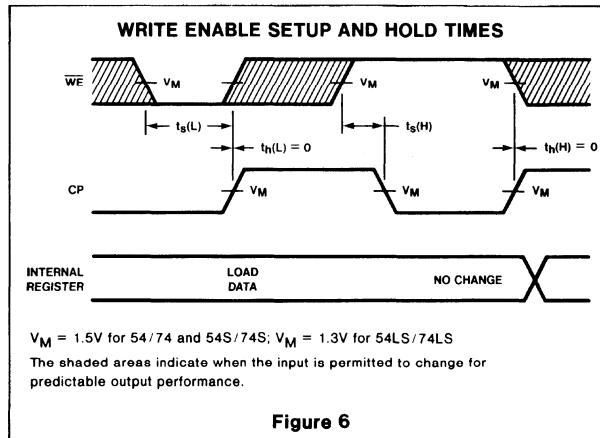
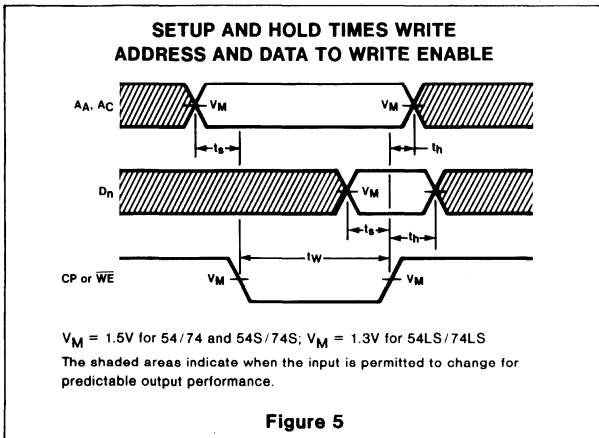
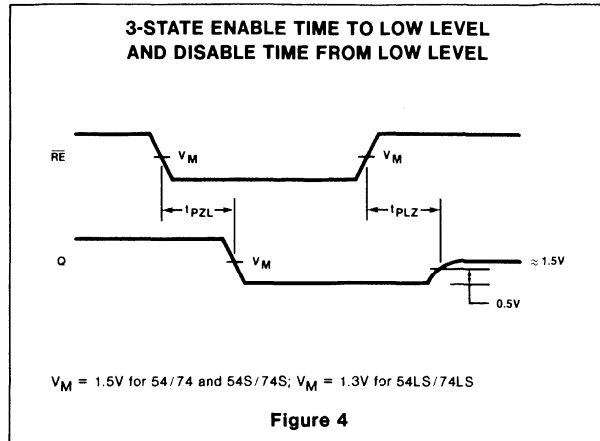
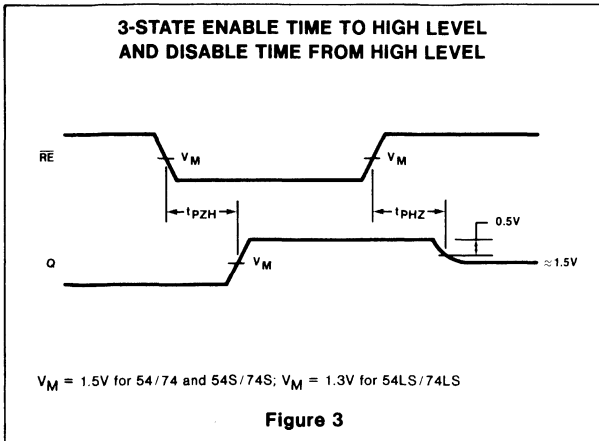
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W Clock pulse width	Figure 1			25				ns
t_s Setup time Write address (A or C) to negative going Clock and \overline{WE} .	Figure 5			15				ns
t_h Hold time Write address (A or C) to positive going Clock and \overline{WE}	Figure 5			0				ns
$t_{S(H)}$ Setup time HIGH Data to Clock	Figure 5			30				ns
$t_{H(H)}$ Hold time HIGH Data to Clock	Figure 5			0				ns
$t_{S(L)}$ Setup time LOW Data to Clock	Figure 5			20				ns
$t_{H(L)}$ Hold time LOW Data to Clock	Figure 5			0				ns
t_s Setup time LOW \overline{WE} to positive going Clock	Figure 6			35				ns
t_h Hold time LOW \overline{WE} to positive going Clock	Figure 6			0				ns
t_s Setup time HIGH \overline{WE} to negative going Clock	Figure 6			10				ns
t_h Hold time HIGH \overline{WE} to positive going Clock	Figure 6			0				ns

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



54/74173
54LS/74LS173

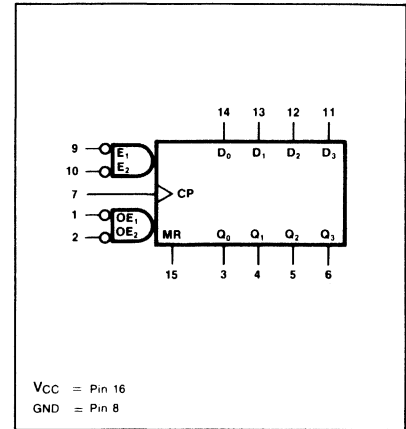
DESCRIPTION

The "173" is a Quad D-Type Flip-Flop with 3-State buffered outputs, a gated input enable and a gated output enable. The device is used as a 4-Bit Register capable of driving a 3-State bus directly. Data is loaded into the register during the LOW-to-HIGH clock transition. The Master Reset asynchronously clears all flip-flops.

FEATURES

- Edge triggered D-Type register
- Gated input enable for "hold" do nothing mode
- 3-State output buffers
- Gated output enable control
- Pin compatible with the 8T10 and DM8551

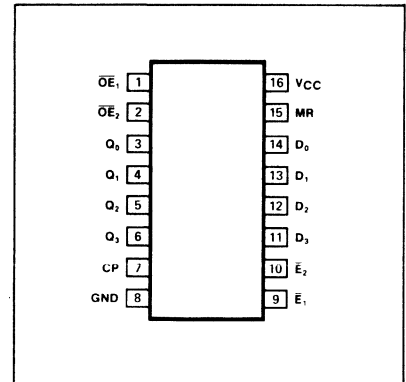
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to +70°C	MILITARY RANGES V _{CC} = 5V ± 10%; T _A = -55°C to +125°C
Plastic DIP	N74173N • N74LS173N	
Ceramic DIP	N74173F • N74LS173F	S54LS173F
Flatpak		S54LS173W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D ₀ -D ₃	Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
\bar{E}_1, \bar{E}_2	Clock Enable inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
CP	Clock (Active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
\bar{OE}_1, \bar{OE}_2	3-State Output Enable inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
MR	Asynchronous Master Reset	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
Q ₀ -Q ₃	3-State outputs	I _{OH} (μA) I _{OL} (mA)	5.2 16		-1/-2.6 (a) 12/24 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "173" is a 4-Bit Parallel Load Register with clock enable control, 3-State buffered outputs and master reset. When the two Clock Enable (\bar{E}_1 and \bar{E}_2) inputs are LOW, the data on the D inputs is loaded into the register synchronously with the LOW-to-HIGH Clock (CP) transition. When one or both \bar{E} inputs are HIGH one setup time before the LOW-to-HIGH clock transition, the register will retain the previous data. The Data inputs and Clock Enable inputs are fully edge-triggered and must be stable only one setup time before the LOW-to-HIGH clock transition.

The Master Reset (MR) is an active HIGH asynchronous input. When the Mr is HIGH all four flip-flops are reset (cleared) independently of any other input condition.

The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable (\bar{OE}_1 and \bar{OE}_2) inputs are LOW, the data in the register is presented at the Q outputs. When one or both \bar{OE} inputs is HIGH the outputs are forced to a high impedance "off" state. The 3-State output buffers are completely independent of the register operation; the \bar{OE} transition do not affect the clock and reset operations.

MODE SELECT—FUNCTION TABLE

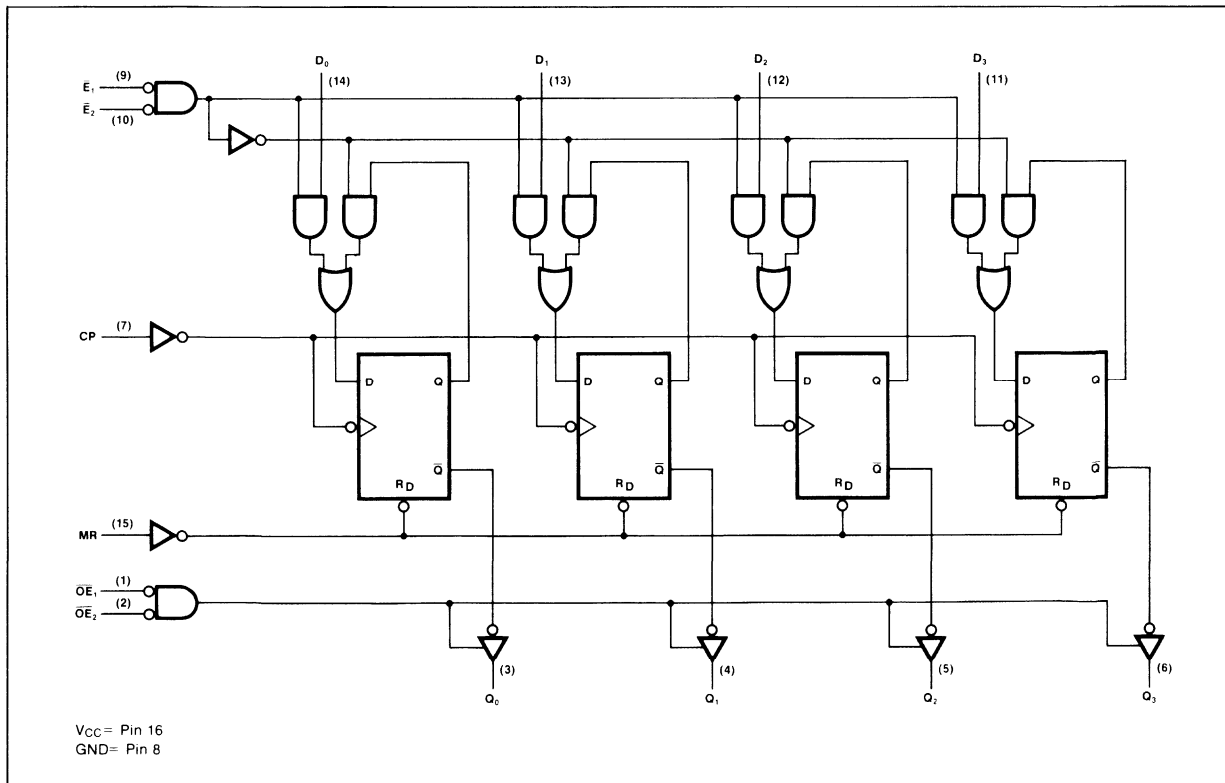
REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	\bar{E}_1	\bar{E}_2	D_n	Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel Load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (No change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS
	Q_n (Register)	\bar{OE}_1	\bar{OE}_2	Q_0, Q_1, Q_2, Q_3
Read	L	L	L	L
	H	L	L	H
Disabled	X	H	X	(Z)
	X	X	H	(Z)

NOTES

- H = HIGH voltage level
- h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
- L = LOW voltage level
- l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
- q_n = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition
- X = Don't care
- (Z) = High impedance "off" state
- ↑ = LOW-to-HIGH transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE ^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min I _{OL} = 16mA		0.4					V
						0.4		V
						0.5 ^(c)		V
V _{OH} Output HIGH voltage	V _{CC} = Min I _{OH} = See Fan Out Table	2.4				2.4		V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-30	-70			-30	-100	mA
I _{CC} Supply current	V _{CC} = Max		72				30	mA

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 50pF R _L = 400Ω				C _L = 45pF R _L = 667Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1	25				30		MHz
t _{PLH} Propagation delay clock to output	Figure 1		43				18	ns
			31				26	ns
t _{PHL} Propagation delay MR to output	Figure 4		27				36	ns
t _{PZH} Output enable to HIGH level	Figure 2		30				15	ns
t _{PZL} Output enable to LOW level	Figure 3		30				18	ns
t _{PHZ} Output disable from HIGH level	Figure 2		14				13	ns
t _{PLZ} Output disable from LOW level	Figure 3		20				20	ns

AC SETUP REQUIREMENTS T_A = 25°C (See Section 4 for test Circuits and Conditions)

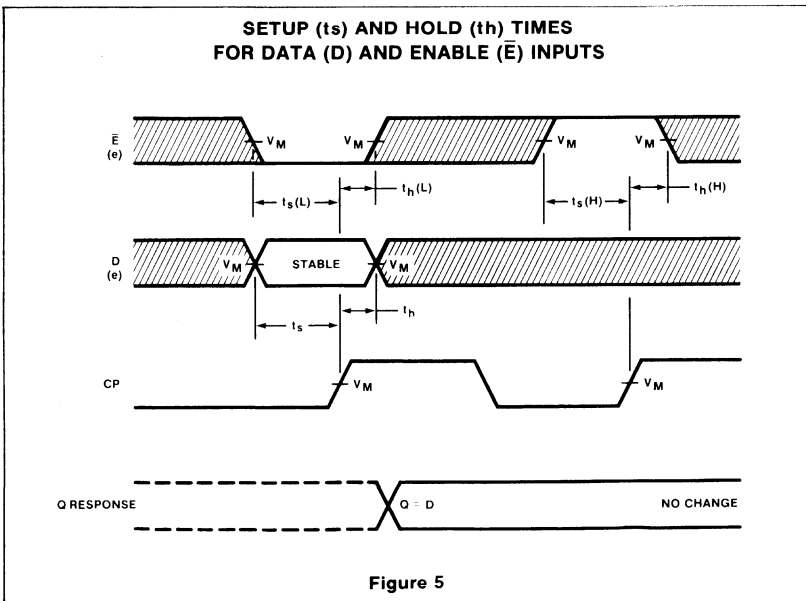
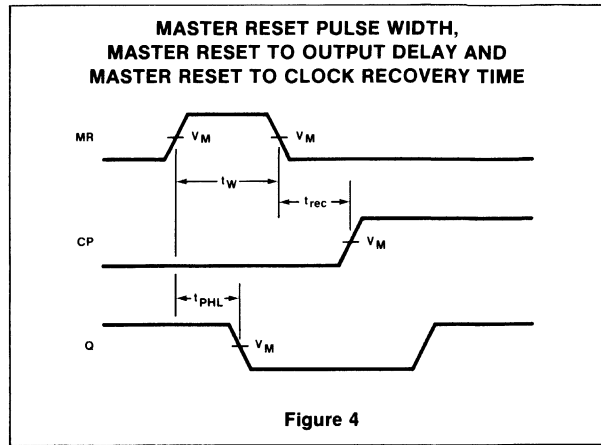
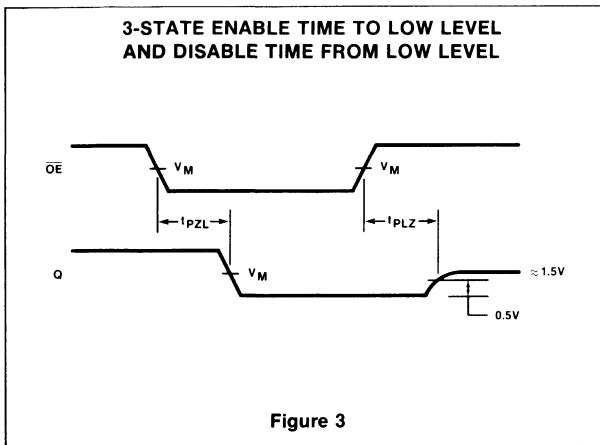
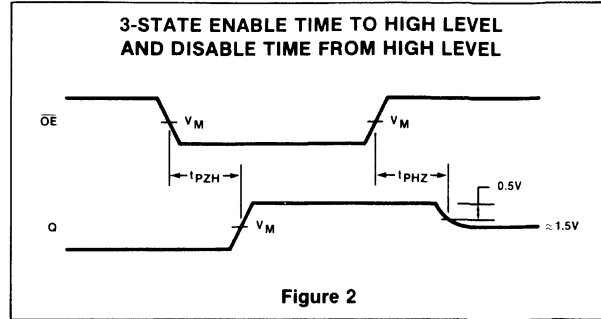
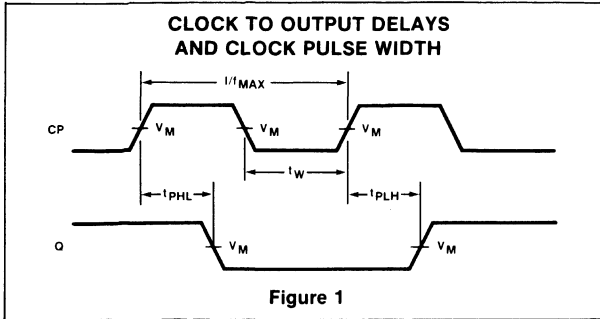
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w (CP) Clock pulse width	Figure 1	20				18		ns
t _w (MR) MR pulse width	Figure 4	20				20		ns
t _s (D) Set up time Data to Clock	Figure 5	10				13		ns
t _h (D) Hold time Data to Clock	Figure 5	10				0		ns
t _s (\bar{E}) Set up time Data to Clock	Figure 5	17				17		ns
t _h (\bar{E}) Hold time Enable to Clock	Figure 5	2				0		ns
t _{rec} (MR) Recovery time Master Reset to Clock	Figure 4	10				17		ns

NOTES

^b: For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications

^c: This parameter for Commercial Range only

AC WAVEFORMS (d)



NOTES

- d. $V_L = 1.5V$ for 54/74 & 54S/74S. $V_M = 1.3V$ for 54LS/74LS.
- e. The shaded areas indicate when the input is permitted to change for predictable

54/74174
54S/74S174
54LS/74LS174

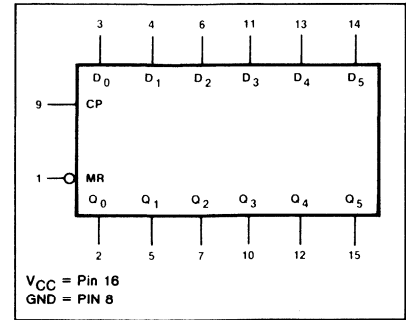
DESCRIPTION

The "174" is a Hex D Flip-Flop used primarily as a 6-bit edge-triggered storage register. Data on the D inputs is loaded into the register during the LOW-to-HIGH transition of the clock pulse. The Master Reset (\overline{MR}) input asynchronously clears all flip-flops.

FEATURES

- Six edge-triggered D flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

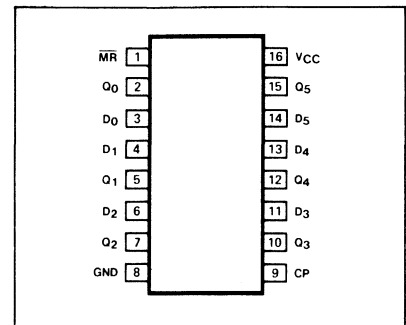
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74174N	
	N74S174N • N74LS174N	
Ceramic DIP	N74174F	S54174F
	N74S174F • N74LS174F	S54LS174F
Flatpak		S54174W
		S54LS174W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
D ₀ - D ₅	Parallel Data inputs	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
\overline{MR}	Master Reset (active LOW) input	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
Q ₀ - Q ₅	Outputs	I_{OH} (μA)	-800	-1000	-400
		I_{OL} (mA)	16	20	4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "174" has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

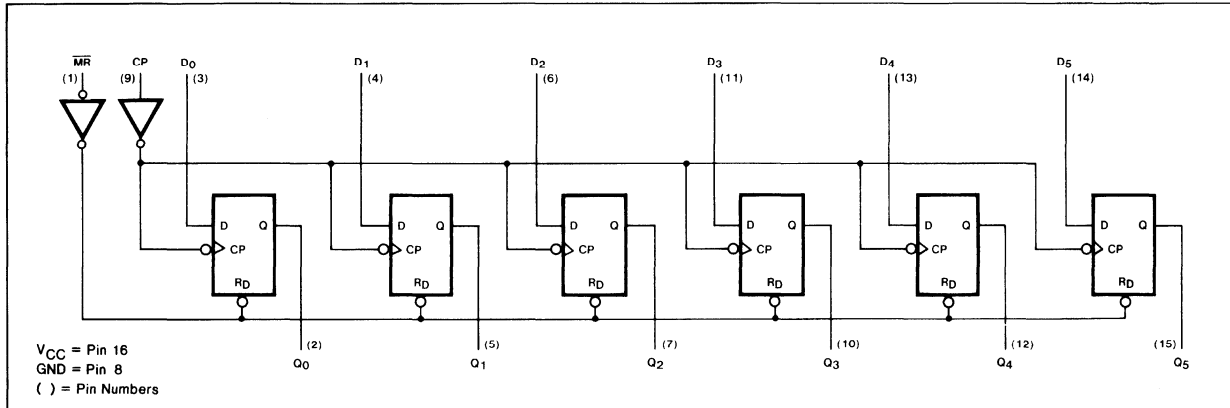
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	\overline{MR}	CP	D _n	Q _n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		65		144		26	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

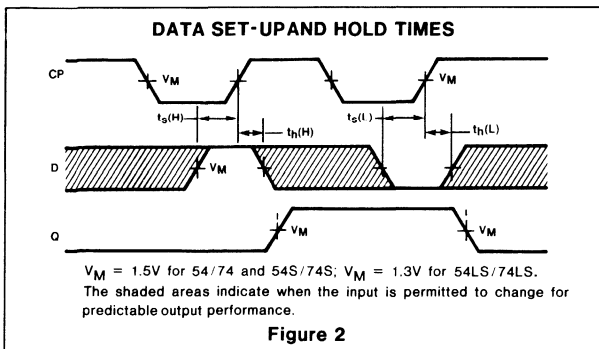
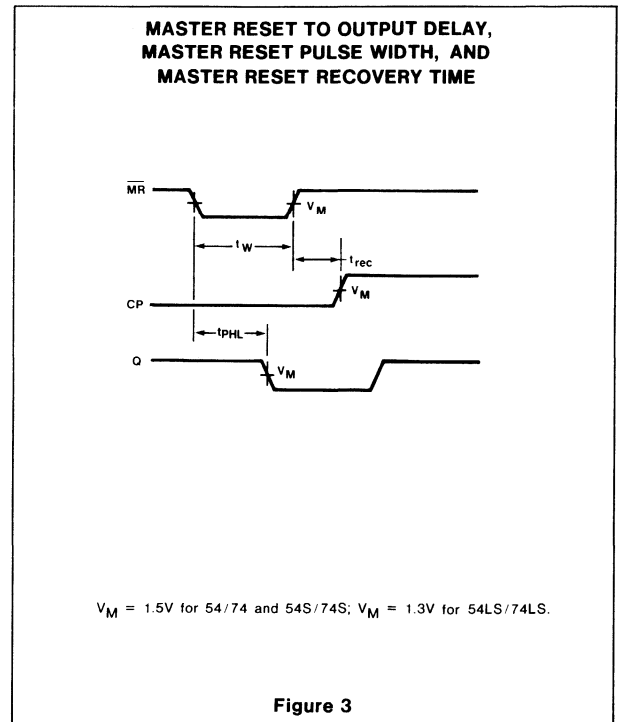
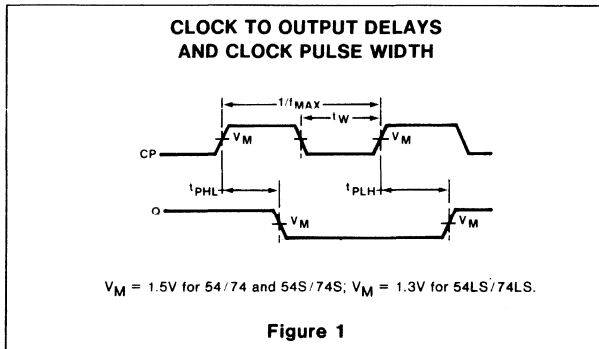
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2KΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1	25		75		30		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Figure 1		30 30		13 15		24 30	ns ns
t _{PHL} Propagation delay \overline{MR} to output	Figure 2		35		15		35	ns

NOTE
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Figure 1	20		7.0		16		ns
t_W Master Reset pulse width	Figure 2	20		10		15		ns
$t_S(H)$ Setup time HIGH data to CP	Figure 3	20		5.0		12		ns
$t_H(H)$ Hold time HIGH data to CP	Figure 3	0		3.0		0		ns
$t_S(L)$ Setup time LOW data to CP	Figure 3	20		5.0		8.0		ns
$t_H(L)$ Hold time LOW data to CP	Figure 3	0		3.0		0		ns
t_{rec} Recovery time \overline{MR} to CP	Figure 2	25		5.0		15		ns

AC WAVEFORMS



**54/74175
54S/74S175
54LS/74LS175**

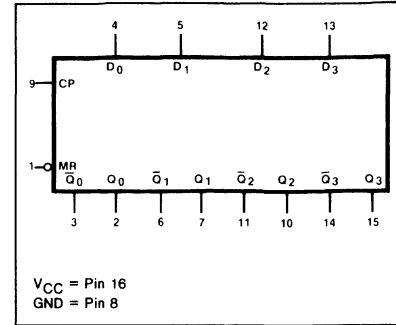
DESCRIPTION

The "175" is a Quad edge-triggered D Flip-Flop useful for general flip-flop requirements where clock and reset inputs are common. Data on the D inputs is loaded into the register during the LOW-to-HIGH transition of the clock pulse. Each flip-flop is provided with both true and complemented outputs. The Master Reset input, when LOW, asynchronously clears all flip-flops.

FEATURES

- Four edge-triggered D flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

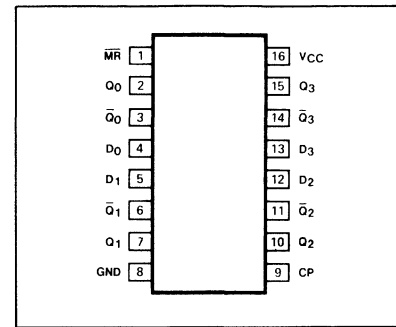
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74175N	
	N74S175N • N74LS175N	
Ceramic DIP	N74175F	S54175F
	N74S175F • N74LS175F	S54LS175F
Flatpak		S54175W
		S54LS175W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
D ₀ -D ₃	Parallel Data inputs	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
\overline{MR}	Master Reset (active LOW) input	I_{IH} (μA)	40	50	20
		I_{IL} (mA)	-1.6	-2.0	-0.4
Q ₀ -Q ₃	True outputs	I_{OH} (μA)	-800	-1000	-400
		I_{OL} (mA)	16	20	4/8 ^(a)
$\overline{Q_0}$ - $\overline{Q_3}$	Complement outputs	I_{OH} (μA)	-800	-1000	-400
		I_{OL} (mA)	16	20	4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "175" is a quad edge-triggered D-type flip-flop with individual D inputs and both Q and \bar{Q} outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

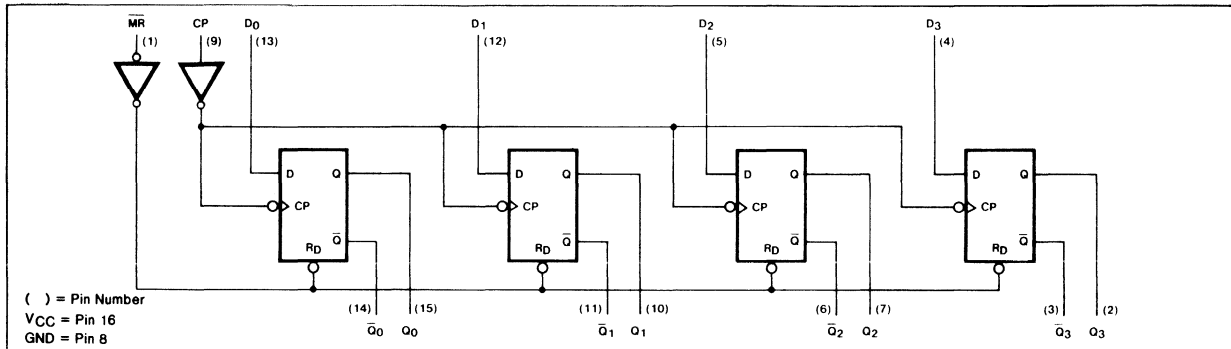
All Q outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	\overline{MR}	CP	D _n	Q _n	\bar{Q}_n
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		45		96		18	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1	25		50		35		MHz
t _{PLH} Propagation delay	Figure 1		30		12		22	ns
t _{PHL} Clock to outputs			35		17		26	ns
t _{PLH} Propagation delay	Figure 3		25		15		24	ns
t _{PHL} \overline{MR} to outputs			35		22		28	ns

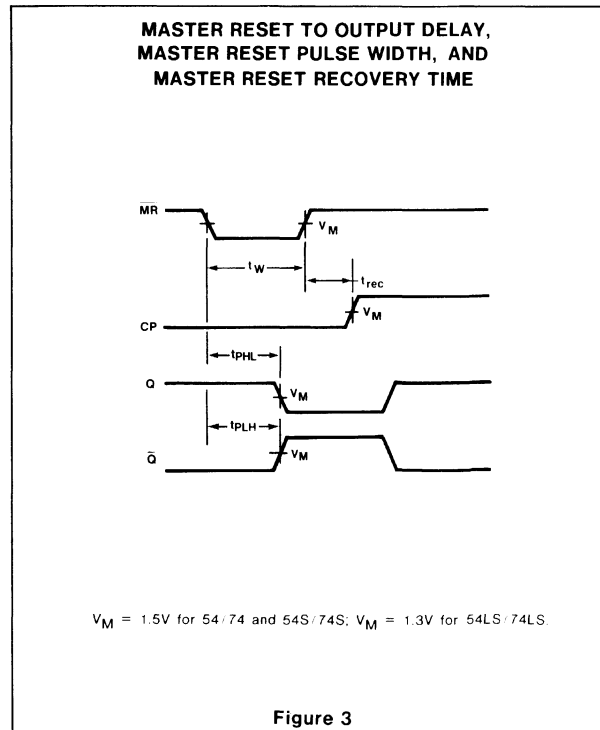
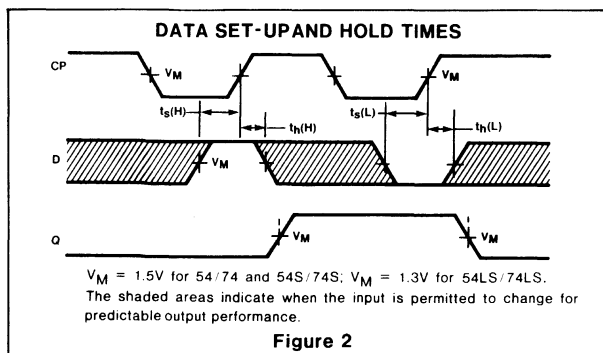
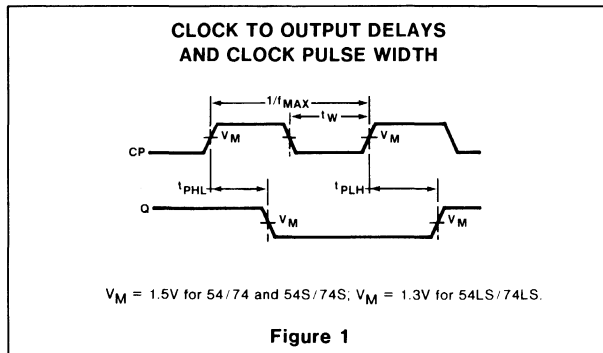
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Figure 1	20		12		16		ns
t_W Master Reset pulse width	Figure 3	20		12		15		ns
$t_{S(H)}$ Setup time HIGH data to CP	Figure 2	20		8.0		12		ns
$t_{h(H)}$ Hold time HIGH data to CP	Figure 2	0		2.0		5.0		ns
$t_{S(L)}$ Setup time LOW data to CP	Figure 2	12		8.0		6.0		ns
$t_{h(L)}$ Hold time LOW data to CP	Figure 2	0		2.0		0		ns
t_{rec} Recovery time \overline{MR} to CP	Figure 3	25		15		20		ns

AC WAVEFORMS



54/74180

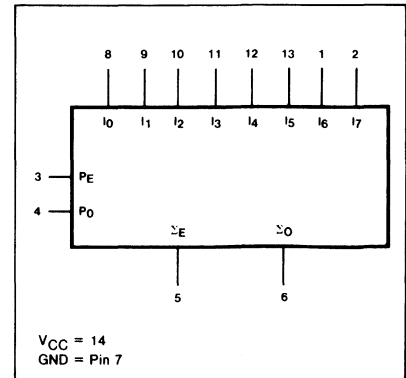
DESCRIPTION

The "180" is a 9-Bit Parity Generator/Checker which features Odd and Even parity outputs. It is used for detecting errors in high speed data transfers. The two enable inputs allow the device to be used to generate or check either odd or even parity. Expansion is easily accomplished by cascading any numbers of 8-bit stages.

FEATURES

- Word-length easily expanded by cascading
- Generate even or odd parity
- Checks for parity errors
- See "280" for faster parity checker

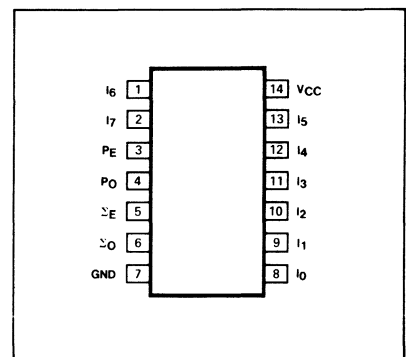
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N74180N	
Ceramic DIP	N74180F	S54180F
Flatpak		S54180W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
I ₀ -I ₇	Data inputs	I _{IH} (μ A) I _{IL} (mA)	40 -1.6		
P _E	Even Parity enable input	I _{IH} (μ A) I _{IL} (mA)	80 -3.2		
P _O	Odd Parity enable input	I _{IH} (μ A) I _{IL} (mA)	80 -3.2		
Σ _E	Even parity output	I _{OH} (μ A) I _{OL} (mA)	-800 16		
Σ _O	Odd parity output	I _{OH} (μ A) I _{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "180" is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even and Odd parity enable inputs and parity outputs are available for generating or checking parity on 8-bits.

True active HIGH or true active LOW parity can be generated at both the Even and Odd outputs. True active HIGH parity is established with Even Parity enable input (P_E) set HIGH and the Odd Parity enable input (P_O) set LOW. True active LOW parity is established when P_E is LOW and P_O is HIGH. When both enable inputs are at the same logic level, both outputs will be forced to the opposite logic level.

Parity checking of a 9-bit word (8-bit plus parity) is possible by using the two enable inputs plus an inverter as the ninth data input. To check for true active HIGH parity, the ninth data input is tied to the P_O input and an inverter is connected between the P_O and P_E inputs. To check for true active LOW parity, the ninth data input is tied to the P_E input and an inverter is connected between the P_E and P_O inputs.

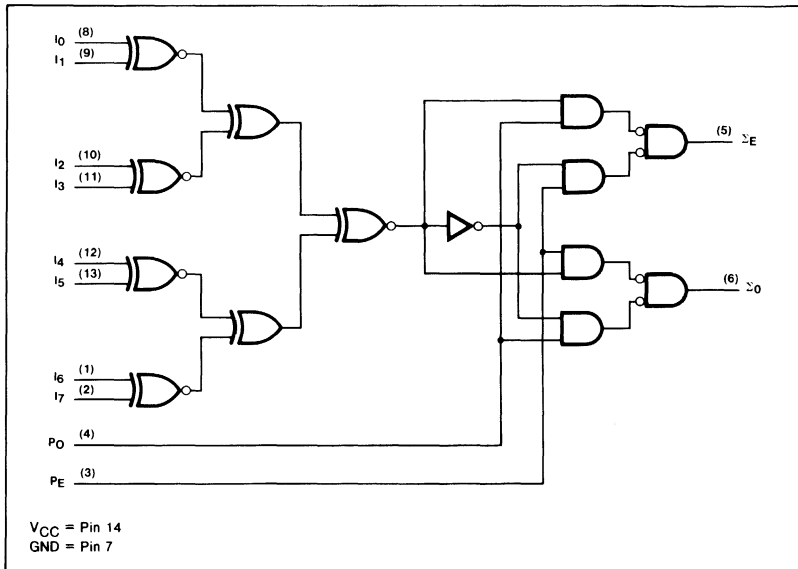
Expansion to larger word sizes is accomplished by serially cascading the "180" in 8-bit increments. The Even and Odd parity outputs of the first stage are connected to the corresponding P_E and P_O inputs respectively of the succeeding stage.

TRUTH TABLE

INPUTS			OUTPUTS	
Number of HIGH Data Inputs (I_0-I_7)	P_E	P_O	ΣE	ΣO
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$	Mil	49					mA
		Com	56					mA

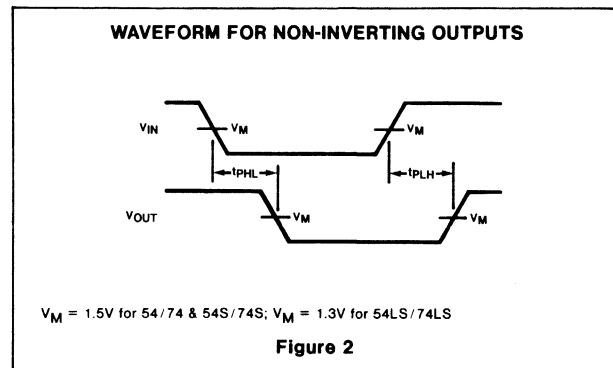
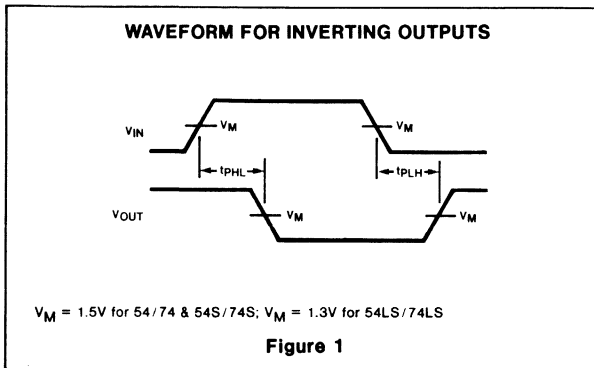
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Even output		60 68					ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Odd output		48 38					ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Even output		48 38					ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Odd output		60 68					ns ns
t_{PLH} t_{PHL}	Propagation delay P_E or P_O to output		20 10					ns ns

AC WAVEFORMS



54/74181
54S/74S181
54LS/74LS181

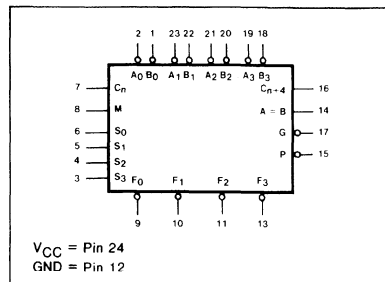
DESCRIPTION

The "181" is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. The "181" can be expanded in 4-bit increments to operate on any word length with a minimum loss in performance.

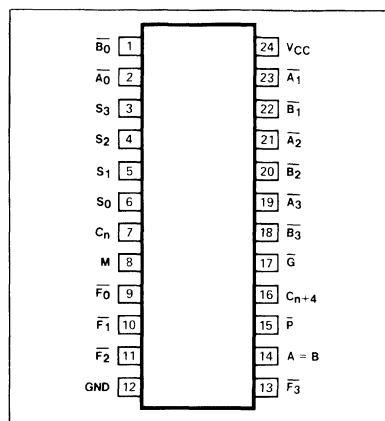
FEATURES

- Provides 16 arithmetic operations **ADD, SUBTRACT, COMPARE, DOUBLE plus twelve other arithmetic operations**
- Provides all 16 logic operations of two variables **EXCLUSIVE-OR, COMPARE, AND, NAND, NOR, OR, plus ten other logic operations**
- Full lookahead carry for high speed arithmetic operation on long words

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74181N N74S181N • N74LS181N	
Ceramic DIP	N74181F N74S181F • N74LS181F	S54181F S54S181F • S54LS181F
Flatpak		S54LS181W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
$\bar{A}_0-\bar{A}_3$	Operand A (active LOW) inputs	I _{IH} (μA) I _{IL} (mA)	120 -4.8	150 -6.0	60 -1.2
$\bar{B}_0-\bar{B}_3$	Operand B (active LOW) inputs	I _{IH} (μA) I _{IL} (mA)	120 -4.8	150 -6.0	60 -1.2
S ₀ -S ₃	Function Select inputs	I _{IH} (μA) I _{IL} (mA)	160 -6.4	200 -8.0	80 -1.6
M	Mode control input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
C _n	Carry input	I _{IH} (μA) I _{IL} (mA)	200 -8.0	250 -10	100 -2.0
$\bar{F}_0-\bar{F}_3$	Function (active LOW) outputs	I _{OH} (μA) I _{OL} (mA)	-800 16	-1000 20	-400 4/8 (a)
A = B	Comparator output (open collector)	I _{OH} (μA) I _{OL} (mA)	+250 16	+250 20	+100 4/8 (a)
\bar{G}	Carry Generate (active LOW) output	I _{OH} (μA) I _{OL} (mA)	-800 16	-1000 20	-400 16
\bar{P}	Carry Propagate (active LOW) output	I _{OH} (μA) I _{OL} (mA)	-800 16	-1000 20	-400 8.0
C _n + 4	Ripple Carry output	I _{OH} (μA) I _{OL} (mA)	-800 16	-1000 20	-400 4/8 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "181" is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \dots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals \bar{P} (Carry Propagate) and \bar{G} (Carry Generate). \bar{P} and \bar{G} are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the device is used in conjunction with the "182" carry lookahead circuit. One carry lookahead package is required for each group of four "181" devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A=B output from the device goes HIGH when all four \bar{F} outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A=B output is open collector and can be wired-AND with other A=B outputs to give a comparison for more than four bits. The A=B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

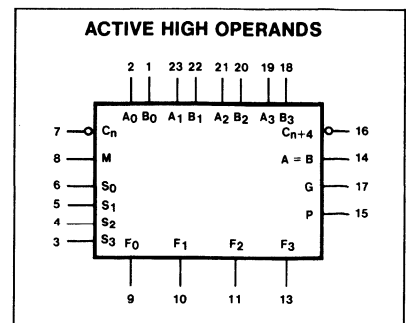
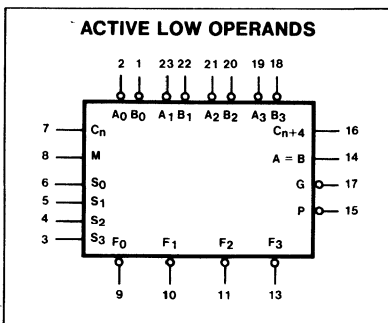
MODE SELECT—FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) ($C_n = H$)
L	L	L	L	\bar{A}	A
L	L	L	H	$\bar{A} + \bar{B}$	A + B
L	L	H	L	$\bar{A}B$	A + \bar{B}
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\bar{A}\bar{B}$	A plus $\bar{A}\bar{B}$
L	H	L	H	\bar{B}	(A + B) plus $\bar{A}\bar{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$\bar{A}\bar{B}$	AB minus 1
H	L	L	L	$\bar{A} + B$	A plus AB
H	L	L	H	$\bar{A} \oplus \bar{B}$	A plus B
H	L	H	L	B	(A + \bar{B}) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	$A + \bar{B}$	(A + B) plus A
H	H	H	L	A + B	(A + \bar{B}) plus A
H	H	H	H	A	A minus 1

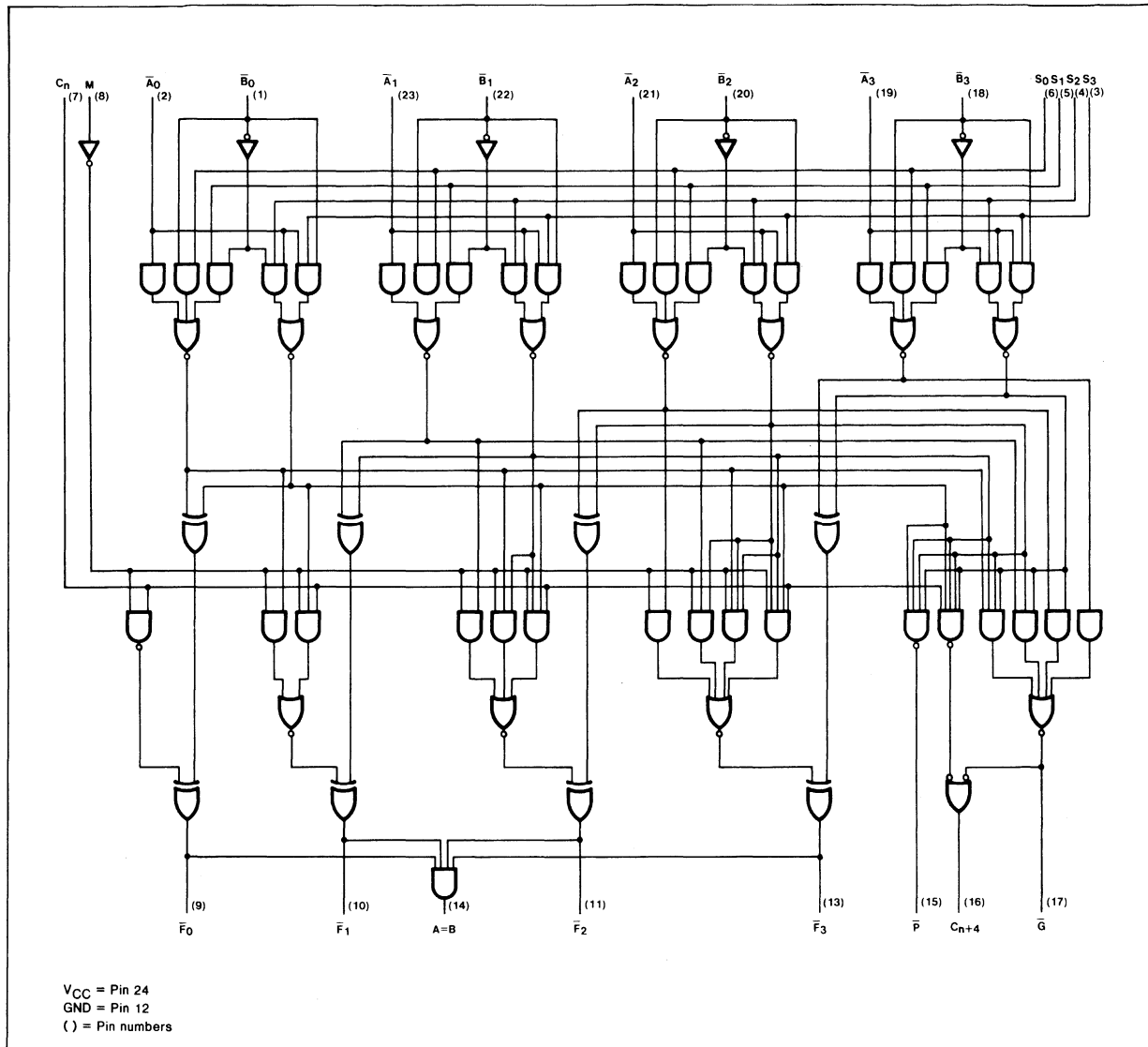
L = LOW voltage level
H = HIGH voltage level

*Each bit is shifted to the next more significant position
**Arithmetic operations expressed in 2s complement notation

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) ($C_n = L$)
L	L	L	L	\bar{A}	A minus 1
L	L	L	H	$\bar{A}\bar{B}$	AB minus 1
L	L	H	L	$\bar{A} + B$	AB minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\bar{A} + \bar{B}$	A plus (A + \bar{B})
L	H	L	H	\bar{B}	AB plus (A + \bar{B})
L	H	H	L	$\bar{A} \oplus \bar{B}$	A minus B minus 1
L	H	H	H	$A + \bar{B}$	A + \bar{B}
H	L	L	L	$\bar{A}\bar{B}$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$\bar{A}\bar{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	$\bar{A}\bar{B}$	AB plus A
H	H	H	L	AB	$\bar{A}\bar{B}$ plus A
H	H	H	H	A	A



LOGIC DIAGRAM



NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage for \bar{P} output	V _{CC} = Min, I _{OL}	Mil	0.4		0.5		0.6	V
	= See Fanout Table	Com	0.4		0.5		0.5	V
V _{OL} Output LOW voltage for \bar{G} output	V _{CC} = Min, I _{OL}	Mil	0.4		0.5		0.7	V
	= See Fanout Table	Com	0.4		0.5		0.7	V
I _{CC} Supply current	V _{CC} = Max	Mil	127		220		32	mA
	V \bar{B} = V _{Cn} = 0V	Com	140		220		34	mA
I _{CC} Supply current	V _{CC} = Max	Mil	135		220		35	mA
	V \bar{A} = V \bar{B} = V _{Cn} = 0V	Com	150		220		37	mA

AC CHARACTERISTICS: T_A = 25° (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay C _n to C _{n+4}	M=0V, Sum or Diff Mode See Figure 2 and Tables I & II		18 19		10.5 10.5		27 10	ns ns
t _{PLH} t _{PHL} Propagation delay C _n to \bar{F} outputs	M=0V, Sum or Diff Mode See Figure 2 and Tables I & II		19 18		12 12		26 20	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A} or \bar{B} inputs to \bar{G} output	M=S ₁ =S ₂ =0V, S ₀ =S ₃ =4.5V Sum Mode, See Figure 2 and Table I		19 19		12 12		29 23	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A} or \bar{B} inputs to \bar{G} output	M=S ₀ =S ₃ =0V, S ₁ =S ₂ =4.5V Diff Mode, See Figure 3 and Table II		25 25		15 15		32 32	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A} or \bar{B} inputs to \bar{P} output	M=S ₁ =S ₂ =0V, S ₀ =S ₃ =4.5V Sum Mode, See Figure 2 and Table I		19 25		12 12		30 30	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A} of \bar{B} inputs to \bar{P} output	M=S ₀ =S ₃ =0V, S ₁ =S ₂ =4.5V Diff Mode, See Figure 3 and Table II		25 25		15 15		30 33	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	M=S ₁ =S ₂ =0V, S ₀ =S ₃ =4.5V Sum Mode, See Figure 2 and Table I		42 32		16.5 16.5		32 20	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	M=S ₀ =S ₃ =0V, S ₁ =S ₂ =4.5V Diff Mode, See Figure 3 and Table II		48 34		20 22		32 32	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	M=4.5V, Logic Mode See Figure 2 and Table III		48 34		20 22		33 38	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A} of \bar{B} inputs to C _{n+4} output	M=0V, S ₀ =S ₃ =4.5V, S ₁ = S ₂ =0V. Sum Mode, See Figure 1 and Table 1		43 41		18.5 18.5		38 38	ns ns
t _{PLH} t _{PHL} Propagation Delay \bar{A} or \bar{B} inputs to C _{n+4} output	M=0V, S ₀ =S ₃ =0V, S ₁ =S ₂ = 4.5V. Diff Mode, See Figure 4 and Table II		50 50		23 23		41 41	ns ns
t _{PLH} t _{PHL} Propagation delay \bar{A} or \bar{B} inputs to A=B output	M=S ₀ =S ₃ =0V, S ₁ =S ₂ =4.5V Diff Mode, See Figure 3 and Table II		50 48		23 30		50 62	ns ns

SUM MODE TEST TABLE 1

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	$C_n + 4$
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or $C_n + 4$

DIFF MODE TEST TABLE II

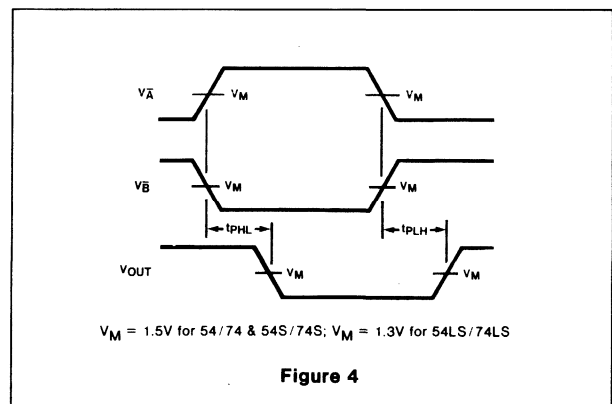
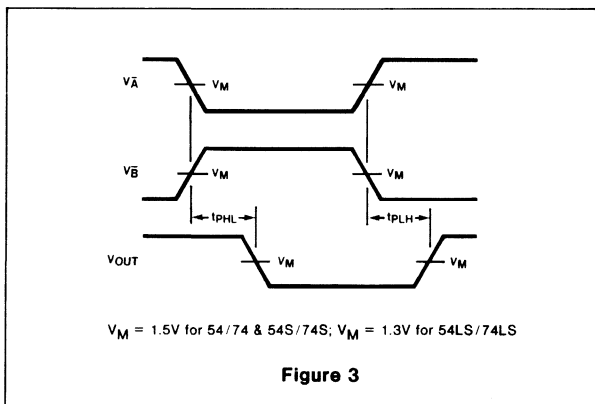
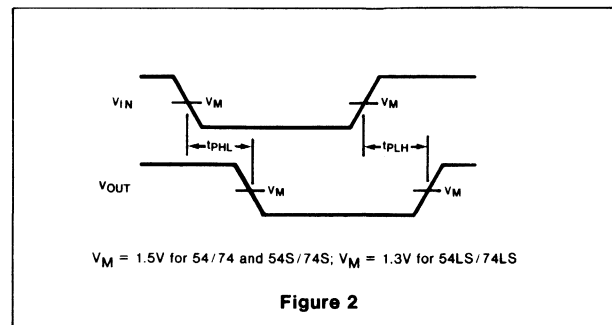
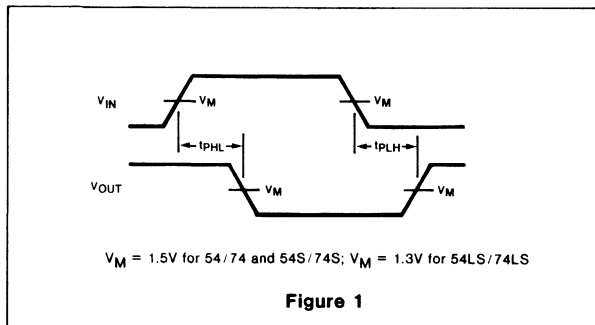
FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	$A = B$
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	$A = B$
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	$C_n + 4$
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All \bar{A} and \bar{B}	None	Any \bar{F} or $C_n + 4$

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	\overline{A}_i	\overline{B}_i	None	None	Remaining \overline{A} and \overline{B} , C_n	\overline{F}_i	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	\overline{B}_i	\overline{A}_i	None	None	Remaining \overline{A} and \overline{B} , C_n	\overline{F}_i	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

AC WAVEFORMS



54/74182
54S/74S182

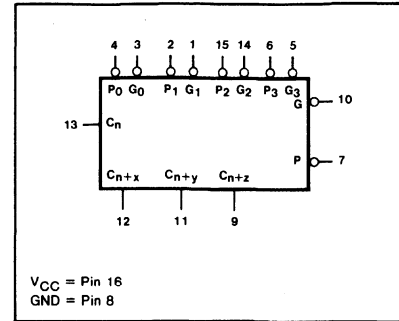
DESCRIPTION

The "182" is a high speed Carry Lookahead Generator. It is generally used with the "181", 2901-1, or other 4-bit Arithmetic Logic Units to provide high speed lookahead over word lengths of more than four bits. The "182" accepts up to four sets of Carry Generate functions, Carry Propagate functions, and a Carry input from four ALU's and provides the three Carry Out signals required by the ALU's. It also provides the next level auxiliary functions needed for further levels of lookahead.

FEATURES

- Provides carry lookahead across a group of four ALU's
- Multi-level lookahead for high speed arithmetic operation over long word lengths

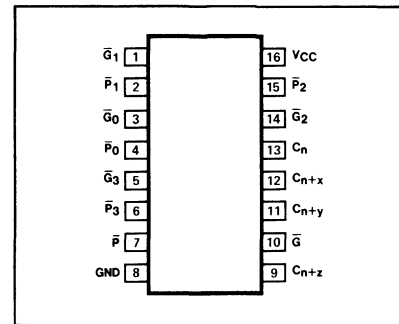
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	N74182N	•	N74S182N	
Ceramic DIP	N74182F	•	N74S182F	S54182F • S54S182W
Flatpak				S54182W • S54S182W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
C_n	Carry input	I_{IH} (μA)	80	50	
		I_{IL} (mA)	-3.2	-2.0	
\bar{P}_3	Carry Propagate (active LOW) input	I_{IH} (μA)	120	100	
		I_{IL} (mA)	-4.8	-4.0	
\bar{P}_2	Carry Propagate (active LOW) input	I_{IH} (μA)	160	150	
		I_{IL} (mA)	-6.4	-6.0	
\bar{P}_0, \bar{P}_1	Carry Propagate (active LOW) input	I_{IH} (μA)	200	200	
		I_{IL} (mA)	-8.0	-8.0	
\bar{G}_3	Carry Generate (active LOW) input	I_{IH} (μA)	200	200	
		I_{IL} (mA)	-8.0	-8.0	
\bar{G}_0, \bar{G}_2	Carry Generate (active LOW) input	I_{IH} (μA)	360	350	
		I_{IL} (mA)	-14.4	-14.0	
\bar{G}_1	Carry Generate (active LOW) input	I_{IH} (μA)	400	400	
		I_{IL} (mA)	-16.0	-16.0	
$C_{n+x}, C_{n+y}, C_{n+z}$	Carry outputs	I_{OH} (μA)	-800	-1000	
		I_{OL} (mA)	16	20	
\bar{P}	Carry Propagate (active LOW) output	I_{OH} (μA)	-800	-1000	
		I_{OL} (mA)	16	20	
\bar{G}	Carry Generate (active LOW) output	I_{OH} (μA)	-800	-100	
		I_{OL} (mA)	16	20	

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "182" carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\bar{P}_0, \bar{P}_1, \bar{P}_2, \bar{P}_3$) and Carry Generate ($\bar{G}_0, \bar{G}_1, \bar{G}_2, \bar{G}_3$) signals and an active HIGH Carry Input (C_n) and provides anticipated active HIGH carries ($C_{n+x}, C_{n+y}, C_{n+z}$) across four groups of binary adders. The "182" also has active LOW Carry Propagate (\bar{P}) and Carry Generate (\bar{G}) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_2 G_0 + P_2 P_1 P_0 C_n$$

$$G = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$$

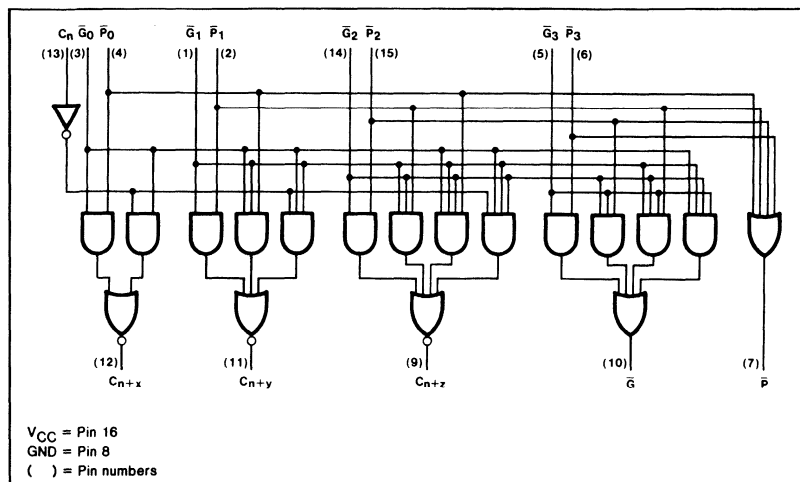
$$\bar{P} = P_3 P_2 P_1 P_0$$

Also, the "182" can also be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	\bar{G}_0	\bar{P}_0	\bar{G}_1	\bar{P}_1	\bar{G}_2	\bar{P}_2	\bar{G}_3	\bar{P}_3	C_{n+x}	C_{n+y}	C_{n+z}	\bar{G}	\bar{P}
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	X	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X	X				L		
X	H	H	H	X	H	X	X				L		
L	H	X	H	X	H	X	X				L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L	X				H		
X	L	X	X	L	X	L	X				H		
H	X	L	X	L	X	L	X				H		
	X		X	X	X	H	H					H	
	X		X	X	H	H	X					H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

LOGIC DIAGRAM



H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil		65		99		mA
		Com		72		109		mA

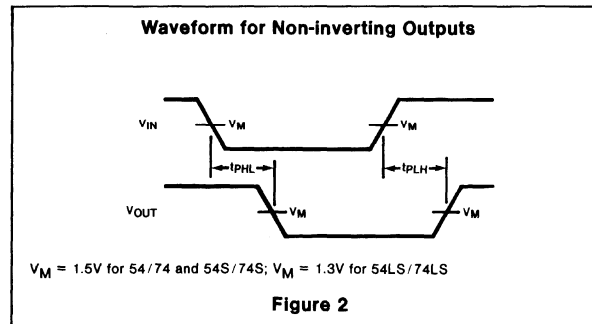
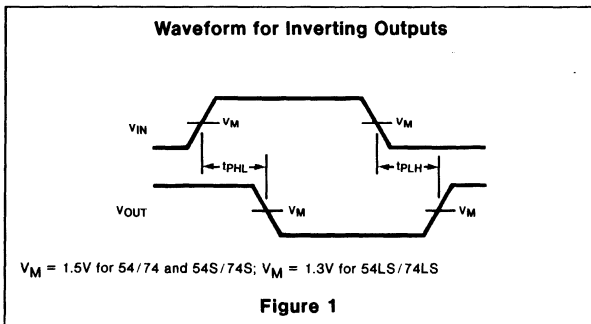
AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω		C _L = 15pF R _L = 280Ω				
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay \bar{G}_n or \bar{P}_n to any C output	Figure 1		17 22		7.0 7.0			ns ns
t _{PLH} t _{PHL} Propagation delay \bar{G}_n or \bar{P}_n to \bar{G} output	Figure 2		17 22		7.5 10.5			ns ns
t _{PLH} t _{PHL} Propagation delay \bar{P}_n to \bar{P} output	Figure 2		17 22		6.5 10			ns ns
t _{PLH} t _{PHL} Propagation delay C_n to any C output	Figure 2		17 22		10 10.5			ns ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54S/74S189
54LS/74LS189 (Preliminary data)

DESCRIPTION

The "189" is a 64-Bit high-speed Read/Write Random Access Memory for use as a "scratch pad" memory with non-destructive read-out. Memory cells are organized in a matrix to provide 16 words of four bits each. Four buffered Address (A_0 - A_3) inputs are decoded on the chip to select one of the sixteen memory words for read or write operations. Four buffered Data inputs (D_1 - D_4) and four 3-state data outputs are provided for versatile memory expansion. Data at the outputs is inverted from the data which was written into the memory. When the write mode is selected the outputs are in the high impedance "off" state.

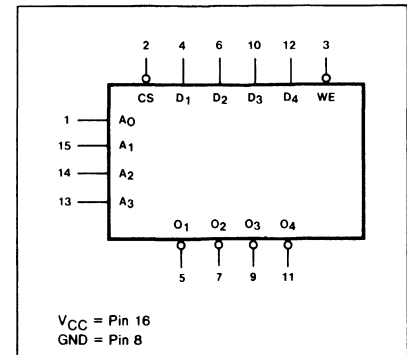
FEATURES

- 16-words by 4-bit memory
- On-chip address decoding
- Inverted data at outputs
- 3-State outputs for easy expansion

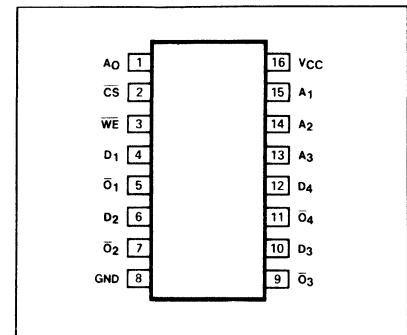
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	N74S189N	• N74LS189N		
Ceramic DIP	N74S189F	• N74LS189F	S54S189F	• S54LS189F
Flatpak				

LOGIC SYMBOL



PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_0 - A_3	Address inputs	I_{IH} (μA) I_{IL} (μA)		25/10 (a) -150/-100(a)	20 -100
\overline{CS}	Chip Select (active LOW) enable input	I_{IH} (μA) I_{IL} (μA)		25/10 (a) -150/-100(a)	20 -400
\overline{WE}	Write Enable (active LOW) input	I_{IH} (μA) I_{IL} (μA)		25/10 (a) 150/-100(a)	20 -400
D_1 - D_4	Data inputs	I_{IH} (μA) I_{IL} (μA)		25/10 (a) -150/-100 (a)	20 -400
\overline{O}_1 - \overline{O}_4	Data (inverting) outputs	I_{OH} (μA) I_{OL} (mA)		-2.0 16	-1/-2.6 (a) 12/24(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "189" is a high-speed array of 64 memory cells organized as 16 words of four bits each. A one-of-sixteen address decoder selects a single word which is specified by the four Address inputs (A_0-A_3). A READ operation is initiated after the address lines are stable when the Write Enable (\overline{WE}) input is HIGH and the Chip Select-Memory Enable (\overline{CS}) input is LOW. Data is read at the outputs inverted from the data which was written into the memory.

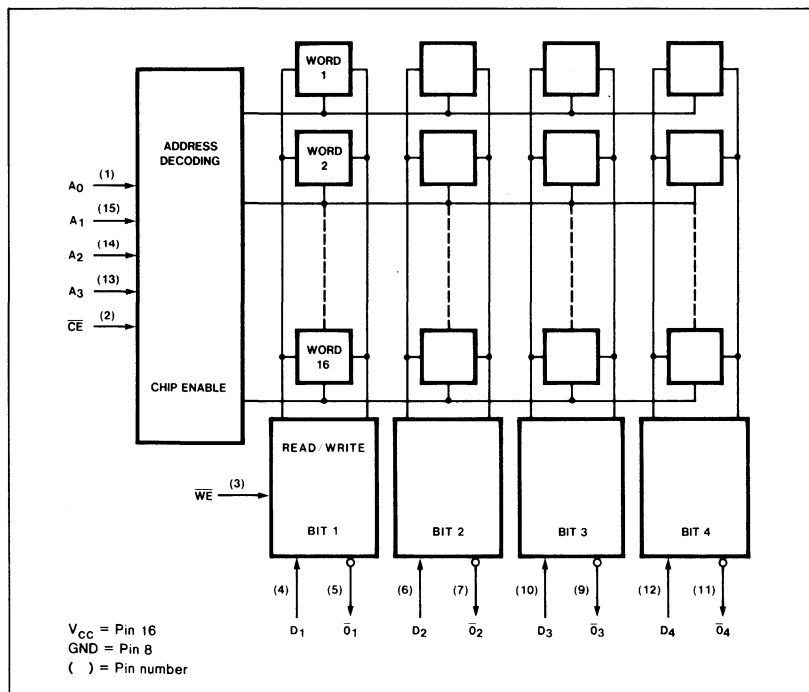
A WRITE operation requires that the \overline{WE} and \overline{CS} inputs be LOW. The address inputs must be stable during the WRITE mode for predictable operation. When the write mode is selected the outputs are in the high impedance "off" state. The selected memory cells are transparent to changes in the data during the WRITE mode. Therefore, data must be stable one setup time before the LOW-to-HIGH transition of \overline{CE} or \overline{WE} .

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	\overline{CS}	\overline{WE}	D_n	\overline{O}_n
Write - Disable Outputs	L	L	L	(Z)
	L	L	H	(Z)
Read	L	H	X	Data
Store - Disable Outputs	H	X	X	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 Data = Read complement of data from addressed word location
 (Z) = High impedance "off" state

BLOCK DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min, I _{OL} = 16mA	Mil			0.5			V
		Com			0.45			V
	V _{CC} = Min	I _{OL} = 12mA					0.4	V
		I _{OL} = 24mA					0.5(c)	V
V _{OH} Output HIGH voltage	V _{CC} = Min I _{OH} = See Fan-Out Table			2.4		2.4		V
I _{CC} Supply current	V _{CC} = Max	Mil			110		45	mA
		Com			110		37	mA

See BIPOLAR & MOS MEMORY DATA MANUAL for 54S/74S189 AC Characteristics

NOTES

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial Range only.

54/74190
54LS/74LS190

DESCRIPTION

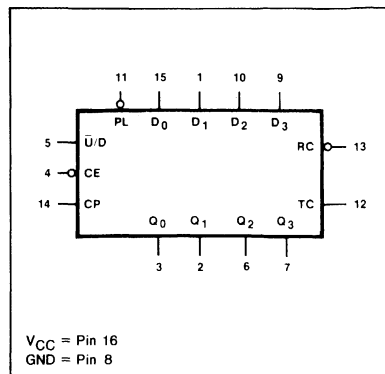
The "190" is a presettable BCD/Decade Up/Down Counter with state changes of the counter synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

The circuit features an asynchronous Parallel Load (\overline{PL}) input which overrides counting and loads the data present on the D_n inputs into the flip-flops. Synchronous expansion in a multistage counter is made possible by a Count Enable (\overline{CE}) input. The count up or count down mode is determined by an Up/Down ($\overline{U/D}$) input. A variety of methods for generating carry/borrow signals in multistage counter application is made possible by Terminal Count (TC) and Ripple Clock (\overline{RC}) outputs.

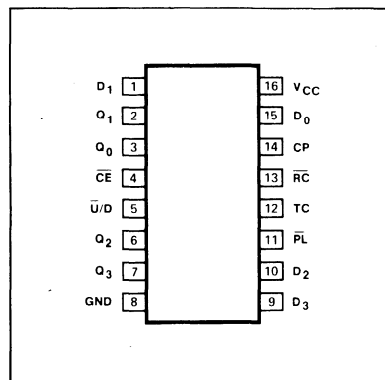
FEATURES

- Synchronous, reversible BCD/Decade counting
- Asynchronous parallel load capability
- Count enable control for synchronous expansion
- Single Up/Down control input

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74190N • N74LS190N	
Ceramic DIP	N74190F • N74LS190F	S54190F • S54LS190F
Flatpak		S54190W • S54LS190W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock Pulse (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
\overline{CE}	Clock Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)	120 -4.8		60 -1.2
$\overline{U/D}$	Up/Down count control input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
\overline{PL}	Parallel Load (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
D_n	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
Q_n	Counter outputs	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)
TC	Terminal Count output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)
\overline{RC}	Ripple Clock (active LOW pulse) output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "190" is an asynchronously presettable Up/Down BCD Decade Counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D₀-D₃) is loaded into the counter and appears on the outputs when the Parallel Load (\overline{PL}) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable (\overline{CE}) input. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the Clock input. The Up/Down ($\overline{U/D}$) input signal determines the direction of counting as indicated in the Mode Select Table. The \overline{CE} input may go LOW when the clock is in either state, however, the LOW-to-HIGH \overline{CE} transition must occur only while the Clock is HIGH. Also, the $\overline{U/D}$ input should be changed only when either \overline{CE} or CP is HIGH.

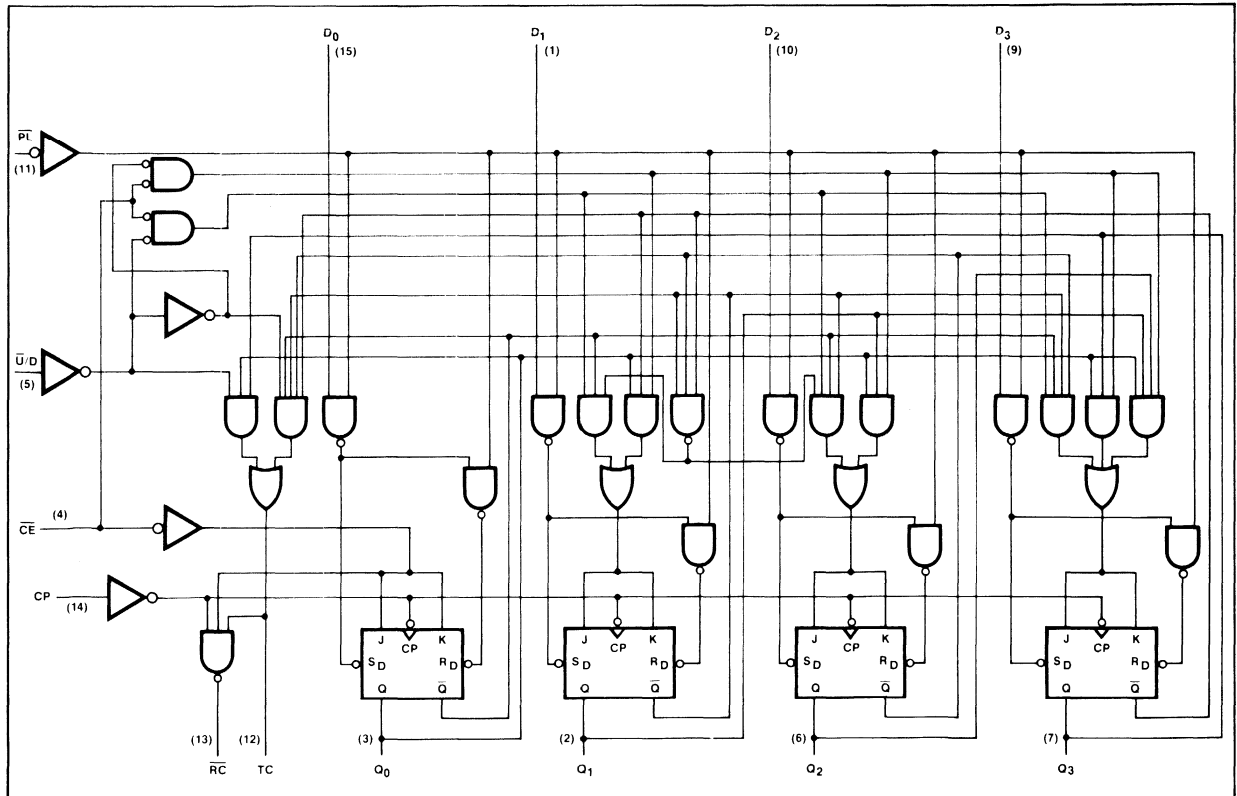
MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	\overline{PL}	$\overline{U/D}$	\overline{CE}	CP	D _n	Q _n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	↓	↑	X	count up
Count down	H	H	↓	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND \overline{RC} TRUTH TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	\overline{CE}	CP	Q ₀	Q ₁	Q ₂	Q ₃	TC	\overline{RC}
H	X	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⌋	H	X	X	H	H	⌋
L	X	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌋	L	L	L	L	H	⌋

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 ⌋ = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.
 ⌋ = LOW pulse.



Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock (RC). The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until \bar{U}/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the Ripple Clock (RC) output. When TC is HIGH and \bar{CE} is LOW, the Ripple Clock follows the Clock Pulse (CP) delayed by two gate delays. The RC output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multi-stage counters as indicated in Figures A and B. In Figure A, each RC output is used as the clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on \bar{CE} inhibits the RC output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure B shows a method of causing state changes to occur simultaneously in all stages. The RC outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. The LOW state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the RC

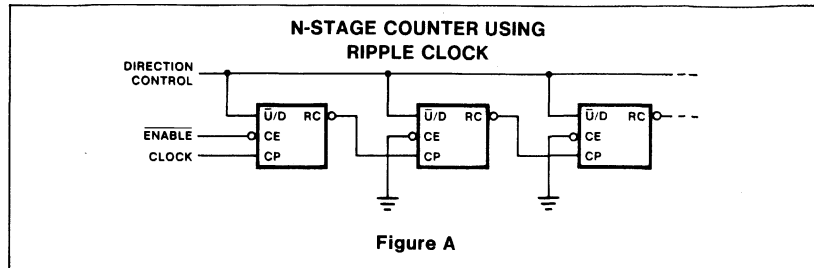


Figure A

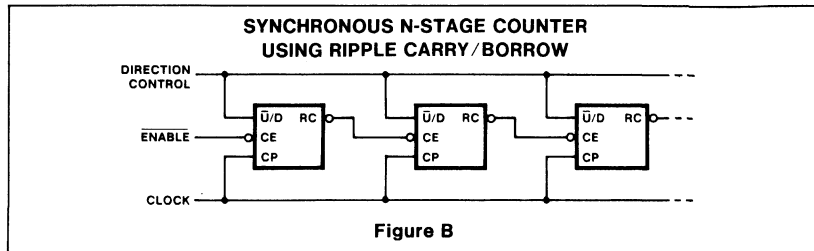


Figure B

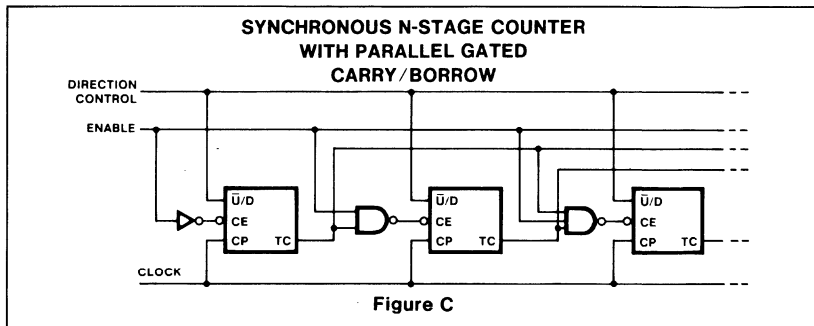


Figure C

output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

In Figure C the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the

preceding stages forms the \bar{CE} input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own \bar{CE} therefore the simple inhibit scheme of Figure A and B does not apply.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max		
I _{CC} Supply current	V _{CC} = Max	Mil	99				35	mA	
		Com	105				35	mA	
I _{OS} Output short circuit current	V _{CC} = Max	Mil	-20	-65			-15	-100	mA
		Com	-18	-65			-15	-100	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

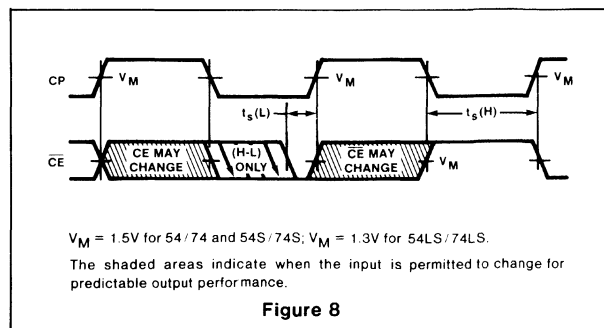
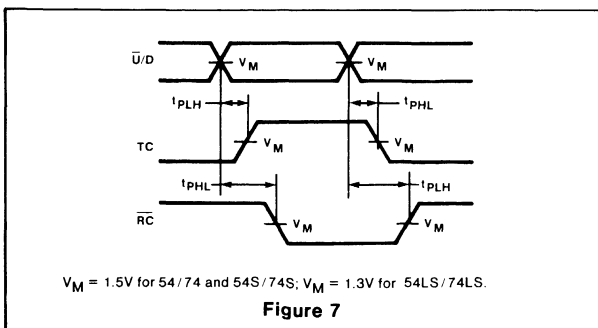
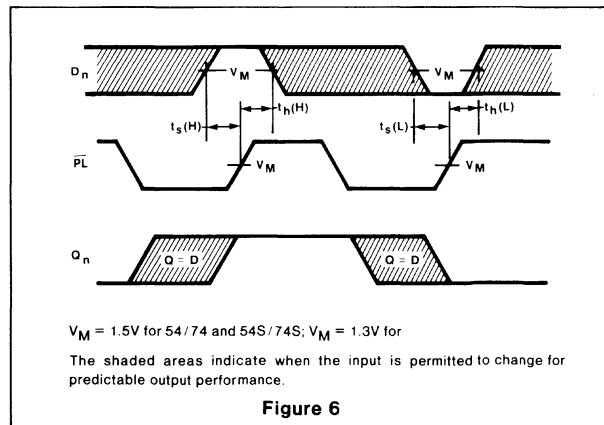
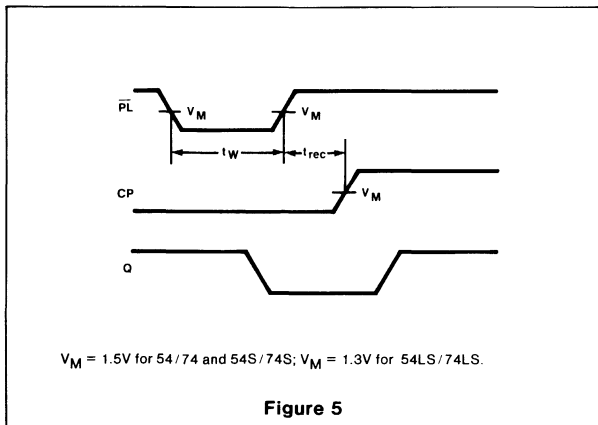
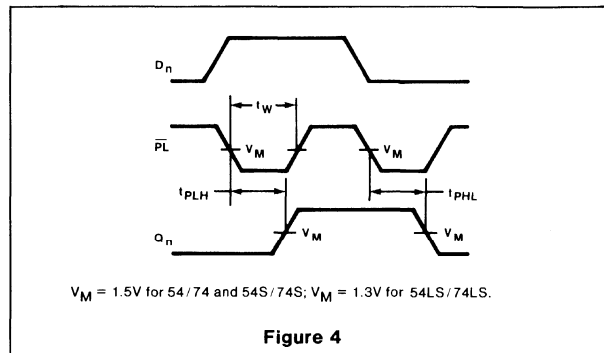
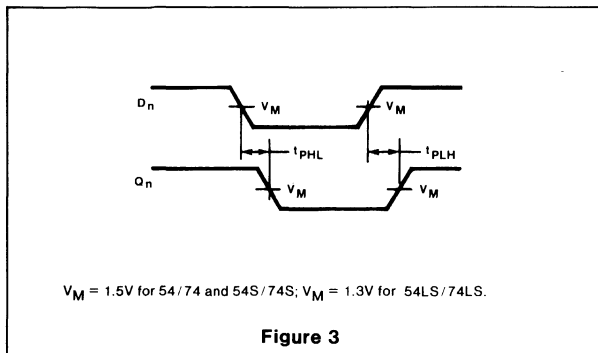
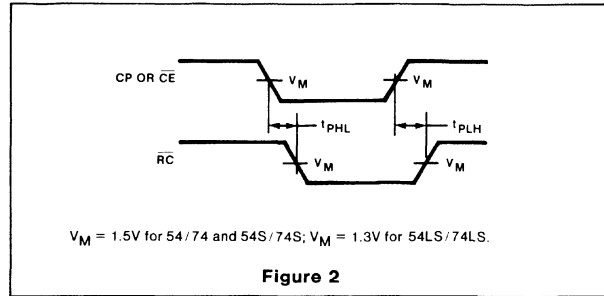
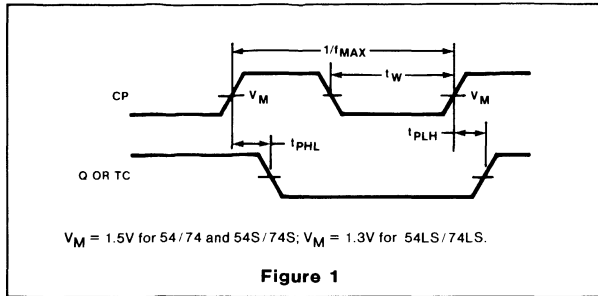
AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$				$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum input count frequency	Figure 1	20				20		MHz
t_{PLH} Propagation delay, t_{PHL} Clock to Q outputs	Figure 1		24 36				24 36	ns ns
t_{PLH} Propagation delay t_{PHL} Clock to $\overline{\text{RC}}$ output	Figure 2		20 24				20 24	ns ns
t_{PLH} Propagation delay t_{PHL} Clock to TC output	Figure 1		42 52				42 52	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{U/D}}$ to $\overline{\text{RC}}$ output	Figure 7		45 45				45 45	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{U/D}}$ to TC output	Figure 7		33 33				33 33	ns ns
t_{PLH} Propagation delay t_{PHL} Data to Q outputs	Figure 3		22 50				32 40	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{PL}}$ to any output	Figure 4		33 50				33 50	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CE}}$ to $\overline{\text{RC}}$ output	Figure 2		33 33				33 33	ns ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w CP pulse width	Figure 1	25				25		ns
t_w $\overline{\text{PL}}$ pulse width	Figure 5	35				35		ns
t_s Setup time Data to $\overline{\text{PL}}$	Figure 6	20				20		ns
t_h Hold time Data to $\overline{\text{PL}}$	Figure 6	0				0		ns
t_{rec} Recovery time $\overline{\text{PL}}$ to CP	Figure 5	40				40		ns
$t_s(\text{L})$ Setup time LOW $\overline{\text{CE}}$ to clock	Figure 8	40				40		ns
$t_h(\text{L})$ Hold time LOW $\overline{\text{CE}}$ to Clock	Figure 8	0				0		ns

AC WAVEFORMS



**54/74191
54LS/74LS191**

DESCRIPTION

The "191" is a presettable 4-Bit Binary Up/Down Counter with state changes of the counter synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

The circuit features an asynchronous Parallel Load (\overline{PL}) input which overrides counting and loads the data present on the D_n inputs into the flip-flops. Synchronous expansion in a multistage counter is made possible by a Count Enable (\overline{CE}) input. The count up or count down mode is determined by an Up/Down ($\overline{U/D}$) input. A variety of methods for generating carry/borrow signals in multistage counter application is made possible by Terminal Count (TC) and Ripple Clock (\overline{RC}) outputs.

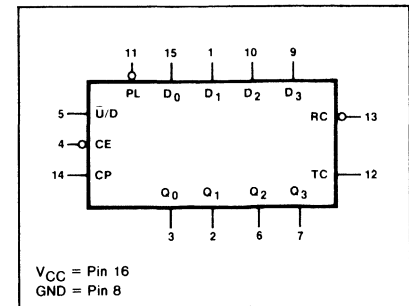
FEATURES

- Synchronous, reversible 4-bit binary counting
- Asynchronous parallel load capability
- Count Enable control for synchronous expansion
- Single Up/Down control input

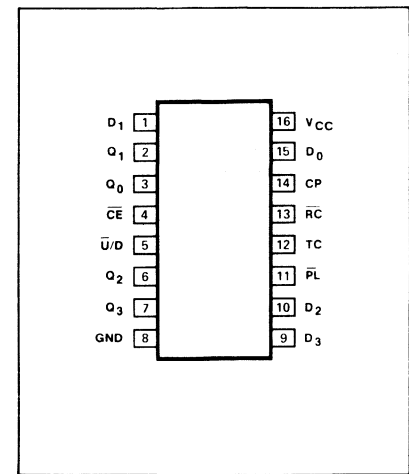
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N74191N	• N74LS191N	
Ceramic DIP	N74191F	• N74LS191F	S54191F	• S54LS191F
Flatpak			S54191W	• S54LS191W

LOGIC SYMBOL



PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock Pulse (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
\overline{CE}	Clock Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)	120 -4.8		60 -1.2
$\overline{U/D}$	Up/Down count control input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
\overline{PL}	Parallel Load (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
D_n	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
Q_n	Counter outputs	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)
TC	Terminal Count output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)
\overline{RC}	Ripple Clock (active LOW pulse) output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "191" is an asynchronously presettable Up/Down 4-Bit Binary Counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load (\overline{PL}) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable (\overline{CE}) input. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the Clock input. The Up/Down ($\overline{U/D}$) input signal determines the direction of counting as indicated in the Mode Select Table. The \overline{CE} input may go LOW when the clock is in either state, however, the LOW-to-HIGH \overline{CE} transition must occur only while the Clock is HIGH. Also, the $\overline{U/D}$ input should be changed only when either \overline{CE} or CP is HIGH.

MODE SELECT-FUNCTION TABLE

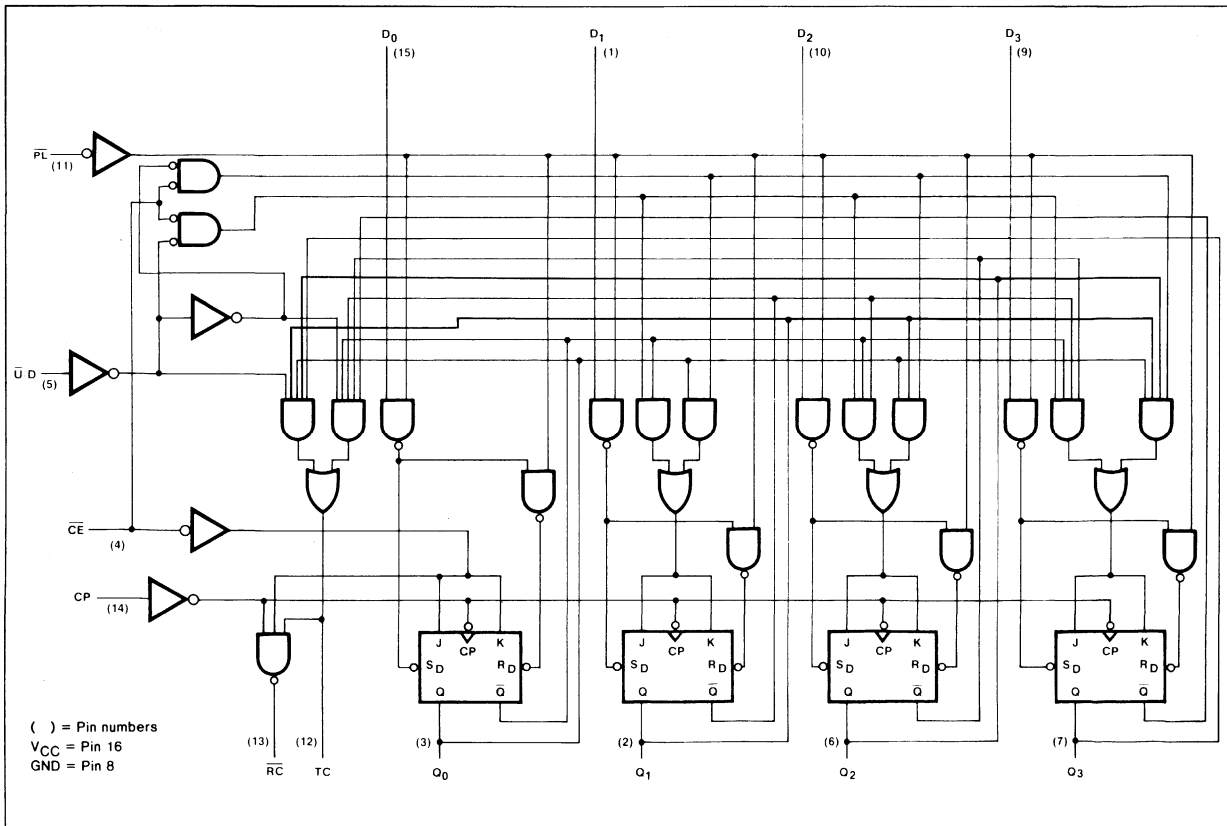
OPERATING MODE	INPUTS					OUTPUTS
	\overline{PL}	$\overline{U/D}$	\overline{CE}	CP	D_n	
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	I	↑	X	count up
Count down	H	H	I	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND \overline{RC} TRUTH TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	\overline{CE}	CP	Q_0	Q_1	Q_2	Q_3	TC	\overline{RC}
H	X	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⌋	H	H	H	H	H	⌋
L	X	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌋	L	L	L	L	H	⌋

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 I = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.
 ⌋ = LOW pulse.

LOGIC DIAGRAM



Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock (RC). The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "15" in the count-up mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until U/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the Ripple Clock (RC) output. When TC is HIGH and CE is LOW, the Ripple Clock follows the Clock Pulse (CP) delayed by two gate delays. The RC output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multi-stage counters as indicated in Figures A and B. In Figure A, each RC output is used as the clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on CE inhibits the RC output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure B shows a method of causing state changes to occur simultaneously in all stages. The RC outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. The LOW state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the RC

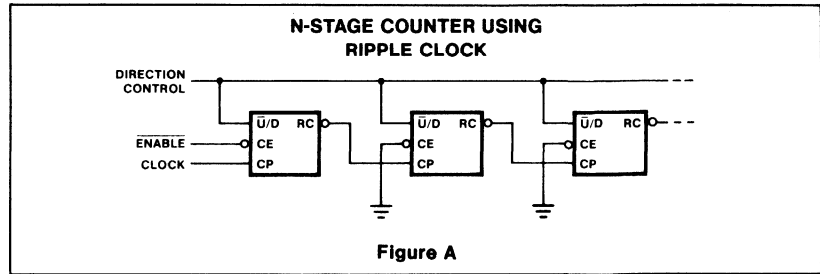


Figure A

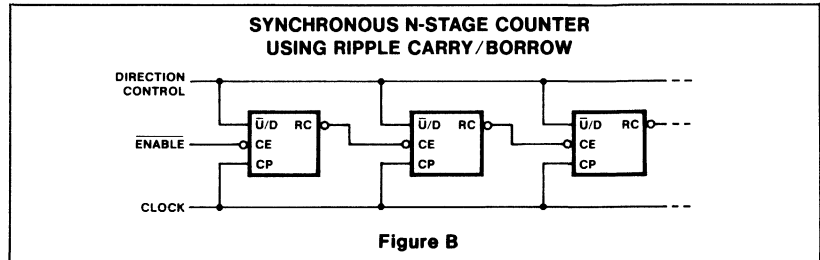


Figure B

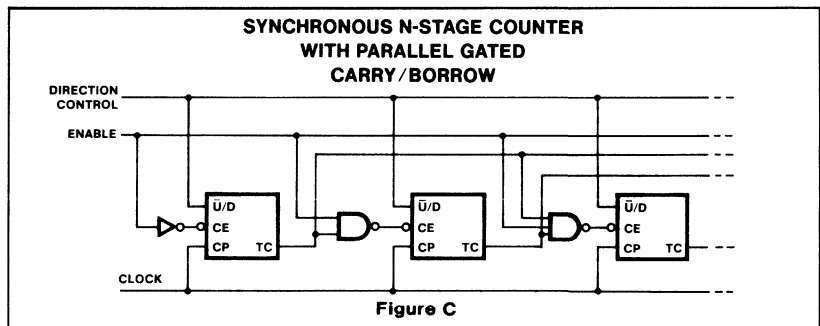


Figure C

output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

In Figure C the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the

preceding stages forms the CE input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own CE therefore the simple inhibit scheme of Figure A and B does not apply.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{OS} Output short circuit current	V _{CC} = Max	Mil	-20	-65		-15	-100	mA
		Com	-18	-65		-15	-100	mA
I _{CC} Supply current	V _{CC} = Max	Mil		99			35	mA
		Com		105			35	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

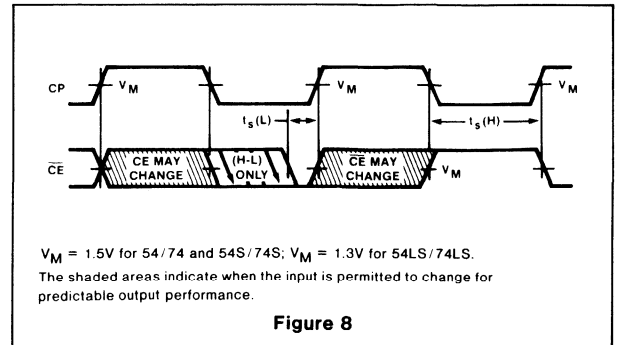
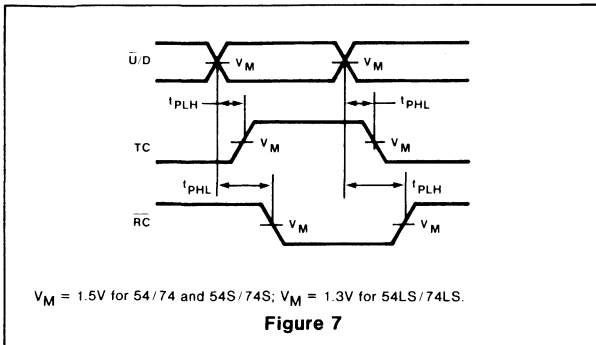
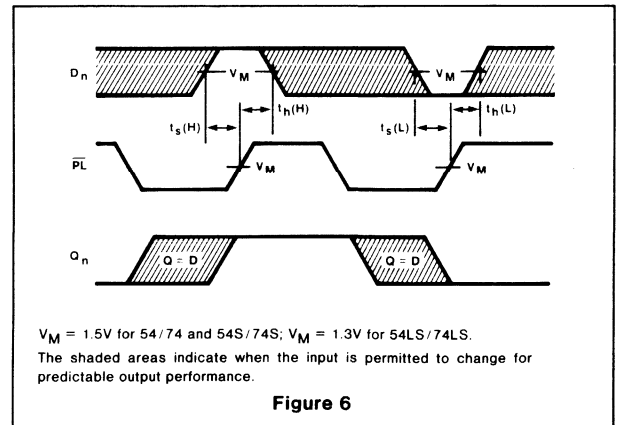
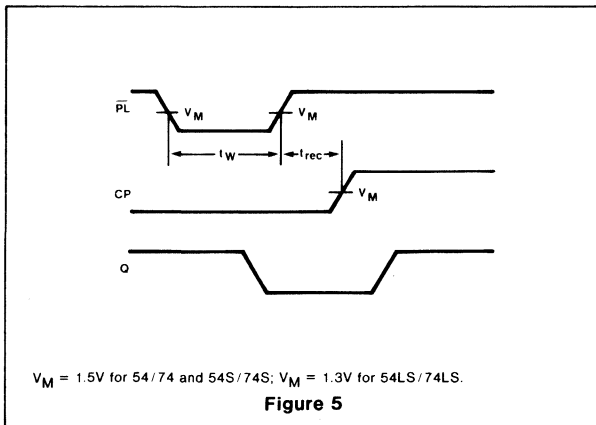
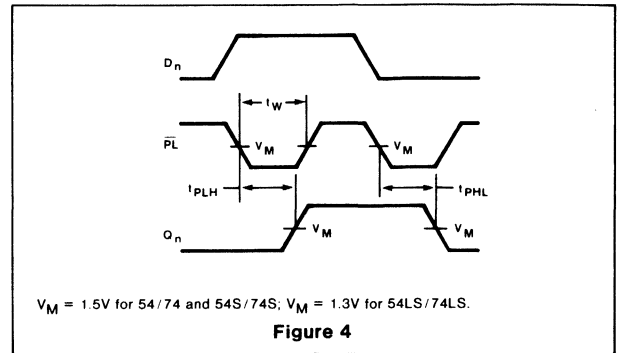
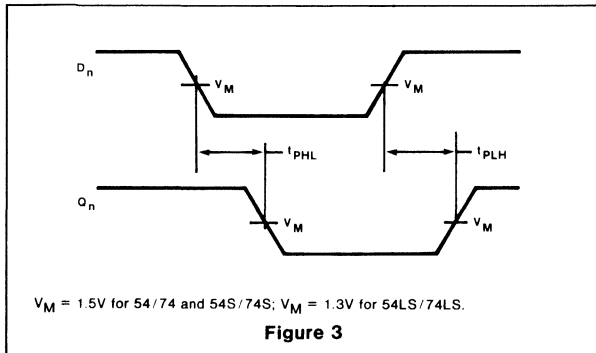
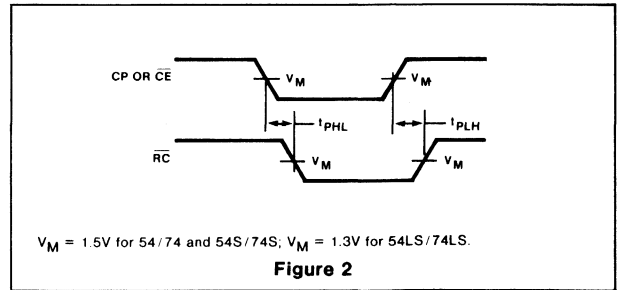
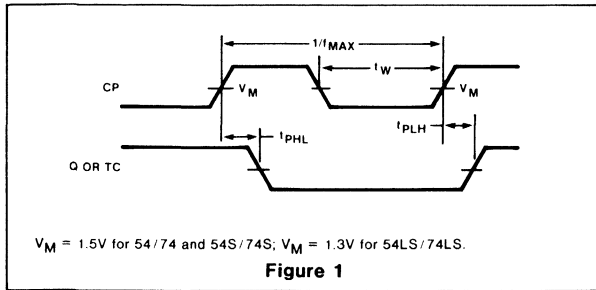
AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$				$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum input count frequency	Figure 1	20				20		MHz
t_{PLH} Propagation delay, t_{PHL} Clock to Q outputs	Figure 1		24 36				24 36	ns ns
t_{PLH} Propagation delay, t_{PHL} Clock to $\overline{\text{RC}}$ output	Figure 2		20 24				20 24	ns ns
t_{PLH} Propagation delay, t_{PHL} Clock to TC output	Figure 1		42 52				42 52	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{U}}/\text{D}$ to $\overline{\text{RC}}$ output	Figure 7		45 45				45 45	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{U}}/\text{D}$ to TC output	Figure 7		33 33				33 33	ns ns
t_{PLH} Propagation delay t_{PHL} Data to Q outputs	Figure 3		22 50				32 40	ns ns
t_{PLH} Propagation delay t_{PHL} PL to any output	Figure 4		33 50				33 50	ns ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CE}}$ to $\overline{\text{RC}}$ output	Figure 2		33 33				33 33	ns ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w CP pulse width	Figure 1	25				25		ns
t_w $\overline{\text{PL}}$ pulse width	Figure 5	35				35		ns
t_s Setup time Data to $\overline{\text{PL}}$	Figure 6	20				20		ns
t_h Hold time Data to $\overline{\text{PL}}$	Figure 6	0				0		ns
t_{rec} Recovery time $\overline{\text{PL}}$ to CP	Figure 5	40				40		ns
$t_{s(L)}$ Setup time LOW $\overline{\text{CE}}$ to clock	Figure 8	40				40		ns
$t_{h(L)}$ Hold time LOW $\overline{\text{CE}}$ to Clock	Figure 8	0				0		ns

AC WAVEFORMS



54/74192
54LS/74LS192

DESCRIPTION

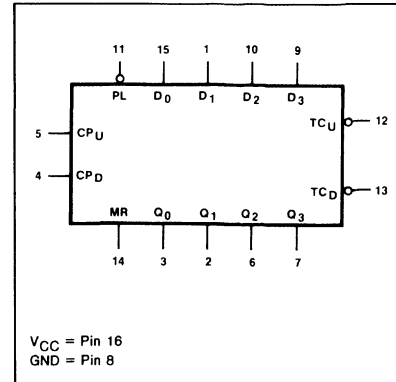
The "192" is an Up/Down BCD Decade Counter featuring separate Count Up and Count Down Clocks. The individual circuits operate synchronously in either counting mode changing state on the LOW-to-HIGH transitions on the clock inputs.

To simplify multistage counter designs separate Terminal Count Up and Terminal Count Down outputs are provided which are used as clocks for subsequent stages without extra logic. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load (PL) and the Master Reset (MR) inputs override the clocks and asynchronously load or clear the counter.

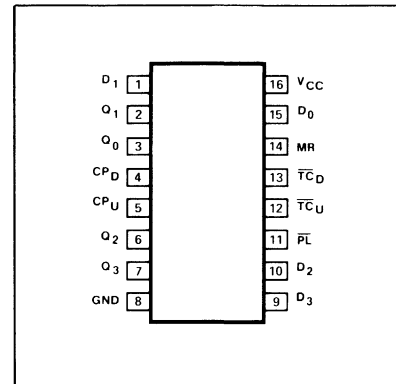
FEATURES

- Synchronous reversible decade counting
- Asynchronous parallel load
- Asynchronous reset (clear)
- Expandable without external logic

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74192N • N74LS192N	
Ceramic DIP	N74192F • N74LS192F	S54192F • S54LS192F
Flatpak		S54192W • S54LS192W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CPU	Count up Clock Pulse input	I _H (μA)	40		20
		I _L (mA)	-1.6		-0.4
CPD	Count down Clock Pulse input	I _H (μA)	40		20
		I _L (mA)	-1.6		-0.4
MR	Master Reset (active HIGH) input	I _H (μA)	40		20
		I _L (mA)	-1.6		-0.4
PL	Parallel Load (active LOW) input	I _H (μA)	40		20
		I _L (mA)	-1.6		-0.4
D _n	Parallel Data inputs	I _H (μA)	40		20
		I _L (mA)	-1.6		-0.4
Q _n	Counter outputs	I _{OH} (μA)	-400		-400
		I _{OL} (mA)	16		4/8(a)
TCU	Terminal Count up (carry) output	I _{OH} (μA)	-400		-400
		I _{OL} (mA)	16		4/8(a)
TCD	Terminal Count down (borrow) output	I _{OL} (μA)	-400		-400
		I _{OH} (mA)	16		4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "192" is an asynchronously presettable Up/Down (reversible) Decade Counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous Master Reset (clear) and Parallel load, and synchronous Count up and Count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on the clock inputs causes the Q outputs to change state synchronously. A LOW-to-HIGH transition on the Count Down Clock Pulse (CP_D) input will decrease the count by one, while a similar transition on the Count Up Clock Pulse (CP_U) input will advance the count by one. One clock should be held HIGH while counting with the other, because the circuit will either count by twos

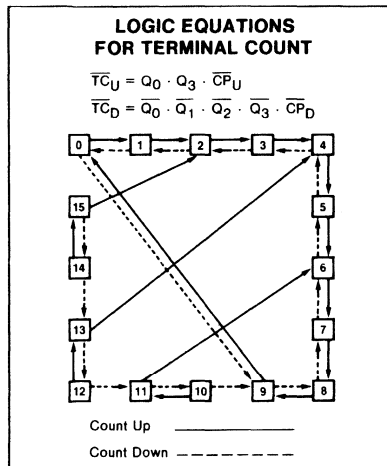
or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally HIGH. When the circuit has reached the maximum count state of "9," the next HIGH-to-LOW transition of CP_U will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, duplicating the Count Up Clock although delayed by two gate delays. Likewise, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The \overline{TC} outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they

duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D₀-D₃) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load (\overline{PL}) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and set all Q outputs LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

STATE DIAGRAM



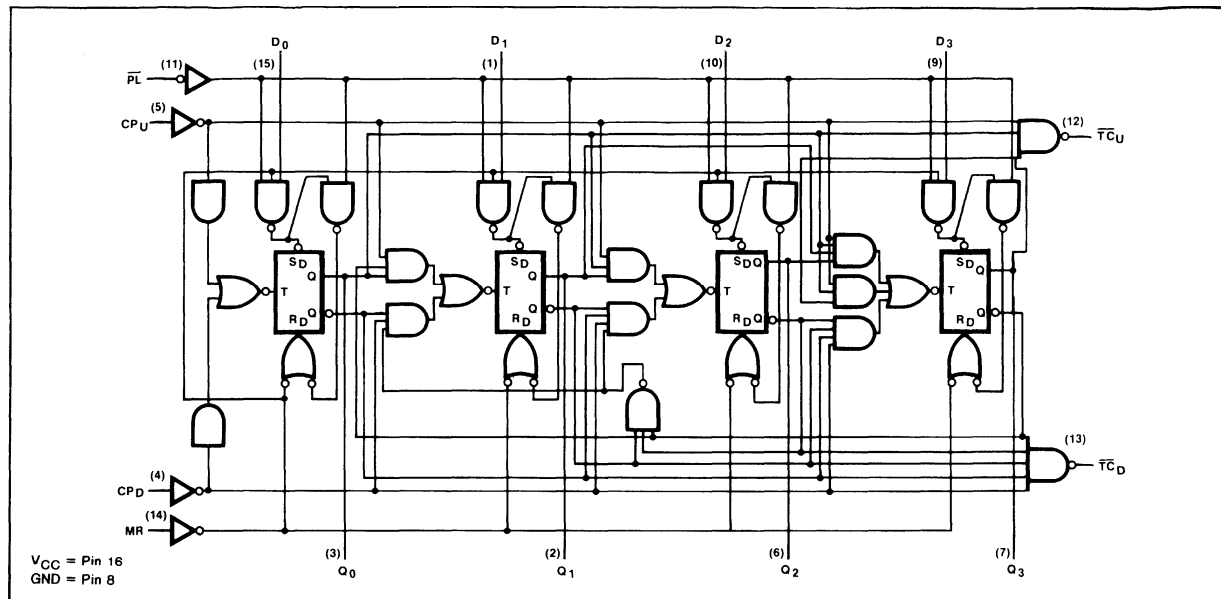
MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	\overline{PL}	CP _U	CP _D	D ₀	D ₁	D ₂	D ₃	Q ₀	Q ₁	Q ₂	Q ₃	\overline{TC}_U	\overline{TC}_D
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	Q _n =D _n				L	H
	L	L	H	X	H	X	X	H	Q _n =D _n				H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H ^(b)	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H ^(c)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

- NOTES
b. \overline{TC}_U = CP_U at terminal count up (HLLH)
c. \overline{TC}_D = CP_D at terminal count down (LLLL)

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(d)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{OS} Output short circuit current	V _{CC} = Max	Mil	-20	-65		-15	-100	mA
		Com	-18	-65		-15	-100	mA
I _{CC} Supply current	V _{CC} = Max	Mil		89		34		mA
		Com		102		34		mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω		C _L = 15pF R _L = 2kΩ		C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum input count frequency	Figure 1	25				25		MHz
t _{PLH} Propagation delay t _{PHL} CPU input to TC _U output	Figure 2		26 24				26 24	ns ns
t _{PLH} Propagation delay t _{PHL} CPD input to TC _D output	Figure 2		24 24				24 24	ns ns
t _{PLH} Propagation delay t _{PHL} CPU or CPD to Q _n output	Figure 1		38 47				38 47	ns ns
t _{PLH} Propagation delay t _{PHL} PL input to Q _n output	Figure 3		40 40				40 40	ns ns
t _{PHL} Propagation delay MR to output	Figure 4		35				35	ns

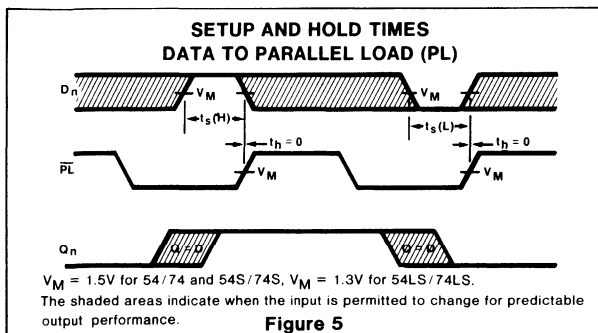
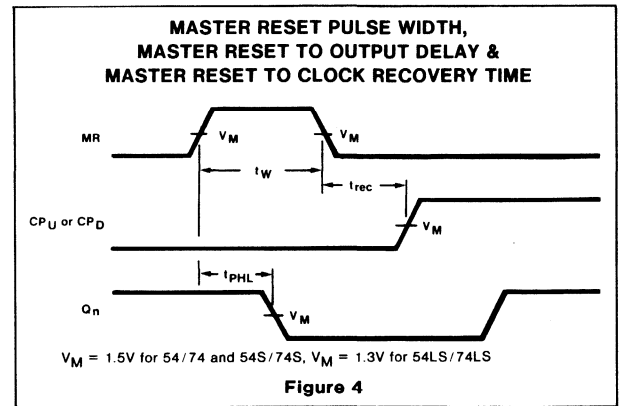
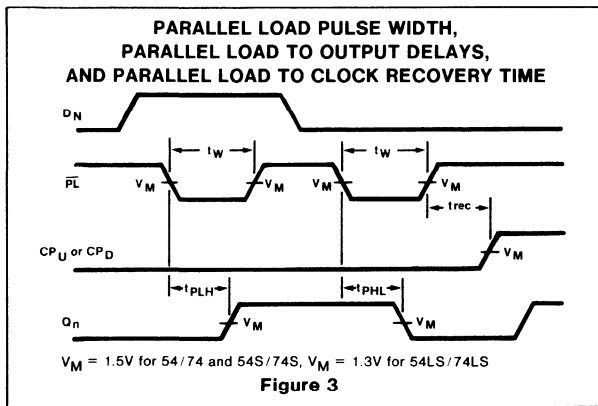
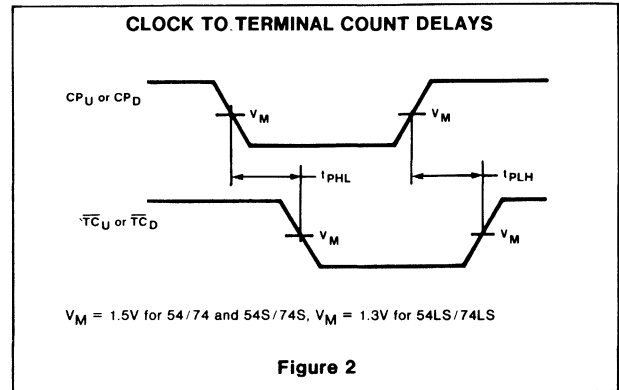
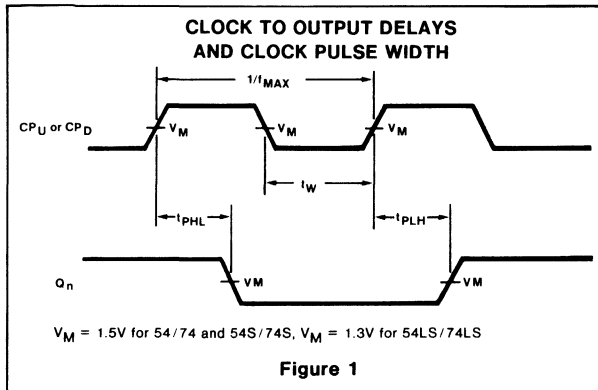
NOTE

d. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w	CP_U pulse width					20		ns
t_w	CP_D pulse width					20		ns
t_w	PL pulse width					20		ns
t_w	MR pulse width					20		ns
t_s	Setup time Data to \overline{PL}					20		ns
t_h	Hold time Data to \overline{PL}					0		ns
t_{rec}	Recovery time, \overline{PL} to CP					40		ns
t_{rec}	Recovery time, MR to CP					40		ns

AC WAVEFORMS



54/74193
54LS/74LS193

DESCRIPTION

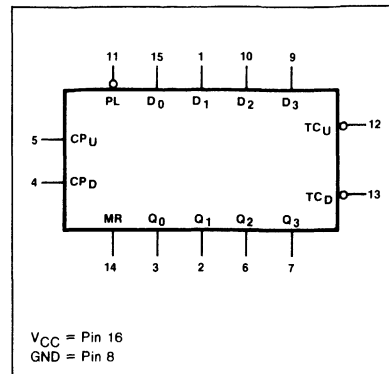
The "193" is an Up/Down Modulo-16 Binary Counter utilizing separate Count Up and Count Down Clocks. The individual circuits operate synchronously in either counting mode changing state on the LOW-to-HIGH transitions on the clock inputs.

To simplify multistage counter designs separate Terminal Count Up and Terminal Count Down outputs are provided which are used as clocks for subsequent stages without extra logic. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load (PL) and the Master Reset (MR) inputs override the clocks and asynchronously load or clear the counter.

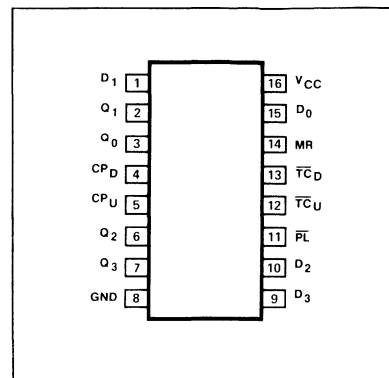
FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset (clear)
- Expandable without external logic

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C		MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C	
	Plastic DIP	N74193N	• N74LS193N	
Ceramic DIP	N74193F	• N74LS193F	S54193F	• S54LS193F
Flatpak			S54193W	• S54LS193W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP _U	Count up Clock Pulse input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
CP _D	Count down Clock Pulse input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
MR	Master Reset (active HIGH) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
\overline{PL}	Parallel Load (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
D _n	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
Q _n	Counter outputs	I _{OH} (μA) I _{OL} (mA)	-400 16		-400 4/8(a)
\overline{TC}_U	Terminal Count up (carry) output	I _{OH} (μA) I _{OL} (mA)	-400 16		-400 4/8(a)
\overline{TC}_D	Terminal Count down (borrow) output	I _{OH} (μA) I _{OL} (mA)	-400 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "193" is an asynchronously presettable, Up/Down (reversible) 4-Bit Binary Counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous Master Reset (clear) and Parallel load, and synchronous Count-up and Count-down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on the clock inputs causes the Q outputs to change state synchronously. A LOW-to-HIGH transition on the Count Down Clock Pulse (CP_D) input will decrease the count by one, while a similar transition on the Count Up Clock Pulse (CP_U) input will advance the count by one. One clock should be held HIGH while counting with the other, because the circuit will either count by twos

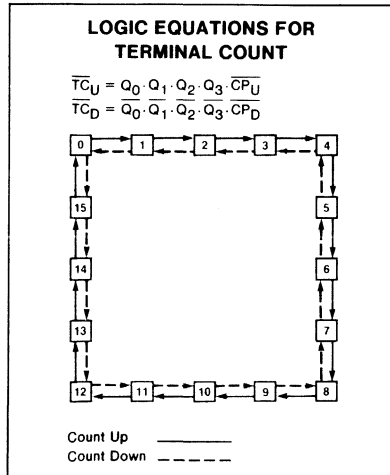
or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The Terminal Count Up (\overline{TC}_U) and Terminal Count Down (\overline{TC}_D) outputs are normally HIGH. When the circuit has reached the maximum count state of "15", the next HIGH-to-LOW transition of CP_U will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, duplicating the Count Up Clock although delayed by two gate delays. Likewise, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The \overline{TC} outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they

duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D₀-D₃) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load (PL) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and set all Q outputs LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

STATE DIAGRAM



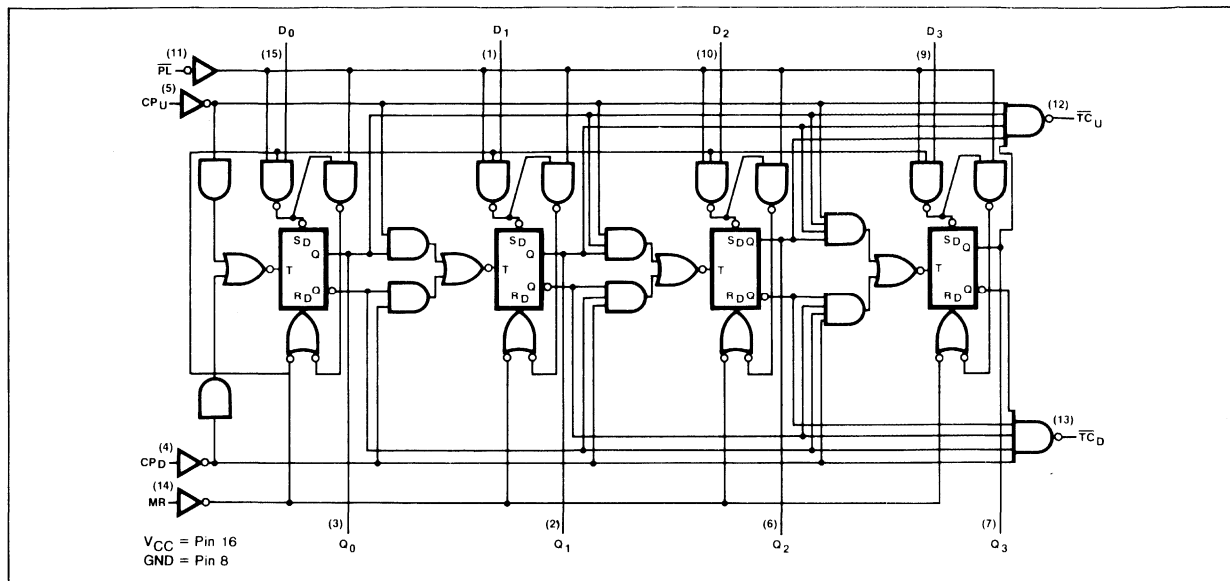
MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	MR	\overline{PL}	CP _U	CP _D	D ₀ , D ₁ , D ₂ , D ₃	Q ₀ , Q ₁ , Q ₂ , Q ₃	\overline{TC}_U	\overline{TC}_D	
Reset (clear)	H	X	X	L	X X X X	L L L L	H	L	
	H	X	X	H	X X X X	L L L L	H	H	
Parallel load	L	L	X	L	L L L L	L L L L	H	L	
	L	L	X	H	L L L L	L L L L	H	H	
	L	L	L	X	H H H H	H H H H	L	H	
	L	L	H	X	H H H H	H H H H	H	H	
Count up	L	H	↑	H	X X X X	Count up	H ^(b)	H	
Count down	L	H	H	↑	X X X X	Count down	H	H ^(c)	

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

NOTES
b. $\overline{TC}_U = CP_U$ at terminal count up (HHHH)
c. $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(d)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max		
I _{OS} Output short circuit current	V _{CC} = Max	Mil	-20	-65			-15	-100	mA
		Com	-18	-65			-15	-100	mA
I _{CC} Supply current	V _{CC} = Max	Mil		89			34	mA	
		Com		102			34	mA	

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum input count frequency	Figure 1	25				25		MHz
t _{PLH} Propagation delay t _{PHL} CPU input to TC _U output	Figure 2		26 24				26 24	ns ns
t _{PLH} Propagation delay t _{PHL} CP _D input to TC _D output	Figure 2		24 24				24 24	ns ns
t _{PLH} Propagation delay t _{PHL} CPU or CP _D to Q _n outputs	Figure 1		38 47				38 47	ns ns
t _{PLH} Propagation delay t _{PHL} PL input to Q _n output	Figure 3		40 40				40 40	ns ns
t _{PHL} Propagation delay MR to output	Figure 4		35				35	ns

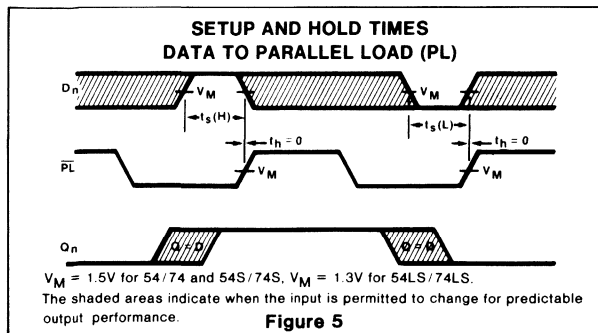
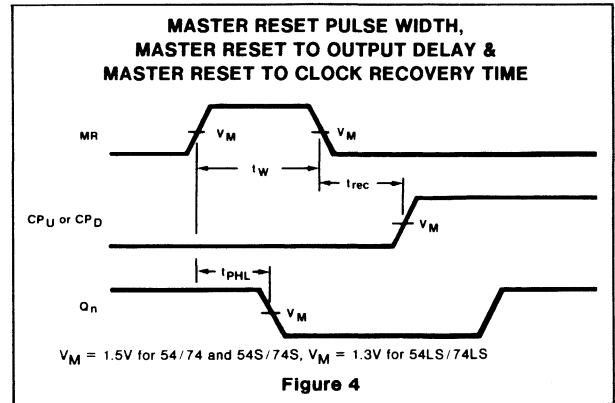
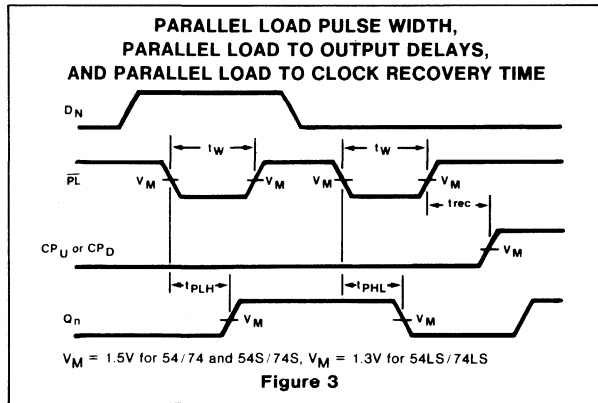
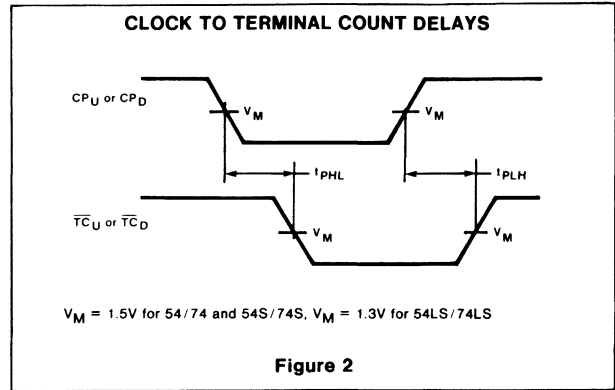
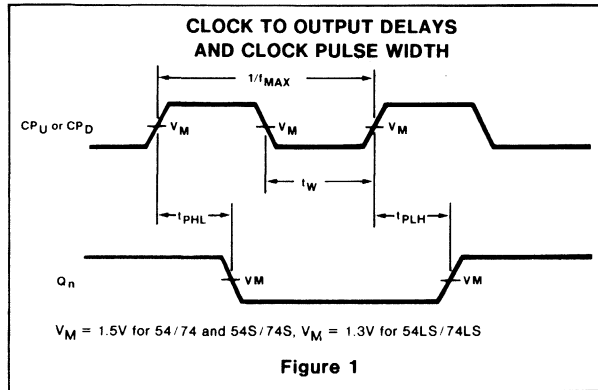
NOTE

d. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w CP_U pulse width	Figure 1	26				20		ns
t_w CP_D pulse width	Figure 1	26				20		ns
t_w \overline{PL} pulse width	Figure 3	20				20		ns
t_w MR pulse width	Figure 4	20				20		ns
t_s Setup time Data to \overline{PL}	Figure 5	20				20		ns
t_h Hold time Data to \overline{PL}	Figure 5	0				0		ns
t_{rec} Recovery time, \overline{PL} to CP	Figure 3	40				40		ns
t_{rec} Recovery time, MR to CP	Figure 4	40				40		ns

AC WAVEFORMS



54/74194
54S/74S194
54LS/74LS194A

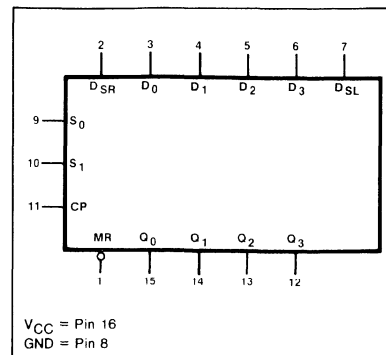
DESCRIPTION

The "194" is a 4-Bit Bidirectional Universal Shift Register useful in a wide variety of applications. As a high speed multifunctional sequential building block, it may be used in serial-serial, serial-parallel, parallel-serial, parallel-parallel, shift left, and shift right data register transfers. The device features - shift left without external connections and hold (do nothing) modes of operation.

FEATURES

- Buffered clock and control inputs
- Shift left and shift right capability
- Synchronous parallel and serial data transfers
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

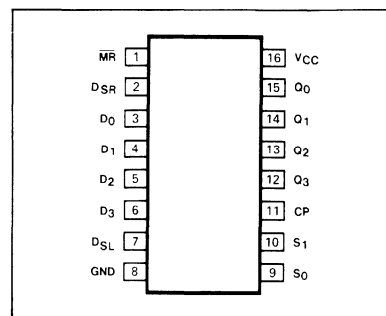
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74194N N74S194N • N74LS194AN	
Ceramic DIP	N74194F N74S194F • N74LS194AF	S54194F S54LS194AF
Flatpak		S54194W S54LS194AW

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
S ₀ , S ₁	Mode Select inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
D ₀ - D ₃	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
D _{SR}	Serial (shift right) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
D _{SL}	Serial (shift left) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
$\overline{\text{MR}}$	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
Q ₀ -Q ₃	Parallel outputs	I _{OH} (μA) I _{OL} (mA)	-800 16	-1000 20	-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The functional characteristics of the "194" 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Truth Table. The register is fully synchronous, with all operations taking place in less than 20 nanoseconds (typical) for the 54/74 and 54LS/74LS, and 12ns (typical) for 54S/74S, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The "194" design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S₀ and S₁. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, Q₀ → Q₁, etc.) or; right to left (shift left, Q₃ → Q₂, etc.) or, parallel data can be entered loading all four bits of the register simultaneously. When both S₀ and S₁ are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type serial data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode Select and Data inputs on the 54S/74S194 and 54LS/74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP).

Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. The Mode Select inputs of the 54/74194 are gated with the clock and should be changed from HIGH-to-LOW only while the Clock input is HIGH.

The four parallel data inputs (D₀ – D₃) are D-type inputs. Data appearing on D₀ – D₃ inputs when S₀ and S₁ are HIGH is transferred to the Q₀ – Q₃ outputs respectively following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset (MR) overrides all other input conditions and forces the Q outputs LOW.

MODE SELECT - FUNCTION TABLE

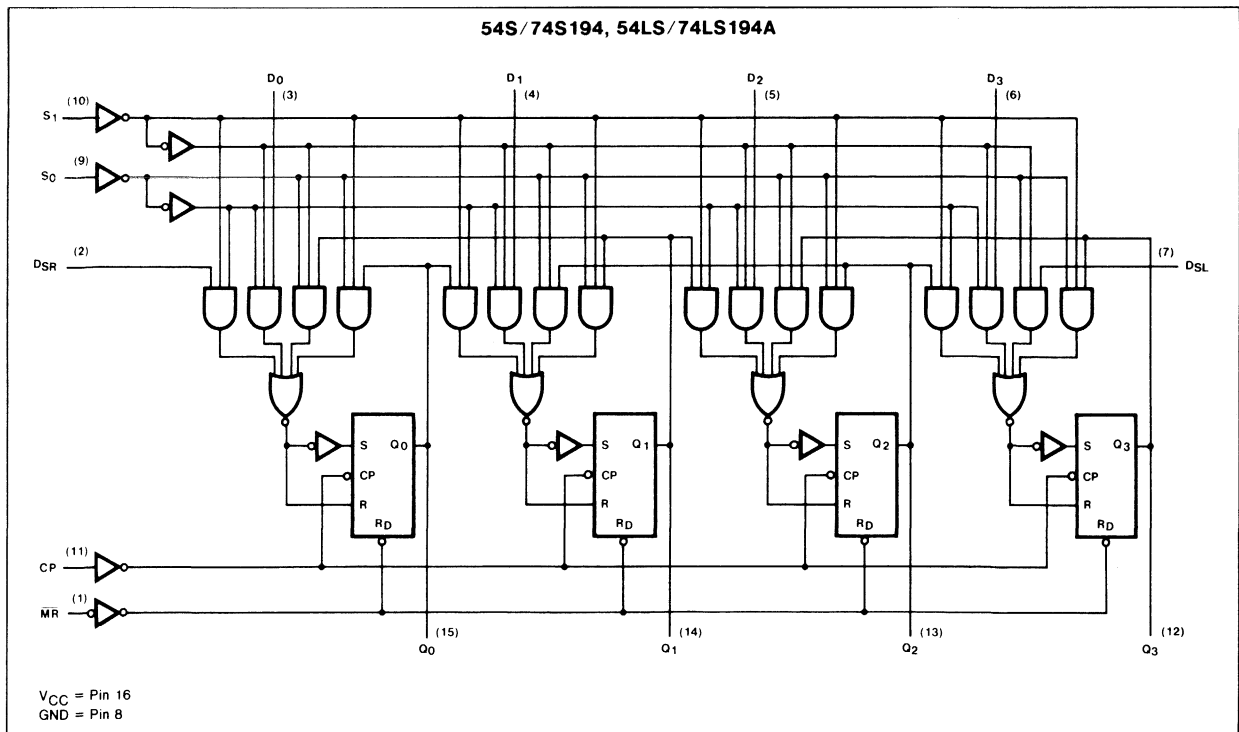
OPERATING MODE	INPUTS							OUTPUTS			
	CP	MR	S ₁	S ₀	D _{SR}	D _{SL}	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l(b)	l(b)	X	X	X	q ₀	q ₁	q ₂	q ₃
Shift Left	↑	H	h	l(b)	X	l	X	q ₁	q ₂	q ₃	L
	↑	H	h	l(b)	X	h	X	q ₁	q ₂	q ₃	H
Shift Right	↑	H	l(b)	h	l	X	X	L	q ₀	q ₁	q ₂
	↑	H	l(b)	h	h	X	X	H	q ₀	q ₁	q ₂
Parallel Load	↑	H	h	h	X	X	d _n	d ₀	d ₁	d ₂	d ₃

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

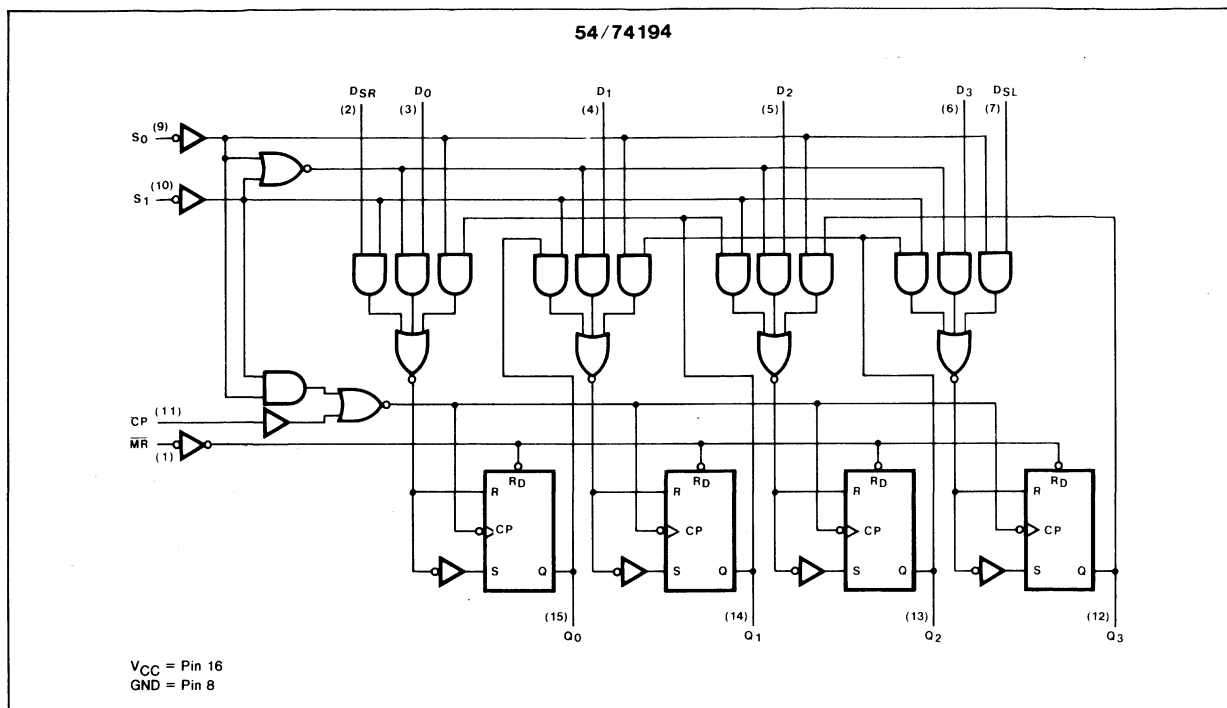
NOTES

b. The HIGH-to-LOW transition of the S₀ and S₁ inputs on the 54/74194 should only take place while CP is HIGH for conventional operation.

LOGIC DIAGRAM



LOGIC DIAGRAM (Cont'd)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$		63		135		23	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Figure 1	25		70		25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Figure 1	7.0	22	4.0	12		22	ns
		7.0	26	4.0	16.5		26	ns
t_{PHL} Propagation delay \overline{MR} to output	Figure 2		30		18.5		30	ns

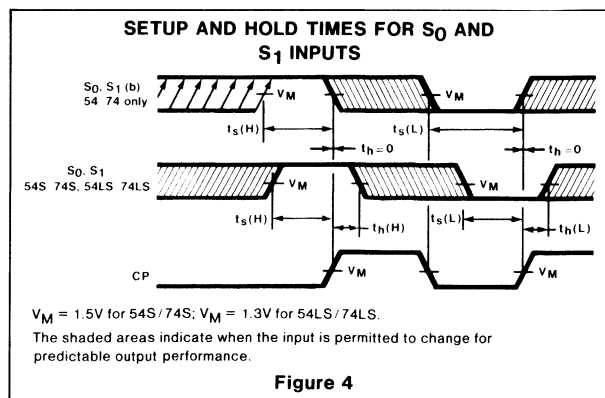
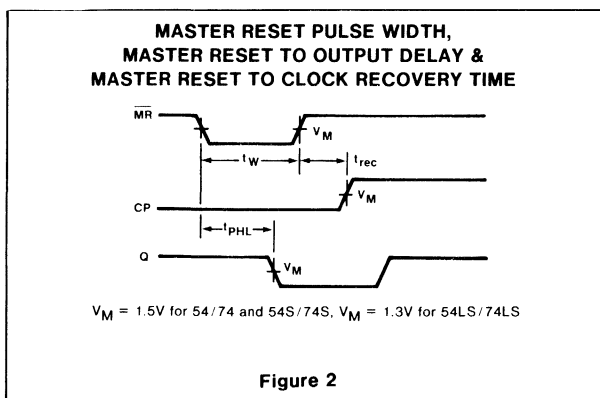
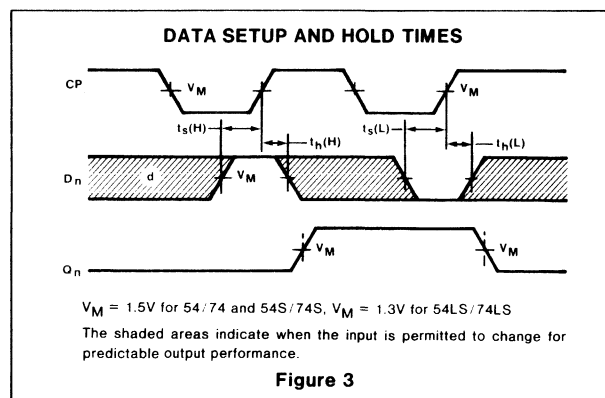
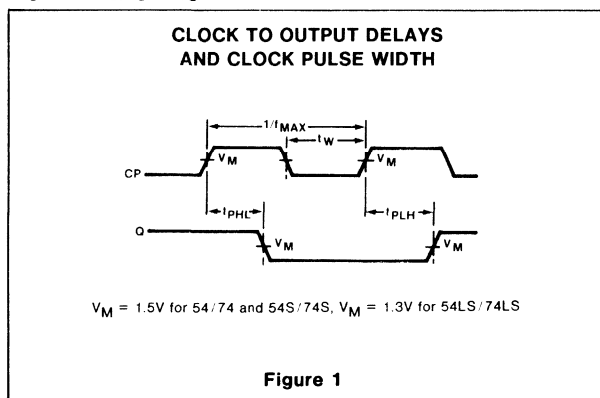
NOTE

c. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width, LOW	Figure 1	20		7.3		20		ns
$t_{W(L)}$ $\overline{\text{MR}}$ pulse width, LOW	Figure 2	20		12		20		ns
t_s Setup time Data to Clock	Figure 3	20		5.0		20		ns
t_h Hold time Data to Clock	Figure 3	0		3.0		0		ns
$t_{s(L)}$ Setup time LOW S_n to CP	Figure 4	(b)		8.0		30		ns
$t_{s(H)}$ Setup time HIGH S_n to CP	Figure 4	30		8.0		30		ns
t_h Hold time S_n to CP	Figure 4	0		3.0		0		ns
t_{rec} Recovery time $\overline{\text{MR}}$ to CP	Figure 2	25		9.0		25		ns

AC WAVEFORMS



54/74195
54S/74S195
54LS/74LS195A

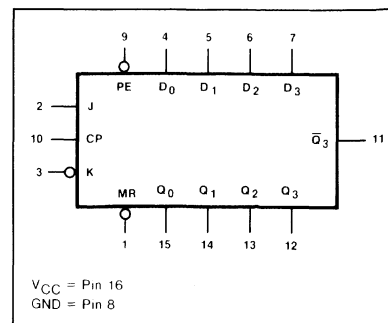
DESCRIPTION

The "195" is a high speed 4-Bit Parallel Access Shift Register useful for a wide variety of register and counting applications. It features fully synchronous parallel and serial data transfers. The Master Reset is asynchronous, and clears the register when LOW.

FEATURES

- Buffered clock and control inputs
- Shift right and parallel load capability
- Fully synchronous data transfers
- J-K̄ (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset

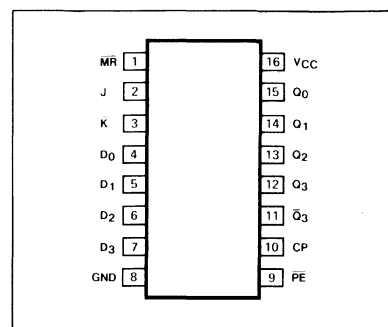
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74195N	
	N74S195N • N74LS195AN	
Ceramic DIP	N74195F	S54195F
	N74S195F • N74LS195AF	S54LS195AF
Flatpak		S54195W
		S54LS195AW

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
D ₀ -D ₃	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
J	First stage J (active HIGH) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
K̄	First stage K (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
PĒ	Parallel Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
MR̄	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6	50 -2.0	20 -0.4
Q ₀ -Q ₃	Parallel outputs	I _{OH} (μA) I _{OL} (mA)	-800 16	-1000 20	-400 4/8(a)
Q ₃ ̄	Complementary last stage output	I _{OH} (μA) I _{OL} (mA)	-800 16	-1000 20	-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military / Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The functional characteristics of the "195" 4-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The "195" operates on two primary modes: shift right ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) and parallel load, which are controlled by the state of the Parallel Enable (\overline{PE}) input. Serial data enters the first flip-flop (Q_0) via the J and \overline{K} inputs when the \overline{PE} input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and \overline{K} inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the \overline{PE} input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0 - D_3) is transferred to the respective Q_0 - Q_3 outputs. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the \overline{PE} input LOW.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The "195" utilizes edge-

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	\overline{MR}	CP	\overline{PE}	J	\overline{K}	D_n	Q_0	Q_1	Q_2	Q_3	\overline{Q}_3
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	\uparrow	h	h	h	X	H	q_0	q_1	q_2	\overline{q}_2
Shift, Reset First Stage	H	\uparrow	h	l	l	X	L	q_0	q_1	q_2	\overline{q}_2
Shift, Toggle First Stage	H	\uparrow	h	h	l	X	\overline{q}_0	q_0	q_1	q_2	\overline{q}_2
Shift, Retain First Stage	H	\uparrow	h	l	h	X	q_0	q_0	q_1	q_2	\overline{q}_2
Parallel Load	H	\uparrow	l	X	X	d_n	d_0	d_1	d_2	d_3	\overline{d}_3

H = HIGH Voltage Level.
 L = LOW Voltage Level.
 X = Don't care.
 l = LOW Voltage level one setup time prior to the LOW-to-HIGH clock transition.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 \uparrow = LOW-to-HIGH clock transition.

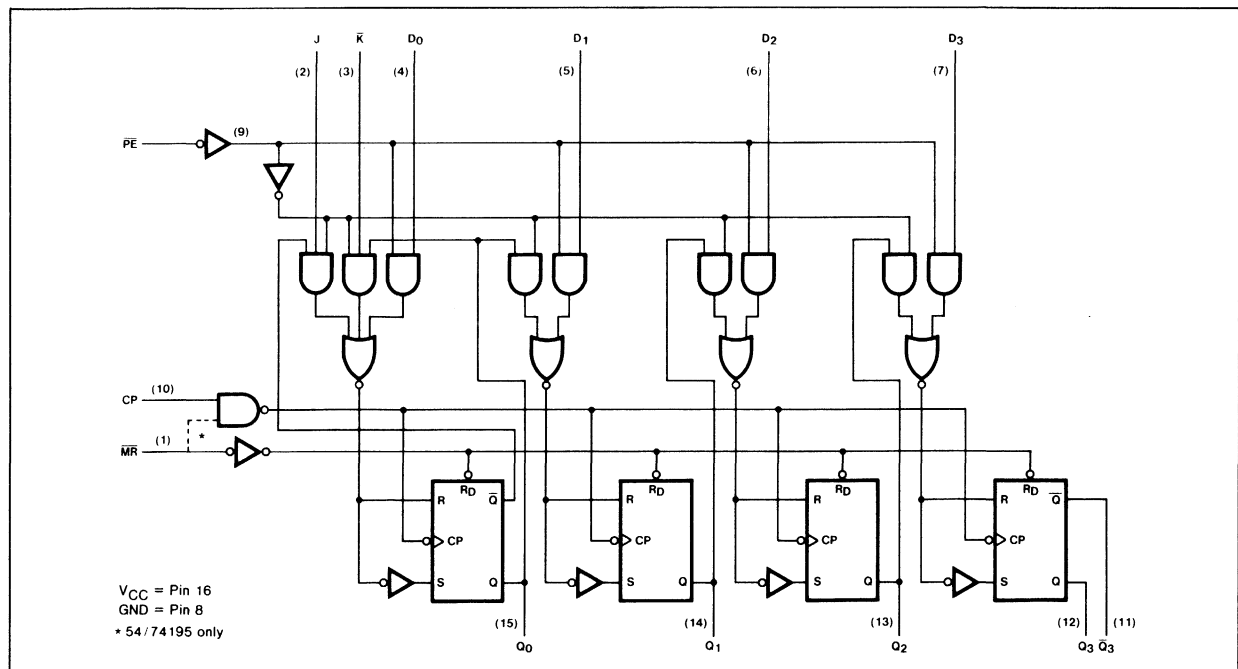
triggering, therefore, there is no restriction on the activity of the J, \overline{K} , D_n , and \overline{PE} inputs for logic operation, other than the setup and release time requirements.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition.

The \overline{MR} on the 54/74195 is gated with the Clock. Therefore, the LOW-to-HIGH \overline{MR} transition should only occur while the Clock is LOW to avoid false clocking of the 54/74195.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current	V _{CC} = Max	Mil		63		99		21	mA
			Com		63		109		21	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

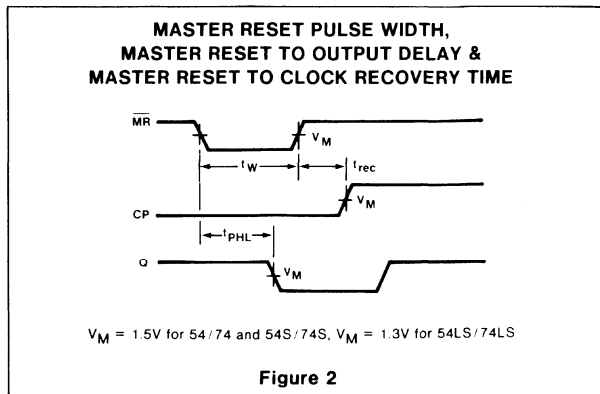
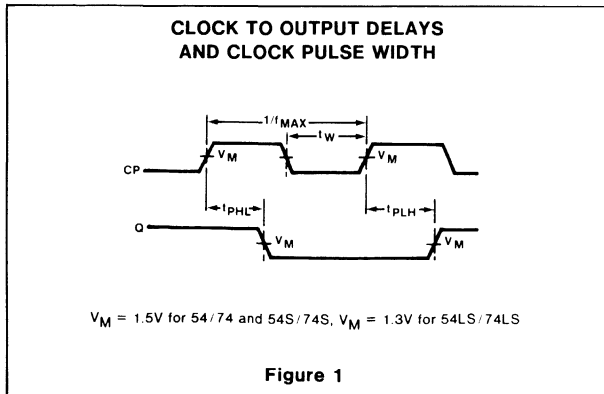
PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 400Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2kΩ		
				Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Figure 1		30		70		30		MHz
t _{PLH}	Propagation delay	Figure 1			22		12		22	ns
t _{PHL}	Clock to output				26		16.5		26	ns
t _{PHL}	Propagation delay \overline{MR} to output	Figure 2			30		18.5		30	ns

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

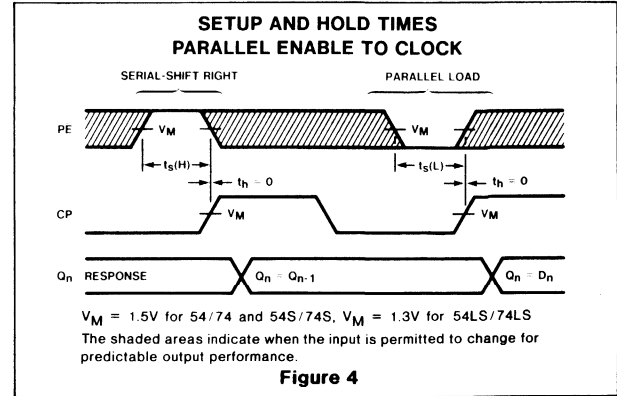
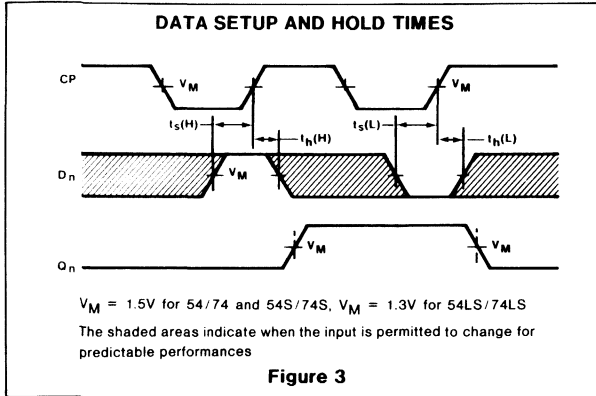
PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
t _{W(L)}	Clock pulse width (LOW)	Figure 1		18		8.0		18		ns
t _W	Master Reset pulse width	Figure 2		12		12		12		ns
t _s	Setup time J, \overline{K} and Data to Clock	Figure 3		20		5.0		15		ns
t _h	Hold time J, \overline{K} and Data to Clock	Figure 3		0		3.0		0		ns
t _s	Setup time \overline{PE} to Clock	Figure 4		25		11		25		ns
t _h	Hold time \overline{PE} to Clock	Figure 4		0		0		0		ns
t _{rec}	Recovery time \overline{MR} to Clock	Figure 2		25		9.0		25		ns

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



54/74196 - See 8290
54S/74S196 - See 82S90
54LS/74LS196

DESCRIPTION

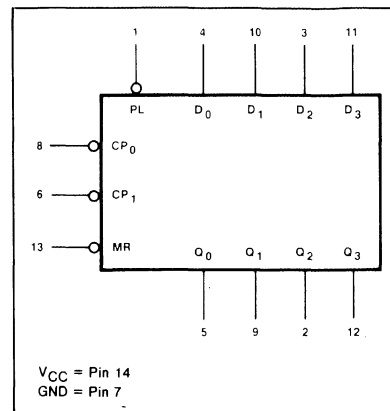
The "196" is an asynchronously presettable Decade Ripple Counter. It is partitioned into divide-by-2 and divide-by-5 sections which can be combined to count in either BCD (8421) mode or bi-quinary mode producing a 50% duty cycle output.

The circuit has a Master Reset (\overline{MR}) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (\overline{PL}) asynchronously loads the data on the parallel Data inputs (D_n) into the flip-flops and overrides clocked operations. The circuit is useable as a programmable counter with this preset feature. The "196" may also be used as a 4-bit latch, loading data from the parallel Data inputs when \overline{PL} is LOW and storing the data when \overline{PL} is HIGH.

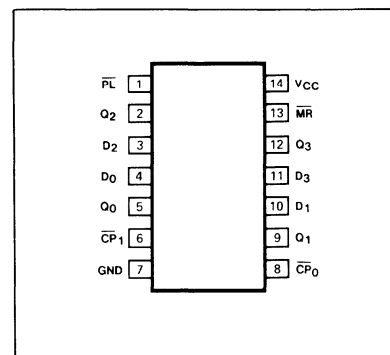
FEATURES

- Performs BCD or Bi-quinary counting
- Asynchronous parallel load for presetting counter
- Overriding Master Reset
- Buffered Q_0 output drives \overline{CP}_1 input plus standard fan-out
- See 82S90 for faster version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS196N	
Ceramic DIP	N74LS196F	S54LS196F
Flatpak		S54LS196W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}_0	Clock (active LOW going edge) input to $\div 2$ section	I_{IH} (μA) I_{IL} (mA)			40 -2.4
\overline{CP}_1	Clock (active LOW going edge) input to $\div 5$ section	I_{IH} (μA) I_{IL} (mA)			80 -2.8
D_0 - D_3	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{PL}	Parallel Load (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{MR}	Master Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)			40 -0.8
Q_0 - Q_3	Counter outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "196" is an asynchronously presettable decade ripple counter partitioned into divide-by-2 and divide-by-5 sections with each section having a separate Clock input. State changes are initiated in the counting modes by the HIGH-to-LOW transition of the Clock inputs, however, state changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to spikes, and thus a decoded signal should not be used as a strobe or clock. The Q₀ flip-flop is triggered by the CP₀ input, while the CP₁ input triggers the divide-by-5 section. The Q₀ output is designed and specified to drive the rated fan-out plus the CP₁ input.

As indicated in the Count Sequence Tables the "196" can be connected to operate in two different count sequences. The circuit counts in the BCD (8,4,2,1) sequence with the input connected to CP₀ and with Q₀ driving CP₁. Q₀ becomes the low frequency output and has a 50% duty cycle waveform with the input connected to CP₁ and Q₃ driving CP₀. The maximum counting rate is reduced in the bi-quinary configuration because of the interstage gating delay within the divide-by-5 section.

The device has an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counter is also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data (D₀-D₃) inputs into the flip-flops. The counter acts as a transparent latch while the PL is LOW and any change in the D_n inputs will be reflected in the outputs.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	MR	PL	CP	D _n	Q _n
Reset (Clear)	L	X	X	X	L
Parallel Load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↓ = HIGH-to-LOW Clock Transition

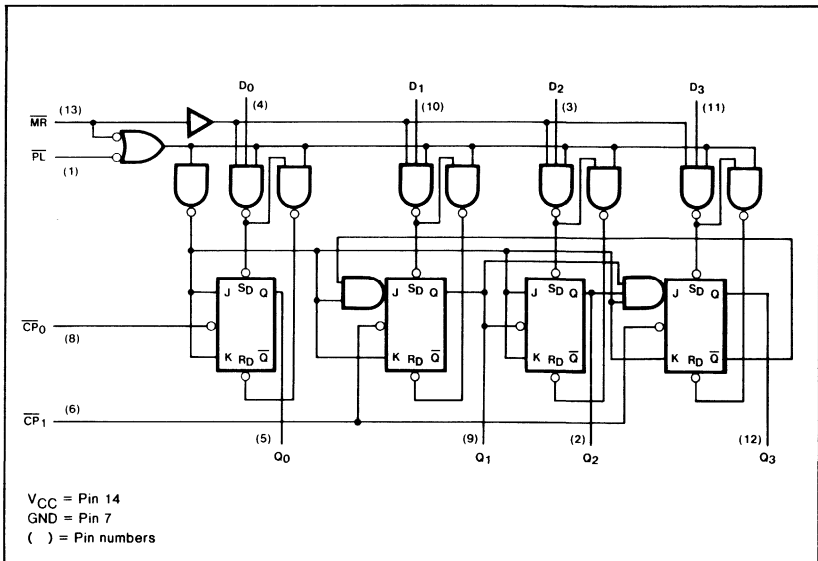
COUNT SEQUENCES

BCD DECADE (b)					BI-QUINARY (c)				
COUNT	Q ₃	Q ₂	Q ₁	Q ₀	COUNT	Q ₀	Q ₃	Q ₂	Q ₁
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES

- b. Input applied to CP₀; Q₀ connected to CP₁.
- c. Input applied to CP₁; Q₃ connected to CP₀.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(d)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						27	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum count frequency	Figure 1					30		MHz
						15		MHz
t _{PLH} Propagation delay t _{PHL} \overline{CP}_0 to Q ₀	Figure 1						15 20	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CP}_1 to Q ₁	Figure 1						24 33	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CP}_1 to Q ₂	Figure 1						52 52	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CP}_1 to Q ₃	Figure 1						18 35	ns ns
t _{PLH} Propagation delay t _{PHL} Data to output	Figure 2						25 28	ns ns
t _{PLH} Propagation delay t _{PHL} PL to output	Figure 3						30 45	ns ns
t _{PHL} Propagation delay \overline{MR} to output	Figure 4						30	ns

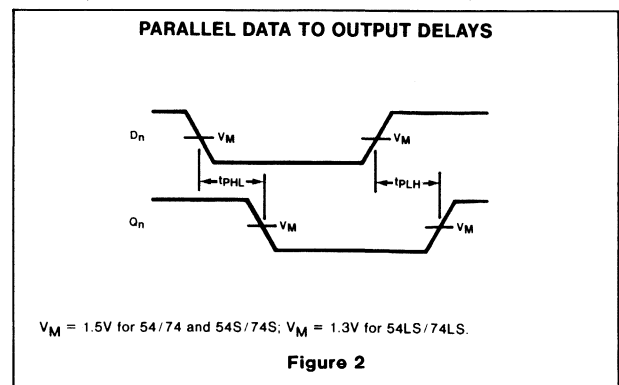
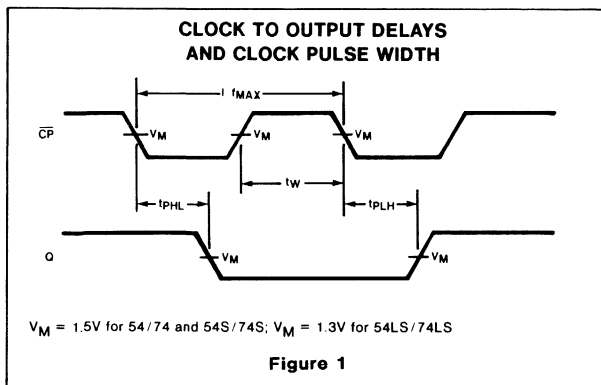
NOTE

d. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

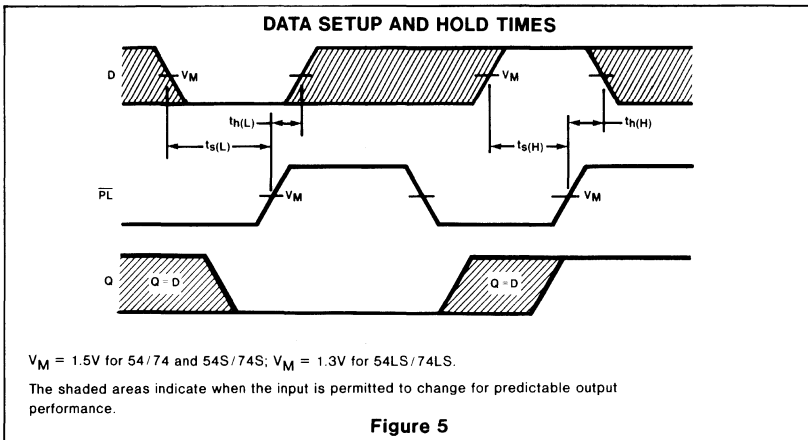
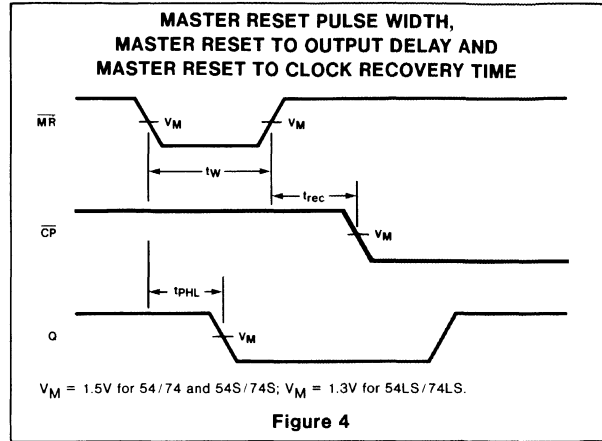
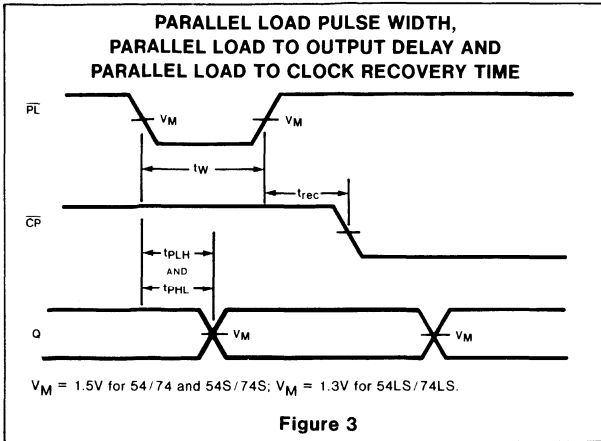
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W Clock pulse width	Figure 1	\overline{CP}_0				20		ns
		\overline{CP}_1				30		ns
t_W \overline{MR} pulse width	Figure 4					15		ns
t_W \overline{PL} pulse width	Figure 3					20		ns
$t_s(H)$ Setup time HIGH Data to \overline{PL}	Figure 5					10		ns
$t_h(H)$ Hold time HIGH Data to \overline{PL}	Figure 5					4.0		ns
$t_s(L)$ Setup time LOW Data to \overline{PL}	Figure 5					15		ns
$t_h(L)$ Hold time LOW Data to \overline{PL}	Figure 5					10		ns
t_{rec} Recovery time \overline{MR} to \overline{CP}	Figure 4					30		ns
t_{rec} Recovery time \overline{PL} to \overline{CP}	Figure 3					30		ns

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



54/74197-See 8291
54S/74S197-See 82S91
54LS/74LS197

DESCRIPTION

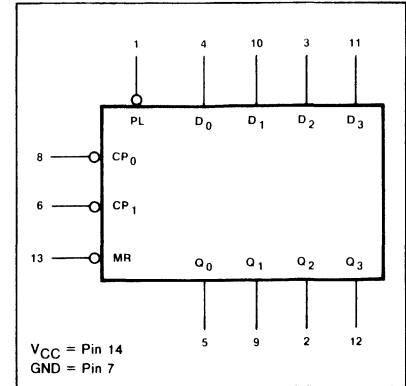
The "197" is a 4-Stage Presettable Ripple Counter containing divide-by-2 and divide-by-8 sections which can be combined to form a modulo-16 binary counter.

The circuit has a Master Reset (\overline{MR}) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (\overline{PL}) asynchronously loads the data on the parallel Data inputs (D_n) into the flip-flops and overrides clocked operations. The circuit is useable as a programmable counter with this preset feature. The "197" may also be used as a 4-bit latch, loading data from the parallel Data inputs when \overline{PL} is LOW and storing the data when \overline{PL} is HIGH.

FEATURES

- High speed 4-bit binary counting
- Asynchronous parallel load for presetting counter
- Overriding Master Reset
- Buffered Q_0 output drives \overline{CP}_1 input plus standard fan-out
- See 82S91 for faster version

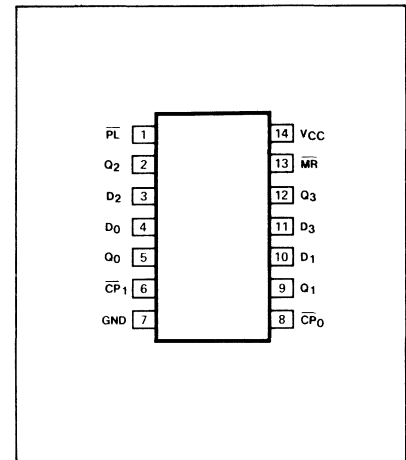
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS197N	
Ceramic DIP	N74LS197F	S54LS197F
Flatpak		S54LS197W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}_0	Clock (active LOW going edge) input to $\div 2$ section	I_{IH} (μA) I_{IL} (mA)			40 -2.4
\overline{CP}_1	Clock (active LOW going edge) input to $\div 8$ section	I_{IH} (μA) I_{IL} (mA)			40 -1.3
D_0 - D_3	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{PL}	Parallel Load (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{MR}	Master Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)			40 -0.8
Q_0 - Q_3	Counter outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "197" is an asynchronously presettable binary ripple counter partitioned into divide-by-2 and divide-by-8 sections with each section having a separate clock input. State changes are initiated in the counting modes by the HIGH-to-LOW transition of the clock inputs, however, stage changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock. The Q₀ flip-flop is triggered by the \overline{CP}_0 input while the \overline{CP}_1 input triggers the divide-by-8 section. The Q₀ output is designed and specified to drive the rated fan-out plus the \overline{CP}_1 input.

The device has an asynchronous active LOW Master Reset input (\overline{MR}) which overrides all other inputs and forces all outputs LOW. The counter is also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from parallel Data (D₀-D₃) inputs into the flip-flops. The counter acts as a transparent latch while the \overline{PL} is LOW and any change in the D_n inputs will be reflected in the outputs.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	\overline{MR}	\overline{PL}	\overline{CP}	D _n	Q _n
Reset (Clear)	L	X	X	X	L
Parallel Load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
L = LOW voltage level

X = Don't care
↓ = HIGH-to-LOW Clock Transition

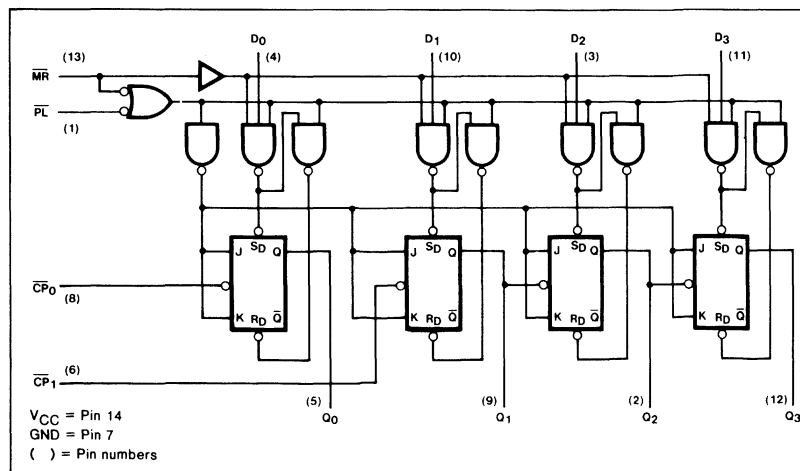
COUNT SEQUENCE

COUNT	4-BIT BINARY(b)			
	Q ₃	Q ₂	Q ₁	Q ₀
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE

b. Q₀ connected to \overline{CP}_1 ; input applied to \overline{CP}_0

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(c)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						27	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						C _L = 15pF R _L = 2KΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum count frequency	Figure 1					30		MHz
						15		MHz
t _{PLH} Propagation delay t _{PHL} \overline{CP}_0 to Q ₀	Figure 1						15 21	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CP}_1 to Q ₁	Figure 1						19 30	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CP}_1 to Q ₂	Figure 1						51 51	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CP}_1 to Q ₃	Figure 1						78 81	ns ns
t _{PLH} Propagation delay t _{PHL} Data to output	Figure 2						25 28	ns ns
t _{PLH} Propagation delay t _{PHL} \overline{PL} to output	Figure 3						30 45	ns ns
t _{PHL} Propagation delay \overline{MR} to output	Figure 4						30	ns

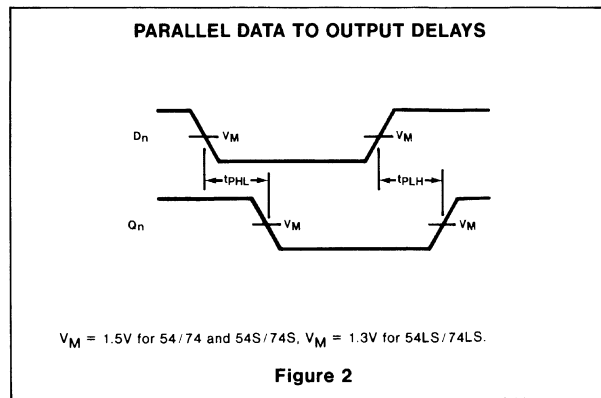
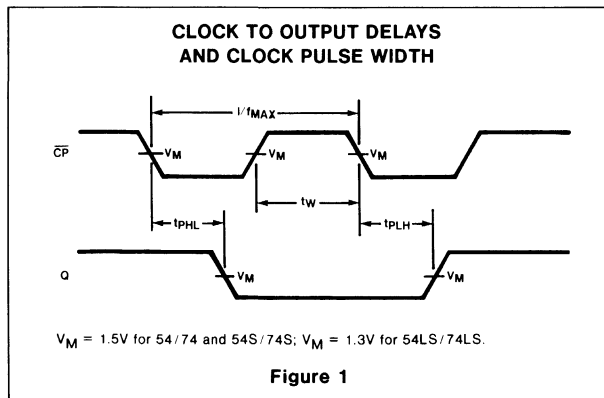
NOTE

c. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S specifications.

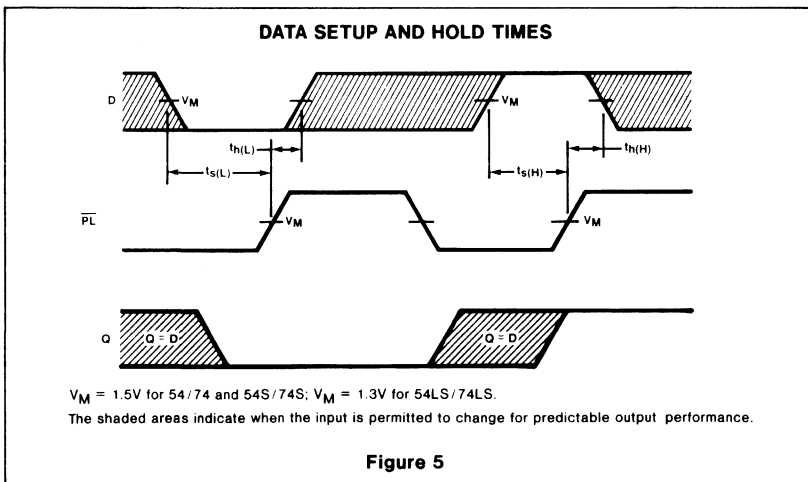
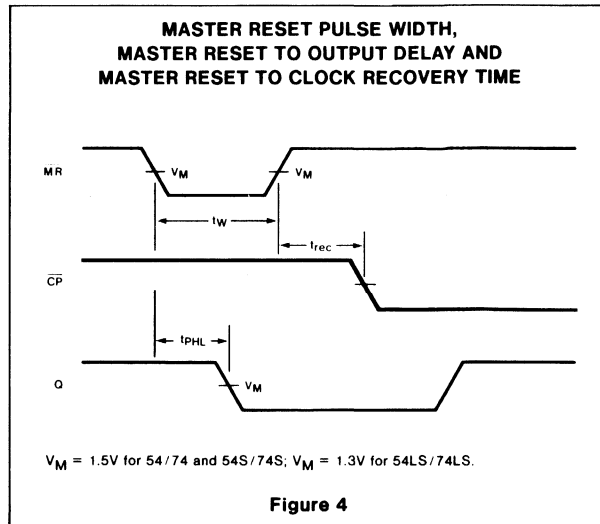
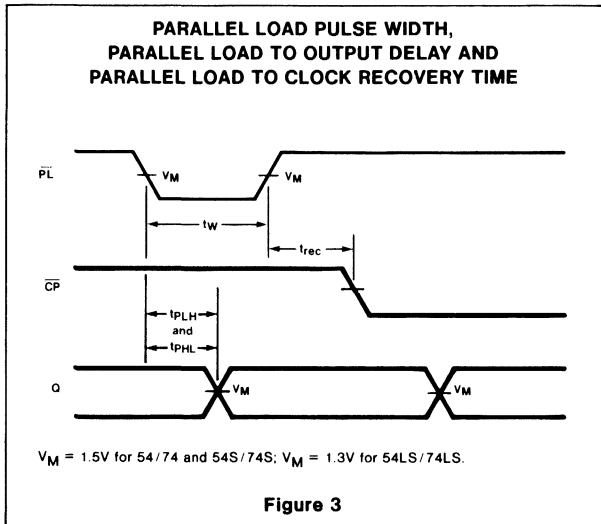
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w Clock pulse width	Figure 1	\overline{CP}_0				20		ns
		\overline{CP}_1				30		ns
t_w \overline{MR} pulse width	Figure 4					15		ns
t_w \overline{PL} pulse width	Figure 3					20		ns
$t_s(H)$ Setup time HIGH Data to \overline{PL}	Figure 5					10		ns
$t_h(H)$ Hold time HIGH Data to \overline{PL}	Figure 5					4.0		ns
$t_s(L)$ Setup time LOW Data to \overline{PL}	Figure 5					15		ns
$t_h(L)$ Hold time LOW Data to \overline{PL}	Figure 5					10		ns
t_{rec} Recovery time \overline{MR} to \overline{CP}	Figure 4					30		ns
t_{rec} Recovery time \overline{PL} to \overline{CP}	Figure 3					30		ns

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



54/74198

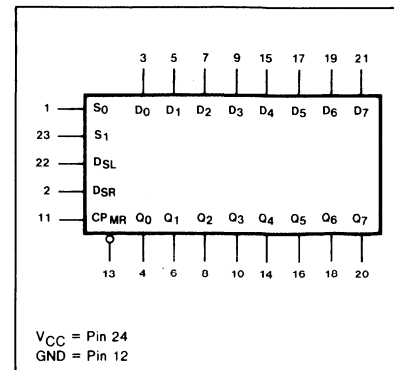
DESCRIPTION

The "198" is a 8-Bit Bidirectional Universal Shift Register useful in a wide variety of applications. As a high speed multifunctional sequential building block, it may be used in serial-serial, serial-parallel, parallel-serial, parallel-parallel, shift left, and shift right data register transfers. The device features shift left without external connections and hold (do nothing) modes of operation.

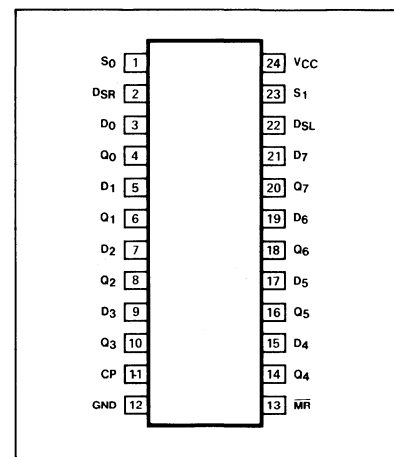
FEATURES

- Buffered clock and control inputs
- Shift left and shift right capability
- Synchronous parallel and serial data transfers
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74198N	
Ceramic DIP	N74198F	S54198F
Flatpak		S54198W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
S ₀ , S ₁	Mode Select inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
D ₀ -D ₇	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
DSR	Serial (shift right) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
DSL	Serial (shift left) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
MR	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
Q ₀ -Q ₇	Parallel outputs	I _{OH} (μA) I _{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The functional characteristics of the "198" 8-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Truth Table. The register is fully synchronous with all operations taking place in less than 20 nanoseconds (typical) making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The "198" design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S₀ and S₁. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, Q₀→Q₁→etc.) or: right to left (shift left, Q₇→Q₆→etc.) or, parallel data can be entered loading all eight bits of the register simultaneously. When both S₀ and S₁ are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type serial data inputs D_{SR}, D_{SL} to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

The Mode Select inputs of the 54/74198 are gated with the clock and should be changed from HIGH-to-LOW only while the Clock input is HIGH for predictable operation. The eight parallel data inputs (D₀-D₇) are D-type inputs. Data appearing on D₀-D₇ inputs when S₀ and S₁ are HIGH is transferred to the Q₀-Q₇ outputs respectively following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset (MR) overrides all other input conditions and forces the Q outputs LOW.

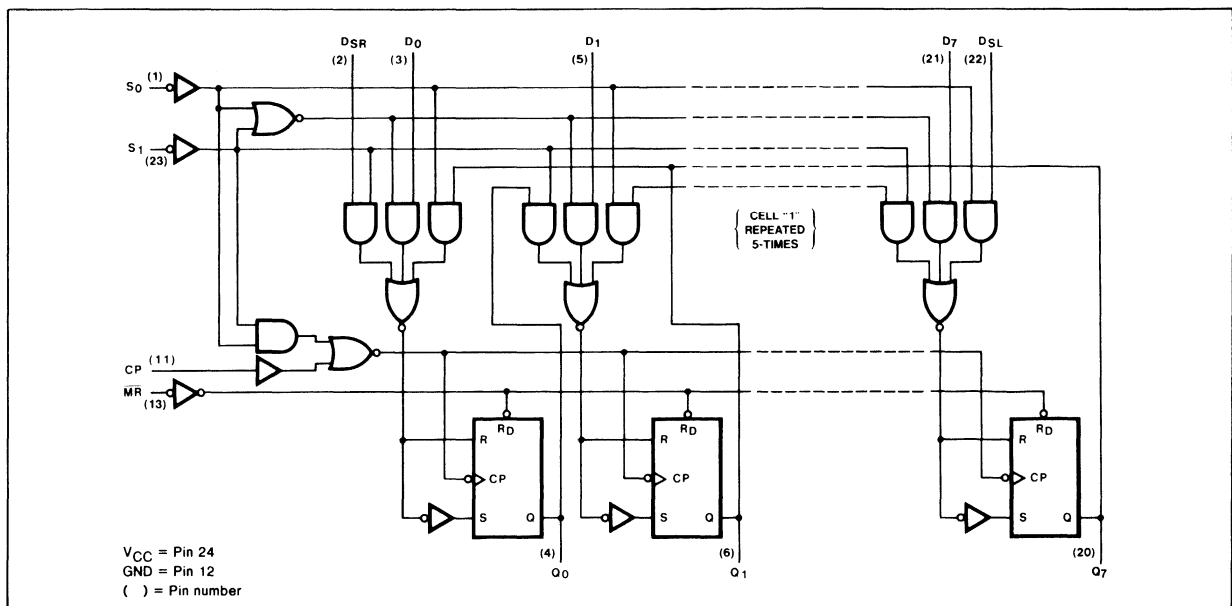
MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS	
	CP	\overline{MR}	S ₁	S ₀	D _{SR}	D _{SL}	D _n	Q ₀ Q ₁ ... Q ₆	Q ₇
Reset (clear)	X	L	X	X	X	X	X	L L ... L	L
Hold (do nothing)	↑	H	i(b)	i(b)	X	X	X	q ₀ q ₁ ... q ₆	q ₇
Shift Left	↑	H	h	i(b)	X	l	X	q ₁ q ₂ ... q ₇	L
	↑	H	h	i(b)	X	h	X	q ₁ q ₂ ... q ₇	H
Shift Right	↑	H	i(b)	h	l	X	X	L q ₀ ... q ₅	q ₆
	↑	H	i(b)	h	h	X	X	H q ₀ ... q ₅	q ₆
Parallel Load	↑	H	h	h	h	X	d _n	d ₀ d ₁ ... d ₆	d ₇

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

NOTE
 b. The HIGH-to-LOW transition of the S₀ and S₁ inputs on the 54/74198 should only take place while CP is HIGH for conventional operation.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(c)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current	V _{CC} = Max	Mil	104						mA
			Com	116						mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 400Ω						
				Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Figure 1		25						MHz
t _{PLH}	Propagation delay	Figure 1			26					ns
t _{PHL}	Clock to output				30					ns
t _{PHL}	Propagation delay MR to output	Figure 2			35					ns

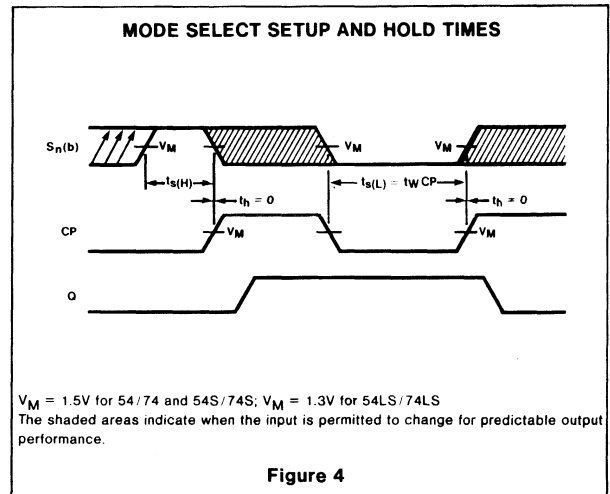
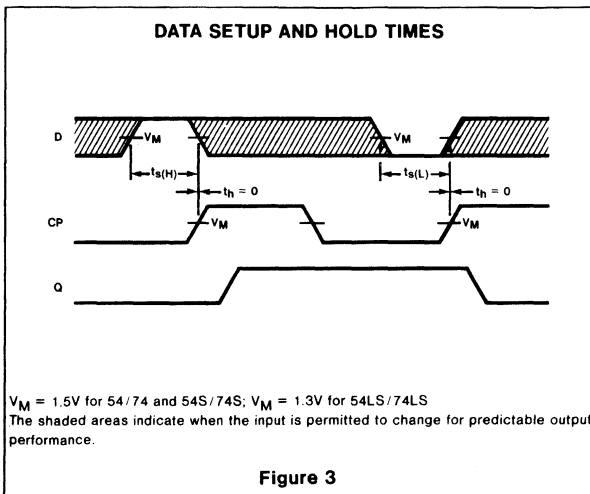
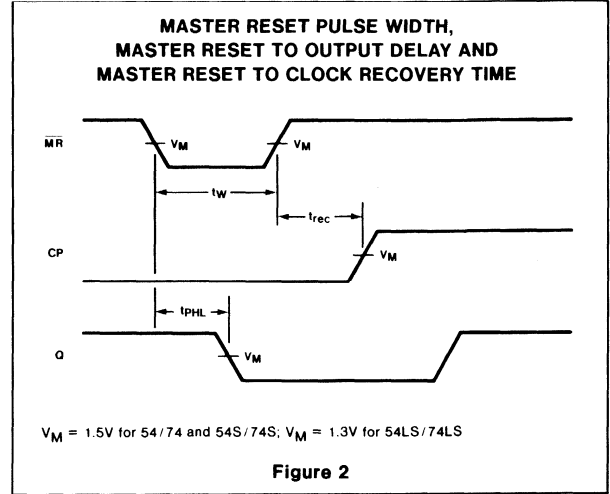
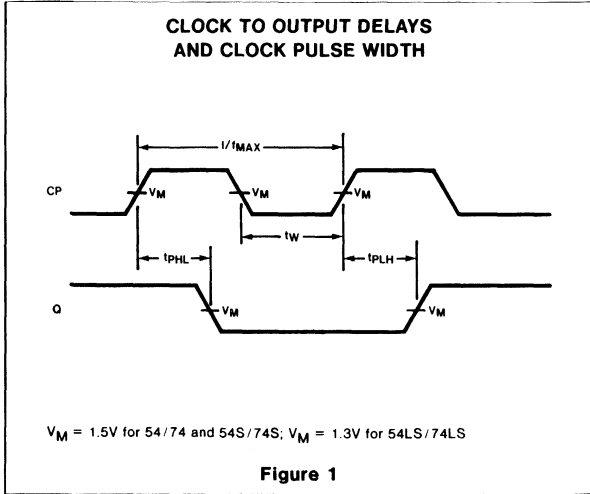
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
t _{W(L)}	Clock pulse width, LOW	Figure 1		20						ns
t _{W(L)}	\overline{MR} pulse width, LOW	Figure 2		20						ns
t _s	Setup time Data to Clock	Figure 3		20						ns
t _h	Hold time Data to Clock	Figure 3		0						ns
t _{s(L)}	Setup time LOW S _n to CP	Figure 4		(b)						ns
t _{s(H)}	Setup time HIGH S _n to CP	Figure 4		30						ns
t _h	Hold time S _n to CP	Figure 4		0						ns
t _{rec}	Recovery time \overline{MR} to CP	Figure 2		30						ns

NOTE

c. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54/74199

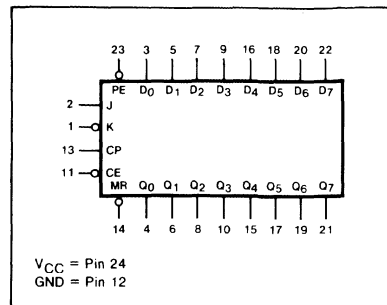
DESCRIPTION

The "199" is a high speed 8-Bit Parallel Access Shift Register useful for a wide variety of register and counting applications. It features fully synchronous parallel and serial data transfers. A gated clock is provided allowing one input to be used as a Clock Enable. The Master Reset is asynchronous, and clears the register when LOW.

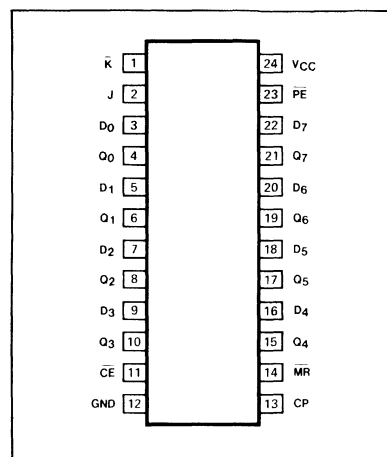
FEATURES

- Buffered clock and control inputs
- Shift right and parallel load capability
- Fully synchronous data transfers
- J-K (D) inputs to first stage
- Clock enable for hold (do nothing) mode
- Asynchronous Master Reset

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74199N	
Ceramic DIP	N74199F	S54199F
Flatpak		S54199W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
D ₀ -D ₇	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
J	First stage J (active HIGH) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
\bar{K}	First stage K (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
\bar{PE}	Parallel Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
\bar{MR}	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
\bar{CE}	Clock Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		
Q ₀ -Q ₇	Parallel outputs	I _{OH} (μA) I _{OL} (mA)	-800 16		

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The functional characteristics of the "199" 8-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The "199" operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable (\overline{PE}) input. Serial data enters the first flip-flop (Q_0) via the J and \overline{K} inputs when the \overline{PE} input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and \overline{K} inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as eight common clocked D flip-flops when the \overline{PE} input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0 - D_7) is transferred to the respective Q_0 - Q_7 outputs.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The "199" utilizes edge-triggering, therefore, there is no restriction on the activity of the J, \overline{K} , D_n , and \overline{PE} inputs for logic operation, other than the setup and release time requirements.

The clock input is a gated OR structure which allows one input to be used as an

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS							OUTPUTS		
	\overline{MR}	CP	\overline{CE}	\overline{PE}	J	\overline{K}	D_n	Q_0	$Q_1 \dots Q_6$	Q_7
Reset (clear)	L	X	X	X	X	X	X	L	L ... L	L
Shift, Set First Stage	H	\uparrow	l	h	h	h	X	H	$q_0 \dots q_5$	q_6
Shift, Reset First Stage	H	\uparrow	l	h	l	l	X	L	$q_0 \dots q_5$	q_6
Shift, Toggle First Stage	H	\uparrow	l	h	h	l	X	$\overline{q_0}$	$q_0 \dots q_5$	q_6
Shift, Retain First Stage	H	\uparrow	l	h	l	h	X	q_0	$q_0 \dots q_5$	q_6
Parallel Load	H	\uparrow	l	l	X	X	d_n	d_0	$d_1 \dots d_6$	d_7
Hold (do nothing)	H	\uparrow	h(b)	X	X	X	X	q_0	$q_1 \dots q_6$	q_7

H = HIGH voltage level steady state
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level steady state
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 X = Don't Care
 d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition
 \uparrow = LOW-to-HIGH clock transition

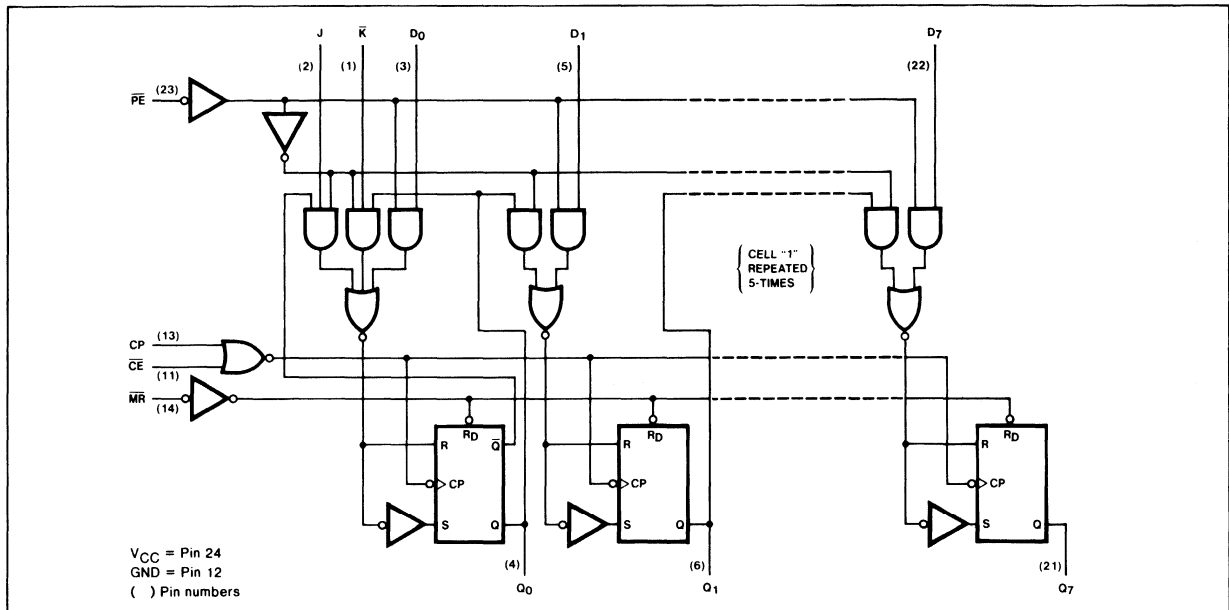
NOTE

b. The LOW-to-HIGH transition of \overline{CE} should only occur while CP is HIGH for conventional operation.

active LOW Clock Enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of \overline{CE} input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE ^(c)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current	V _{CC} = Max	Mil	104						mA
			Com	116						mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 400Ω						
				Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Figure 1		25						MHz
t _{PLH}	Propagation delay	Figure 1			26					ns
t _{PHL}	Clock to output				30					ns
t _{PHL}	Propagation delay \overline{MR} to output	Figure 2			35					ns

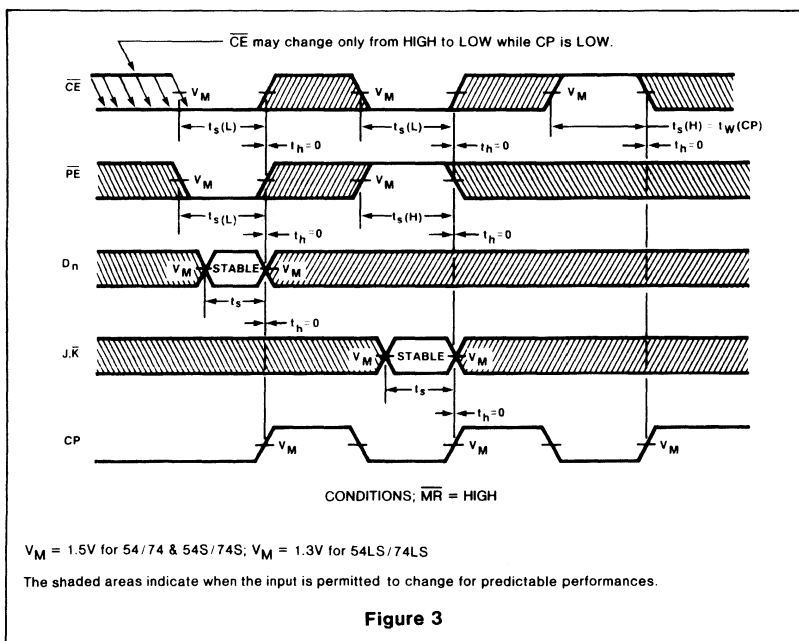
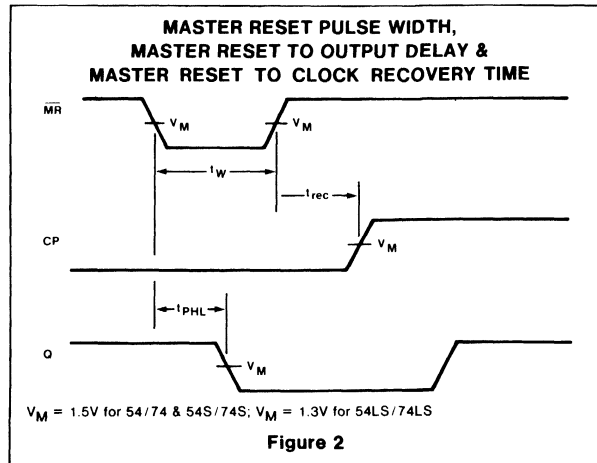
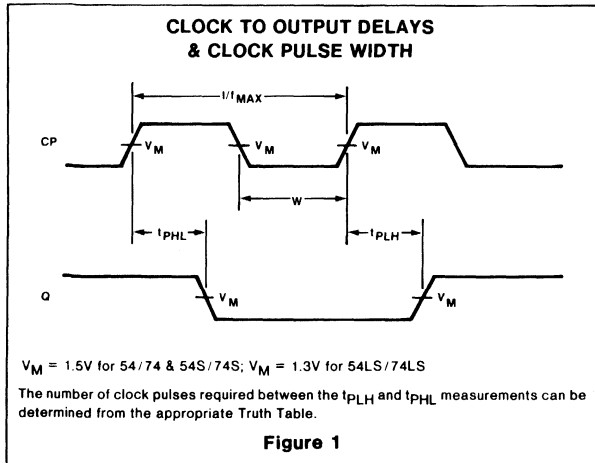
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
t _w	Clock pulse width	Figure 1		20						ns
t _w	\overline{MR} pulse width	Figure 2		20						ns
t _s	Setup time J, \overline{K} and Data to clock	Figure 3		20						ns
t _h	Hold time J, \overline{K} and Data to clock	Figure 3		0						ns
t _s	Setup time \overline{CE} to clock	Figure 3		30						ns
t _h	Hold time \overline{CE} to clock	Figure 3		0						ns
t _s	Setup time \overline{PE} to clock	Figure 3		30						ns
t _h	Hold time \overline{PE} to clock	Figure 3		0						ns
t _{rec}	Recovery time \overline{MR} to clock	Figure 2		30						ns

NOTE

c. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54/74221
54LS/74LS221

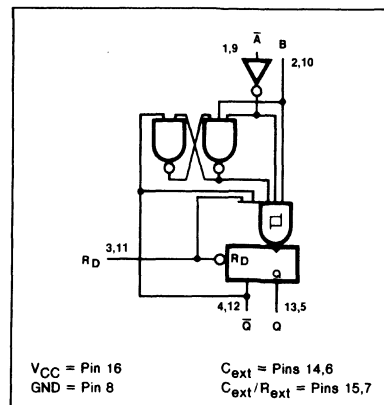
DESCRIPTION

The "221" is a Dual Monostable Multivibrator with Schmitt-trigger inputs (B) and an overriding direct Reset (\bar{R}_D). The output pulse width is independent of the input pulse width and can be varied from 35 nanoseconds to over one minute for the 74LS221. The output pulse width is determined by the value of the external resistance and capacitance connected to the C_{ext} and R_{ext}/C_{ext} terminals.

FEATURES

- Pulse-Width Variance is typically less than $\pm 0.5\%$ for 98% of the units
- The "221" demonstrates electrical and switching characteristics that are virtually identical to the "121" one-shots
- Pin-Out is identical to the "123"
- Overriding Reset terminates output pulse
- B input has hysteresis for improved noise immunity
- Maximum pulse width:
54221 21 seconds
74221 28 seconds
54LS221 49 seconds
74LS221 70 seconds

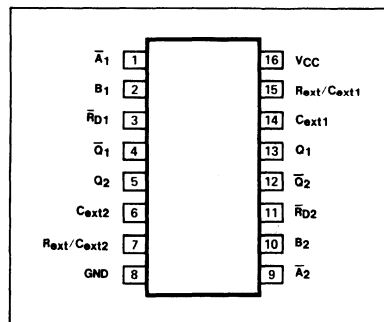
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	N74221N	•	N74LS221N	
Ceramic DIP	N74221F	•	N74LS221F	S54221F • S54LS221F
Flatpak				S54221W • S54LS221W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\bar{A}	Trigger (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6		20 -0.4
B	Trigger (active HIGH) input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		20 -0.8
\bar{R}_D	Direct Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)	80 -3.2		20 -0.8
Q	Pulse (active HIGH) output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)
\bar{Q}	Pulse (active LOW) output	I_{OH} (μA) I_{OL} (mA)	-800 16		-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "221" is a dual monostable multivibrator with performance characteristics virtually identical to those of the "121". Each multivibrator features an active LOW going edge input (\bar{A}) and an active HIGH going edge input (B) either of which can be used as an enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the \bar{A} and B inputs and

are a function of the timing components. The output pulses can be terminated by the overriding active LOW Reset (\bar{R}_D). Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the FEATURES by choosing appropriate timing components. With $R_{ext} = 2k\Omega$ and $C_{ext} = 0$, an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter free operation is maintained over the full temperature and V_{CC} ranges for more

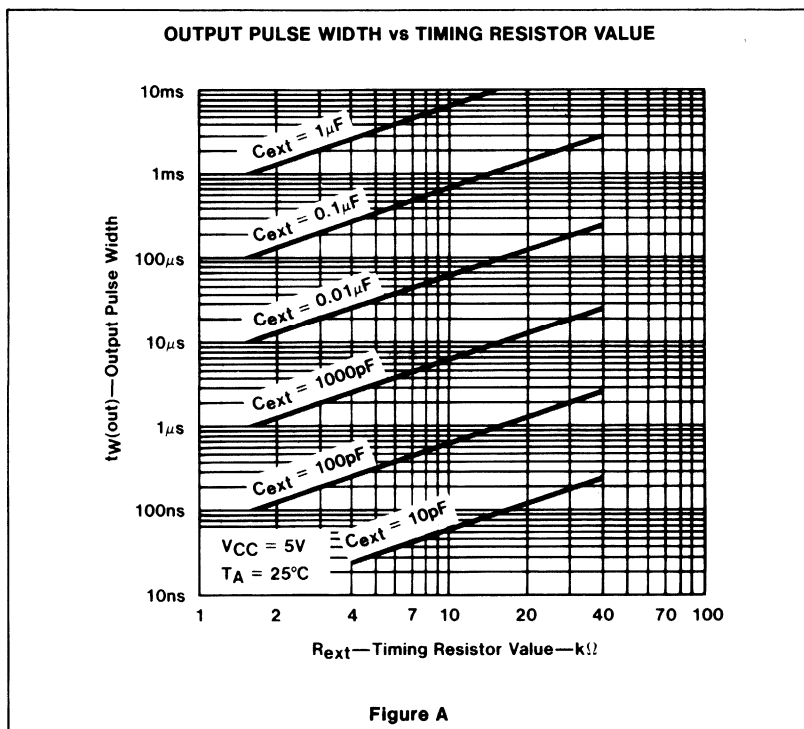
than six decades of timing capacitance (10pF to 10 μ F) and more than one decade of timing resistance (2k Ω to 30k Ω for the 54221, 2k Ω to 40k Ω for the 74221, 2k Ω to 70k Ω for the 54LS221, and 2k Ω to 100k Ω for the 74LS221). Throughout these ranges, pulse width is defined by the following relationship: (See Figure A)

$$t_{W(out)} = C_{ext}R_{ext}\ln 2$$

$$t_{W(out)} \approx 0.7C_{ext}R_{ext}$$

In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4k Ω may be used.

Pin assignments for these devices are identical to those of the "123" so that the "221" can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext} .



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		Quiescent	50			11	mA
	Triggered		80			27	mA	

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
		C _L = 15pF R _L = 400Ω				C _L = 15pF R _L = 2kΩ			
		Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation delay \bar{A} input to Q & \bar{Q} output	Figure 1 C _{ext} =80pF, R _{ext} =2kΩ					70 80	ns ns	
t _{PLH} t _{PHL}	Propagation delay B input to Q & \bar{Q} output	Figure 2 C _{ext} =80pF, R _{ext} =2kΩ					55 65	ns ns	
t _{PLH} t _{PHL}	Propagation delay \bar{R}_D input to \bar{Q} & Q output	Figure 3 C _{ext} =80pF, R _{ext} =2kΩ					40 27	ns ns	
t _w	Minimum output pulse width	C _{ext} = 0pF, R _{ext} =2kΩ		20	50		20	70	ns
t _w	Output pulse width	C _{ext} =80pF, R _{ext} =2kΩ		70	150		70	150	ns
		C _{ext} = 100pF, R _{ext} =10kΩ		650	750		600	750	ns
		C _{ext} = 1μF, R _{ext} =10kΩ		6.5	7.5		6.0	7.5	ns

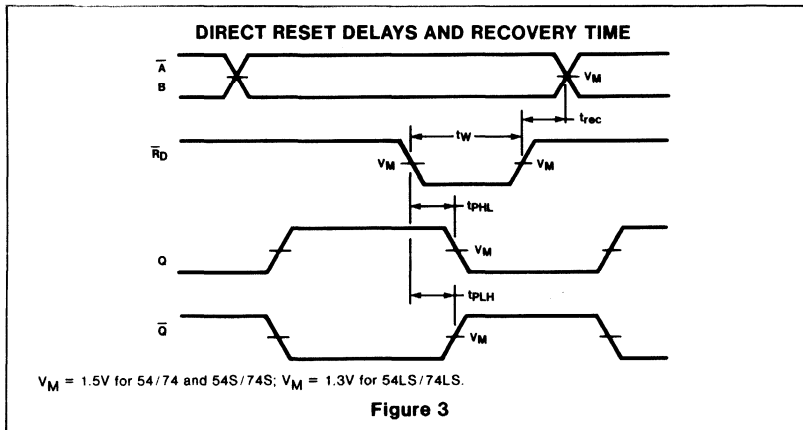
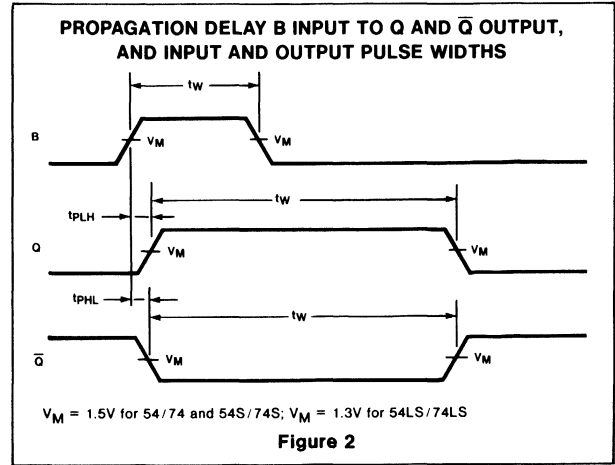
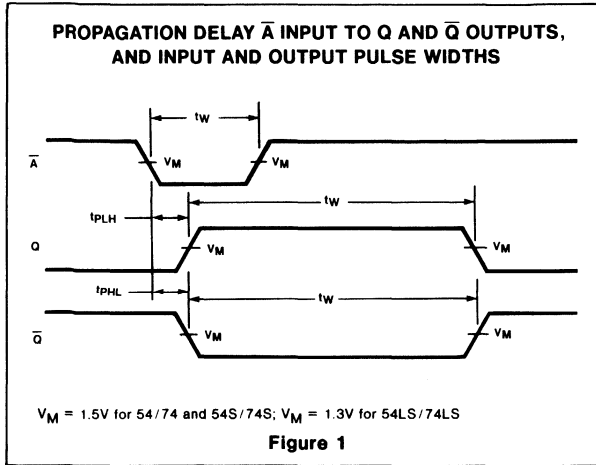
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
		Min	Max	Min	Max	Min	Max		
t _w	Minimum input pulse width to trigger	Figures 1 & 2		50			50	ns	
t _w	Minimum Reset pulse width	Figure 3		20			40	ns	
t _{rec}	Recovery time from Reset to trigger input	Figure 3		15			15	ns	
R _{ext}	External timing resistor range	Mil	1.4	30			1.4	70	kΩ
		Com	1.4	40			1.4	100	kΩ
C _{ext}	External timing capacitance range		0	1000			0	1000	μF
Output duty cycle	R _{ext} = 2kΩ			67				67	%
	R _{ext} = R _{ext} (Max)			90				90	%

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54LS/74LS240

PIN CONFIGURATION

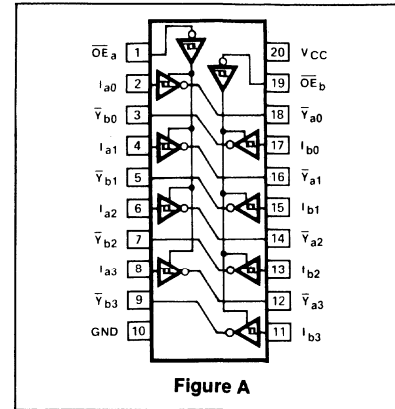


Figure A

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	Fig. A	N74LS240N	
Ceramic DIP	Fig. A	N74LS240F	S54LS240F
Flatpak			

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I _{IH} (μA)				20
	I _{IL} (mA)				-0.2
Outputs	I _{OH} (mA)				-12/-15(a)
	I _{OL} (mA)				12/24(a)

TRUTH TABLE

INPUTS				OUTPUTS	
OE _a	I _a	OE _b	I _b	Y _a	Y _b
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance (off) state

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} =Min V _I =V _{IL} V _{OE} =V _{IL}	I _{OH} =-3.0mA						2.4		V
		I _{OH} =-12mA						2.0		V
		I _{OH} =-15mA(c)						2.0		V
V _{OL} Output LOW voltage	V _{CC} =Min V _I =2V V _{OE} =V _{IL}	I _{OL} =12mA						0.4		V
		I _{OL} =24mA(c)						0.5		V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V							-40	-120	mA
I _{CCH} Supply current HIGH	V _{CC} = Max, V _I = 0V V _{OE} = 0V								23	mA
I _{CCL} Supply current LOW	V _{CC} = Max, V _I = 4.5V V _{OE} = 0V								28	mA
I _{CCZ} Supply current "off"	V _{CC} = Max, V _I = 0V V _{OE} = 4.5V								33	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. This parameter for Commercial Range only.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
								$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1								14	ns
t_{PHL} Propagation delay	Waveform 1								18	ns
t_{PZH} Enable to HIGH	Waveform 6								23	ns
t_{PZL} Enable to LOW	Waveform 7								35	ns
t_{PHZ} Disable from HIGH	Waveform 6	$C_L = 45\text{pF}$							35	ns
		$C_L = 5\text{pF(d)}$							18	ns
t_{PLZ} Disable from LOW	Waveform 7	$C_L = 45\text{pF}$							30	ns
		$C_L = 5\text{pF(d)}$							25	ns

NOTE

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54LS/74LS241

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74LS241N	
Ceramic DIP	Fig. A	N74LS241F	S54LS241F
Flatpak			

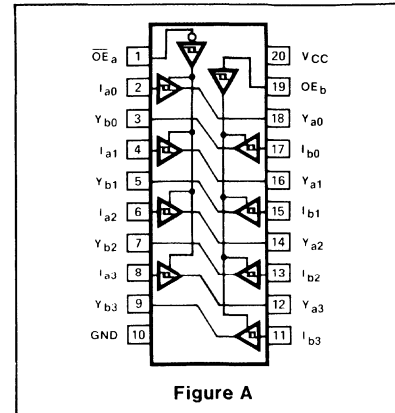


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)				20
	I_{IL} (mA)				-0.2
Outputs	I_{OH} (mA)				-12/-15(a)
	I_{OL} (mA)				12/24(a)

TRUTH TABLE

INPUTS				OUTPUTS	
\overline{OE}_a	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance (off) state

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}$ $V_I = 2V$							2.4		V
	$\overline{VOE} = V_{IL}$ $VOE = 2V$							2.0		V
								2.0		V
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$ $V_I = V_{IL}$								0.4	V
	$\overline{VOE} = V_{IL}$ $VOE = 2V$								0.5	V
I_{OS} Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$							-40	-120	mA
I_{CCH} Supply current HIGH	$V_{CC} = \text{Max}, V_I = 4.5V$ $\overline{VOE} = 0V, VOE = 4.5V$								23	mA
I_{CCL} Supply current LOW	$V_{CC} = \text{Max}, V_I = 0V$ $\overline{VOE} = 0V, VOE = 4.5V$								40	mA
I_{CCZ} Supply current "off"	$V_{CC} = \text{Max}, V_I = 0V$ $\overline{VOE} = 4.5V, VOE = 0V$								43	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. This parameter for Commercial Range only.

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT	
									C _L = 45pF R _L = 667Ω			
			Min	Max	Min	Max	Min	Max	Min	Max		
t _{PLH}	Propagation delay	Waveform 2								18	ns	
t _{PHL}	Propagation delay	Waveform 2								18	ns	
t _{PZH}	Enable to HIGH	Waveform 6								23	ns	
t _{PZL}	Enable to LOW	Waveform 7								28	ns	
t _{PHZ}	Disable from HIGH	Waveform 6	CL = 45pF								35	ns
			CL = 5pF(d)									18
t _{PLZ}	Disable from LOW	Waveform 7	CL = 45pF								30	ns
			CL = 5pF(d)									25

NOTE

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54LS/74LS242

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74LS242N	
Ceramic DIP	Fig. A	N74LS242F	S54LS242F
Flatpak	Fig. A		S54LS242W

PIN CONFIGURATION

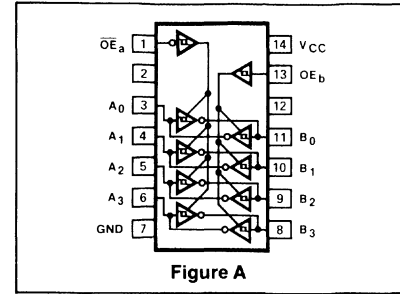


Figure A

FUNCTION TABLE

INPUTS		INPUT/OUTPUT	
\overline{OE}_a	OE_b	A_n	B_n
L	L	INPUT	$B = \overline{A}$
H	L	(Z)	(Z)
L	H	(e)	(e)
H	H	$A = \overline{B}$	INPUT

H = HIGH voltage level
 L = LOW voltage level
 (Z) = High impedance (off) state
 (e) = This condition is not allowed due to excessive currents

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)				20
	I_{IL} (mA)				-0.2
Outputs	I_{OH} (mA)				-12 / -15 ^(a)
	I_{OL} (mA)				12 / 24 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IL}$ $V_{OE} = V_{OE}$ $= V_{IL}$ or $2V$							2.4		V
	$I_{OH} = -3.0\text{mA}$							2.0		V
	$I_{OH} = -12\text{mA}$ $I_{OH} = -15\text{mA}^{(c)}$							2.0		V
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$ $V_{IN} = 2V$ $V_{OE} = V_{OE}$ $= V_{IL}$ or $2V$							0.4		V
	$I_{OL} = 12\text{mA}$ $I_{OL} = 24\text{mA}^{(c)}$							0.5		V
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$, $V_{OUT} = 0V$							-40	-120	mA
I_{CCH} Supply current HIGH	$V_{CC} = \text{Max}$, $V_A = 0V$ $V_{OE} = 0V$, $V_{OE} = 0V$							23		mA
I_{CCL} Supply current LOW	$V_{CC} = \text{Max}$, $V_A = 4.5V$ $V_{OE} = 0V$, $V_{OE} = 0V$							28		mA
I_{CCZ} Supply current "off"	$V_{CC} = \text{Max}$, $V_A = V_B = \text{open}$ $V_{OE} = 4.5V$, $V_{OE} = 0V$							33		mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. This parameter for Commercial Range only.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54H/74H		54S/74S		54LS/74LS		UNIT
										$C_L = 45\text{pF}$ $R_L = 667\Omega$		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1								14	ns	
t_{PHL}	Propagation delay	Waveform 1								18	ns	
t_{PZH}	Enable to HIGH	Waveform 6								23	ns	
t_{PZL}	Enable to LOW	Waveform 7								35	ns	
t_{PHZ}	Disable from HIGH	Waveform 6	CL = 45pF							35	ns	
			CL = 5pF(d)							18	ns	
t_{PLZ}	Disable from LOW	Waveform 7	CL = 45pF							30	ns	
			CL = 5pF(d)							25	ns	

NOTE

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54LS/74LS243

PIN CONFIGURATION

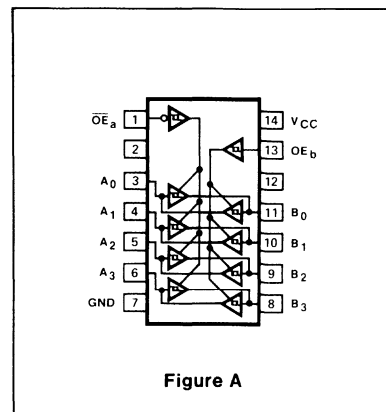


Figure A

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	Fig. A	N74LS243N	
Ceramic DIP	Fig. A	N74LS243F	S54LS243F
Flatpak	Fig. A		S54LS243W

FUNCTION TABLE

INPUTS		INPUT / OUTPUT	
OE _a	OE _b	A _n	B _n
L	L	INPUT	B=A
H	L	(Z)	(Z)
L	H	(e)	(e)
H	H	A=B	INPUT

H = HIGH voltage level
 L = LOW voltage level
 (Z) = High impedance (off) state
 (e) = This condition is not allowed due to excessive currents

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I _{IH} (μA)				20
	I _{IL} (mA)				-0.2
Outputs	I _{OH} (mA)				-12/-15(a)
	I _{OL} (mA)				12/24(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = Min V _{IN} = 2V							2.4		V
	V _{OE} = V _{OE}							2.0		V
	= V _{IL} or 2V							2.0		V
V _{OL} Output LOW voltage	V _{CC} = Min V _{IN} = V _{IL}								0.4	V
	V _{OE} = V _{OE} = V _{IL} or 2V								0.5	V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V							-40	-120	mA
I _{CCH} Supply current HIGH	V _{CC} = Max, V _A = 4.5V V _{OE} = 0V, V _{OE} = 0V								30	mA
I _{CCL} Supply current LOW	V _{CC} = Max, V _A = 0V V _{OE} = 0V, V _{OE} = 0V								40	mA
I _{CCZ} Supply current "off"	V _{CC} = Max, V _A = V _B = open V _{OE} = 4.5V, V _{OE} = 0V								43	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. This parameter for Commercial Range only.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
								$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 2								18	ns
t_{PHL} Propagation delay	Waveform 2								18	ns
t_{PZH} Enable to HIGH	Waveform 6								23	ns
t_{PZL} Enable to LOW	Waveform 7								30	ns
t_{PHZ} Disable from HIGH	Waveform 6	$C_L = 45\text{pF}$							35	ns
		$C_L = 5\text{pF}(d)$							18	ns
t_{PLZ} Disable from LOW	Waveform 7	$C_L = 45\text{pF}$							30	ns
		$C_L = 5\text{pF}(d)$							25	ns

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54LS/74LS244

PIN CONFIGURATION

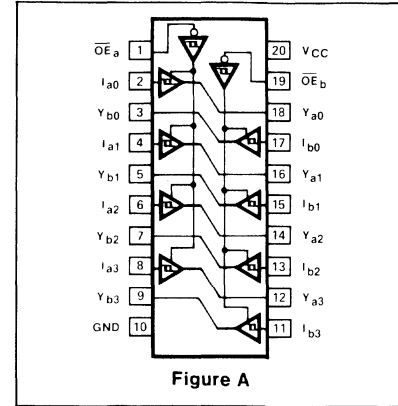


Figure A

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74LS244N	
Ceramic DIP	Fig. A	N74LS244F	S54LS244F
Flatpak			

TRUTH TABLE

INPUTS				OUTPUTS	
\overline{OE}_a	I_a	\overline{OE}_b	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)				20
	I_{IL} (mA)				-0.2
Outputs	I_{OH} (mA)				-12/-15(a)
	I_{OL} (mA)				12/24(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}$ $V_I = 2V$							2.4		V
	$V_{OE} = V_{IL}$ $I_{OH} = -3.0mA$							2.0		V
	$I_{OH} = -15mA^{(c)}$							2.0		V
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$ $V_I = V_{IL}$								0.4	V
	$V_{OE} = V_{IL}$ $I_{OL} = 12mA$								0.5	V
I_{OS} Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$							-40	-120	mA
I_{CCH} Supply current HIGH	$V_{CC} = \text{Max}, V_I = 4.5V$ $V_{OE} = 0V$								23	mA
I_{CCL} Supply current LOW	$V_{CC} = \text{Max}, V_I = 0V$ $V_{OE} = 0V$								40	mA
I_{CCZ} Supply current "off"	$V_{CC} = \text{Max}, V_I = 0V$ $V_{OE} = 4.5V$								43	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. This parameter for Commercial Range only.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
								$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 2								18	ns
t_{PHL} Propagation delay	Waveform 2								18	ns
t_{PZH} Enable to HIGH	Waveform 6								23	ns
t_{PZL} Enable to LOW	Waveform 7								28	ns
t_{PHZ} Disable from HIGH	Waveform 6	CL = 45pF							35	ns
		CL = 5pF(d)							18	ns
t_{PLZ} Disable from LOW	Waveform 7	CL = 45pF							30	ns
		CL = 5pF(d)							25	ns

NOTE

- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54LS/74LS245 (Preliminary Data)

PIN CONFIGURATION

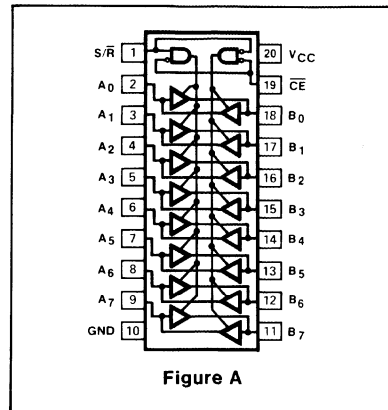


Figure A

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74LS245N	
Ceramic DIP	Fig. A	N74LS245F	S54LS245F
Flatpak			

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)				20
	I_{IL} (mA)				-0.2
Outputs	I_{OH} (μA)				-12/-15 ^(a)
	I_{OL} (mA)				12/24 ^(a)

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
CE	S/R	A _n	B _n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance "off" state

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	$V_{CC} = \text{Min}$ $V_{IN} = 2V$ $V_{CE} = V_{IL}$	$I_{OH} = -3.0mA$						2.4		V
		$I_{OH} = -12mA$						2.0		V
		$I_{OH} = -15mA^{(c)}$						2.0		V
V _{OL} Output LOW voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IL}$ $V_{CE} = V_{IL}$	$I_{OL} = 12mA$						0.4		V
		$I_{OL} = 24mA^{(c)}$						0.5		V
I _{OS} Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$							-40	-120	mA
I _{CCH} Supply current HIGH	$V_{CC} = \text{Max}, V_A = 4.5V$ $V_{CE} = 0V, V_{S/R} = 0V$							70		mA
I _{CCL} Supply current LOW	$V_{CC} = \text{Max}, V_A = 0V$ $V_{CE} = 0V, V_{S/R} = 0V$							90		mA
I _{CCZ} Supply current "off"	$V_{CC} = \text{Max}, V_A = V_B = \text{open}$ $V_{CE} = 4.5V, V_{S/R} = 0V$							95		mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. This parameter for Commercial Range only.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
								$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
tPLH Propagation delay	Waveform 2								12	ns
tPHL Propagation delay	Waveform 2								12	ns
tpZH Enable to HIGH	Waveform 6								40	ns
tpZL Enable to LOW	Waveform 7								40	ns
tPHZ Disable from HIGH	Waveform 6	CL = .45pF							35	ns
		CL = 5pF(d)							18	ns
tPLZ Disable from LOW	Waveform 7	CL = 45pF							30	ns
		CL = 5pF(d)							25	ns

NOTE

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

**54S/74S251
54LS/74LS251A**

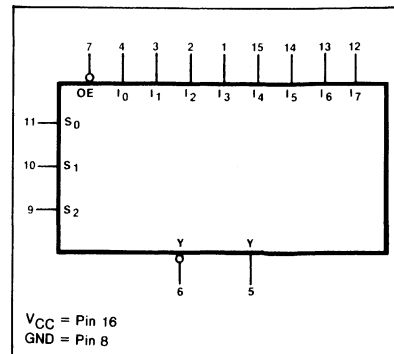
DESCRIPTION

The "251" is a high speed 8-Input Digital Multiplexer providing, in one package, the ability to select one bit of data from up to eight sources. Assertion and negation outputs are both provided. Both outputs are 3-state buffers which can be used for further multiplexer expansion, or for driving a 3-state bus.

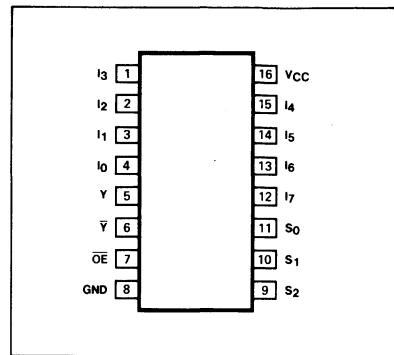
FEATURES

- High speed 8-to-1 multiplexing
- True and complement outputs
- Both outputs are 3-State for further multiplexer expansion
- 3-State outputs are buffer type with 12mA/24mA outputs for Military/Commercial applications

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N74S251N	•	N74LS251AN
Ceramic DIP	N74S251F	•	N74LS251AF	S54S251F • S54LS251AF
Flatpak				S54S251W • S54LS251AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S ₀ -S ₂	Select inputs	I _H (μA)		50	20
		I _L (mA)		-2.0	-0.4
I ₀ -I ₇	Multiplexer inputs	I _H (μA)		50	20
		I _L (mA)		-2.0	-0.4
OE	Output Enable (active LOW) input	I _H (μA)		50	20
		I _L (mA)		-2.0	-0.4
Y	3-State multiplexer output	I _{OH} (mA)		-2/-6.5 ^(a)	-1/-2.6 ^(a)
		I _{OL} (mA)		20	12/24 ^(a)
Y-bar	3-State complementary multiplexer output	I _{OH} (mA)		-2/-6.5 ^(a)	-1/-2.6 ^(a)
		I _{OL} (mA)		20	12/24 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "251" is a logical implementation of a single pole, 8-position switch with the state of the three Select inputs (S_0, S_1, S_2) controlling the switch position. Assertion (Y) and negation (\bar{Y}) outputs are both provided. The Output Enable input (\overline{OE}) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \overline{OE} (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

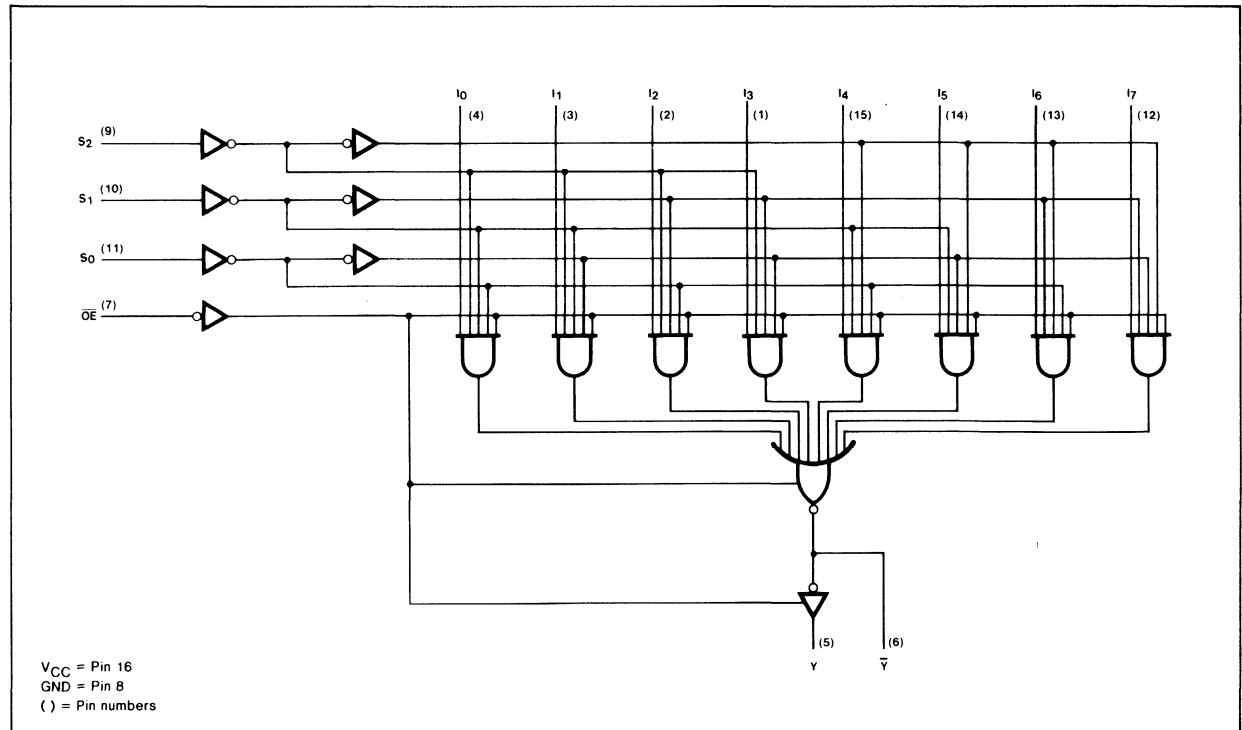
Both outputs are in the high impedance (high Z) state when the Output Enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State devices are tied together. Design of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

				INPUTS								OUTPUTS	
\overline{OE}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	\bar{Y}	\bar{Y}
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance (off)

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min I _{OL} = 20mA I _{OL} = 12mA I _{OL} = 24mA				0.5			V
						0.4		V
						0.5 ^(c)		V
V _{OH} Output HIGH voltage	V _{CC} = Min I _{OH} = See Fan Out Table			2.4		2.4		V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V			-40	-100	-30	-100	mA
I _{CC} Supply current	V _{CC} = Max Outputs LOW Outputs "off"						10	mA
					85		12	mA

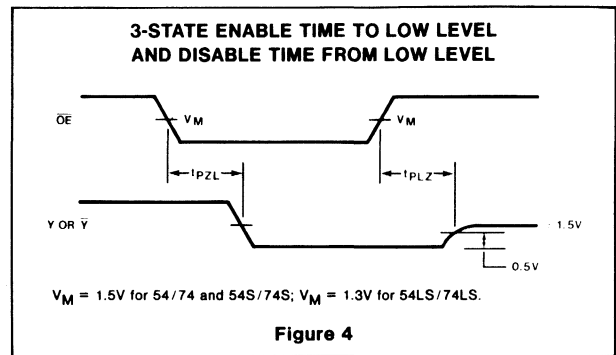
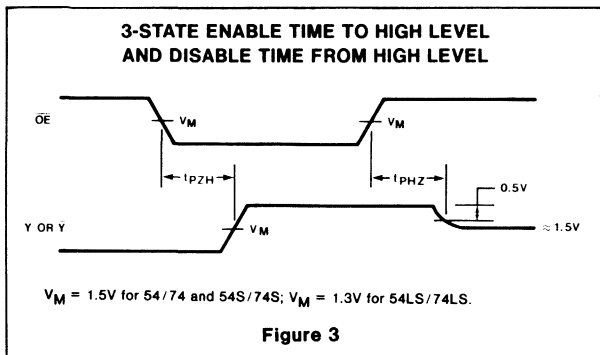
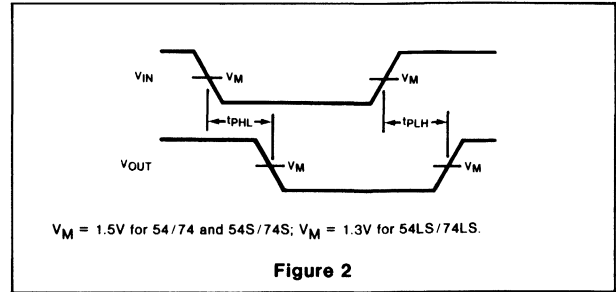
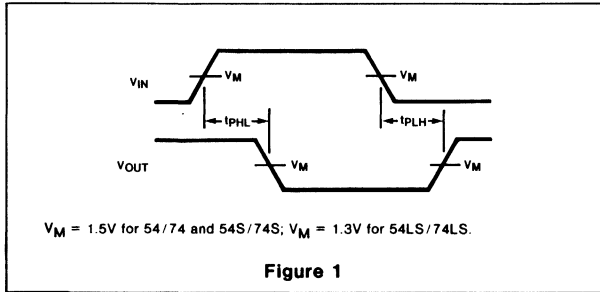
AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 280Ω		C _L = 45pF R _L = 667Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagatation delay Select to Y output	Figure 2			18 19.5		35 40	ns ns
t _{PLH} t _{PHL}	Propagatation delay Select to \bar{Y} output	Figure 1			15 13.5		28 33	ns ns
t _{PLH} t _{PHL}	Propagatation delay Data to Y output	Figure 2			12 12		28 28	ns ns
t _{PLH} t _{PHL}	Propagatation delay Data to \bar{Y} output	Figure 1			7.0 7.0		15 15	ns ns
t _{PZH}	Output enable to HIGH level	Figure 3			19.5		25	ns
t _{PZL}	Output enable to LOW level	Figure 4			21		25	ns
t _{PHZ}	Output disable from HIGH level	Figure 3			12		45	ns
		Figure 3, C _L = 5pF ^(d)			8.5		30	ns
t _{PLZ}	Output disable from LOW level	Figure 4			16		25	ns
		Figure 4, C _L = 5pF ^(d)			14		20	ns

NOTES

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial Range only.
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC WAVEFORMS



**54S/74S253
54LS/74LS253**

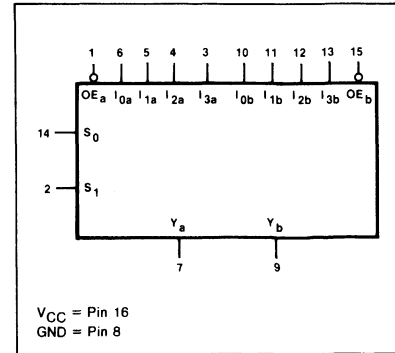
DESCRIPTION

The "253" is a Dual 4-Input Multiplexer with 3-State outputs. It selects two bits of data from four sources using common select inputs. The 3-State outputs are controlled by separate Output Enable (OE) inputs which set the outputs into the high impedance state when HIGH.

FEATURES

- 3-State outputs for bus interface and multiplex expansion
- Common Select inputs
- Separate Output Enable inputs

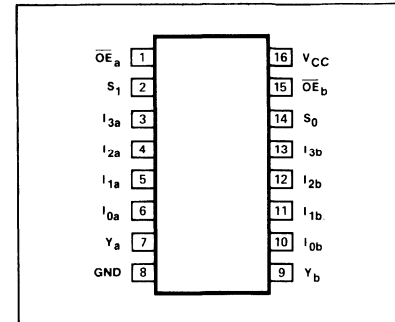
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$	
	Plastic DIP	N74S253N	• N74LS253N	
Ceramic DIP	N74S253F	• N74LS253F	S54S253F	• S54LS253F
Flatpak			S54S253W	• S54LS253W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S_0, S_1	Common Select inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$\overline{OE}_a, \overline{OE}_b$	Output Enable (Active LOW) inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$I_{0a} - I_{3a}$	Data inputs from multiplexer "a"	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$I_{0b} - I_{3b}$	Data inputs from multiplexer "b"	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
Y_a, Y_b	3-State outputs	I_{OH} (mA) I_{OL} (mA)		-2/-6.5(a) 20	-1/-2.6(a) 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "253" has two identical 4-input Multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S₀, S₁). When the individual Output Enable (E_{0a}, E_{0b}) inputs of the 4-input Multiplexers are HIGH, the outputs are forced to a high impedance (high Z) state.

The "253" is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$Y_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S_0} + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1b} \cdot \overline{S_1} \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S_0} + I_{3b} \cdot S_1 \cdot S_0)$$

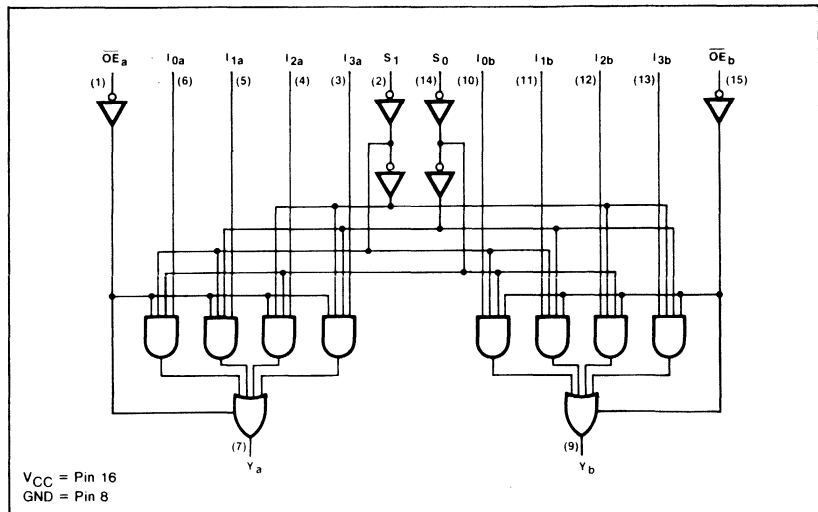
All but one device must be in the high impedance state to avoid high currents exceeding the maximum ratings, if the outputs of 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S ₀	S ₁	I ₀	I ₁	I ₂	I ₃	\overline{OE}	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't Care
 (Z) = High impedance (off) state

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

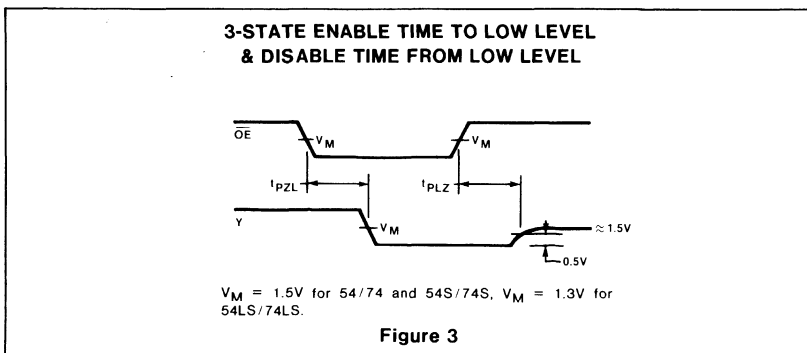
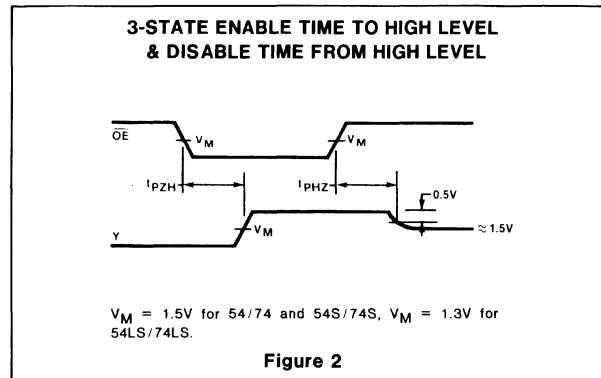
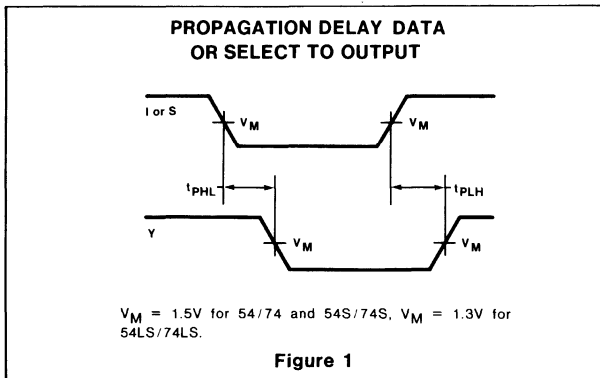
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min I _{OL} = 20mA				0.5			V
							0.4	V
							0.5(c)	V
V _{OH} Output HIGH voltage	V _{CC} = Min I _{OH} = See Table			2.4		2.4		V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V			-40	-100	-15	-100	mA
I _{CC} Supply current	V _{CC} = Max	Outputs LOW			70		12	mA
		Outputs "off"					14	mA

NOTES
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
 c. This parameter for Commercial range only.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
				$C_L=15\text{pF}$ $R_L=280\Omega$		$C_L=15\text{pF}$ $R_L=2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output				9.0 9.0		25 20	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output				18 18		45 32	ns ns
t_{PZH}	Output enable time to HIGH level				13		23	ns
t_{PZL}	Output enable time to LOW level				14		23	ns
t_{PHZ}	Output disable time from HIGH level				8.5		41	ns
t_{PLZ}	Output disable time from LOW level				14		27	ns

AC WAVEFORMS



54LS/74LS256 (Preliminary data)

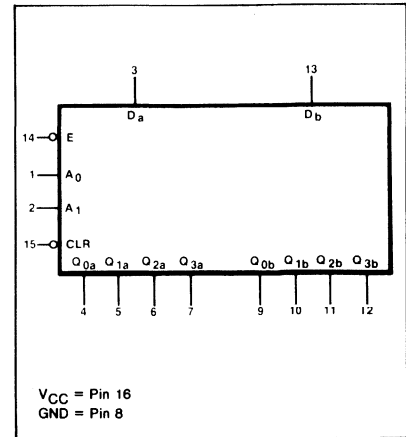
DESCRIPTION

The "256" is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address inputs (A_0 , A_1), an active LOW Enable input (\bar{E}) and an active LOW Clear input. Each latch has a D input and four outputs. The "256" combines the features of a dual 1-of-4 demultiplexer and an 8-bit transparent latch into one 16 pin package.

FEATURES

- Combines dual demultiplexer and 8-bit latch
- Serial-to-Parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common clear input
- Useful as dual 1-of-4 active HIGH decoder.

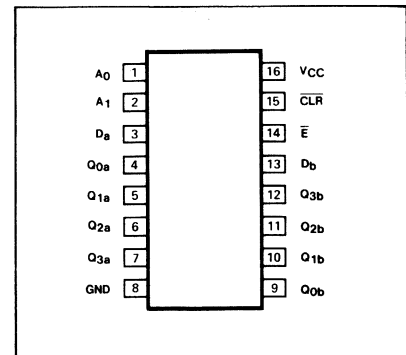
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS256N	
Ceramic DIP	N74LS256F	S54LS256F
Flatpak		S54LS256W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_0, A_1	Address inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$			20 -0.4
D_a, D_b	Data inputs	$I_{IH} (\mu A)$ $I_{IL} (mA)$			20 -0.4
\bar{E}	Latch Enable (active LOW) input	$I_{IH} (\mu A)$ $I_{IL} (mA)$			40 -0.8
\overline{CLR}	Clear (active LOW) input	$I_{IH} (\mu A)$ $I_{IL} (mA)$			20 -0.4
$Q_{0a}-Q_{3a}$	Outputs from Latch "a"	$I_{OH} (\mu A)$ $I_{OL} (mA)$			-400 4/8 (a)
$Q_{0b}-Q_{3b}$	Outputs from Latch "b"	$I_{OH} (\mu A)$ $I_{OL} (mA)$			-400 4/8 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "256" Dual Addressable Latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see the function table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the data input with all unaddressed latches remaining in their previous states.

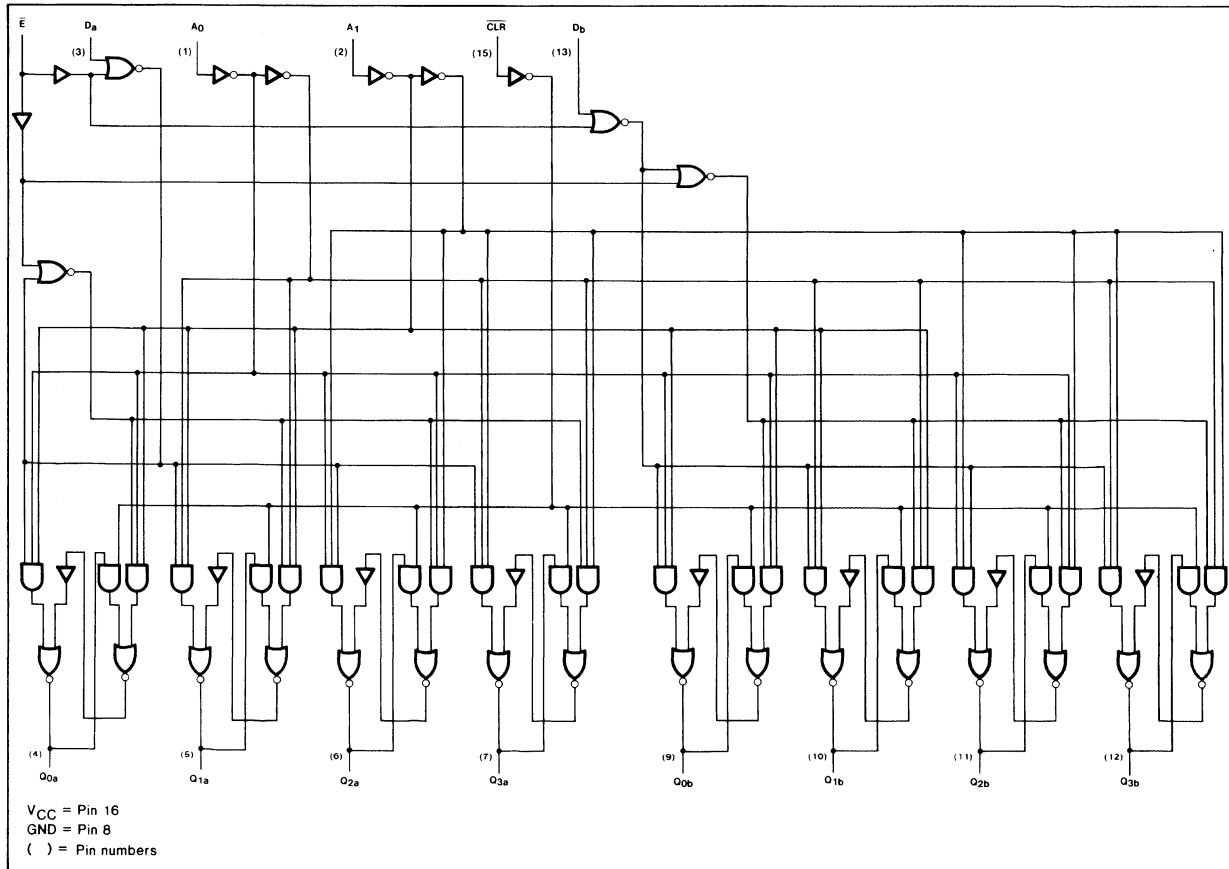
In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode, ($\overline{\text{CLR}} = \overline{\text{E}} = \text{LOW}$) addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the address and data inputs.

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	$\overline{\text{CLR}}$	$\overline{\text{E}}$	D	A ₀	A ₁	Q ₀	Q ₁	Q ₂	Q ₃
Clear	L	H	X	X	X	L	L	L	L
Demultiplex (active HIGH decoder when D=H)	L	L	d	L	L	Q=d	L	L	L
	L	L	d	H	L	L	Q=d	L	L
	L	L	d	L	H	L	L	Q=d	L
	L	L	d	H	H	L	L	L	Q=d
Store (do nothing)	H	H	X	X	X	q ₀	q ₁	q ₂	q ₃
Addressable latch	H	L	d	L	L	Q=d	q ₁	q ₂	q ₃
	H	L	d	H	L	q ₀	Q=d	q ₂	q ₃
	H	L	d	L	H	q ₀	q ₁	Q=d	q ₃
	H	L	d	H	H	q ₀	q ₁	q ₂	Q=d

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 X = Don't care.
 d = HIGH or LOW data one setup time prior to LOW-to-HIGH Enable transition.
 q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current						36	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 2kΩ						
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Enable to output						35 24	ns ns
t _{PLH} t _{PHL}	Propagation delay Data to output						32 21	ns ns
t _{PLH} t _{PHL}	Propagation delay Address to output						38 29	ns ns
t _{PHL}	Propagation delay clear to output						27	ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside cover for 54S/74S and 54LS/74LS specifications.

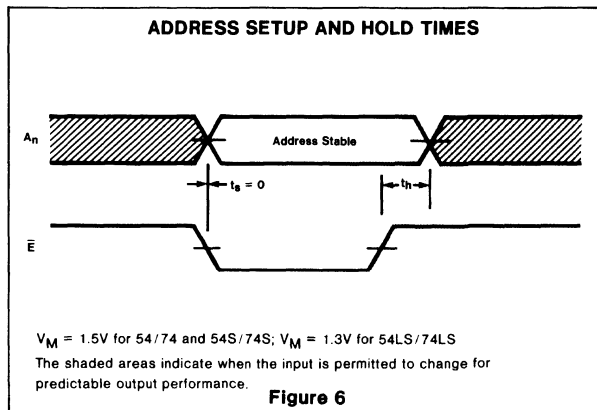
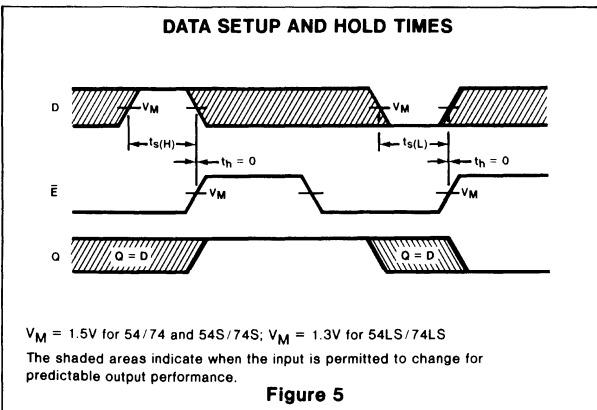
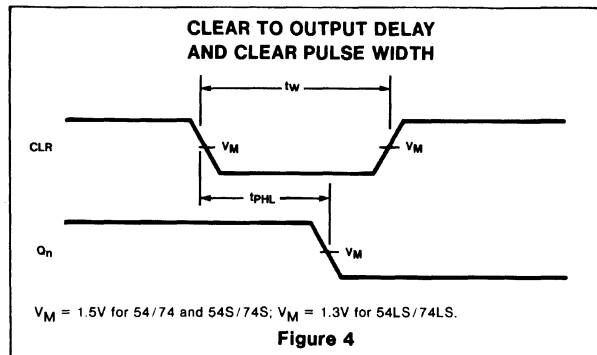
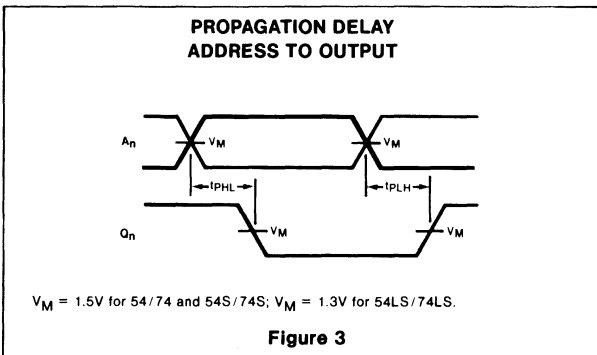
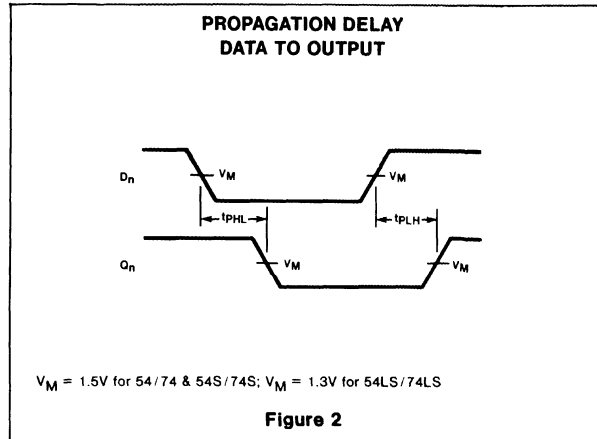
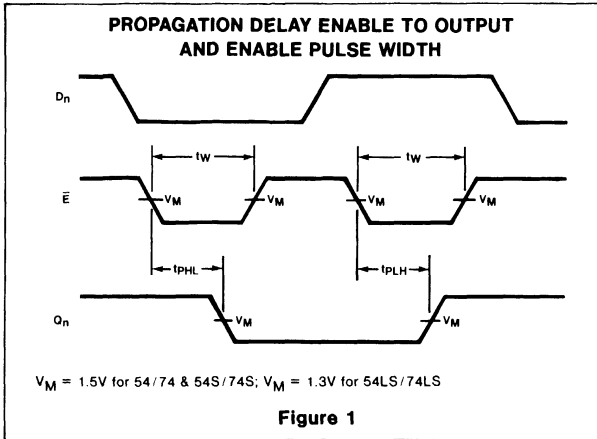
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w	Enable pulse width					15		ns
t _w	Clear pulse width					15		ns
t _s (H)	Setup time HIGH Data to Enable					20		ns
t _h (H)	Hold time HIGH Data to Enable					0		ns
t _s (L)	Setup time LOW Data to Enable					15		ns
t _h (L)	Hold time LOW Data to Enable					0		ns
t _s	Setup time Address to Enable ^(c)					0		ns
t _h	Hold time Address to Enable ^(d)					10		ns

NOTES

- c. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- d. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS



QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (3-STATE) 54/74 SERIES "257"

54S/74S257 54LS/74LS257A

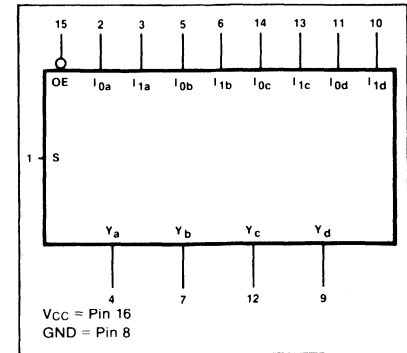
DESCRIPTION

The Quad 2-Input Multiplexer with 3-State outputs can select four bits of data from two sources using a common Data Select input. The four outputs of the "257" present data in true (non-inverted) form. The outputs may be set to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) Input allowing the outputs to interface directly with 3-State bus-organized systems.

FEATURES

- Multifunction capability
- Non-inverting data path
- 3-State outputs
- Replaces DM8123 for higher performance

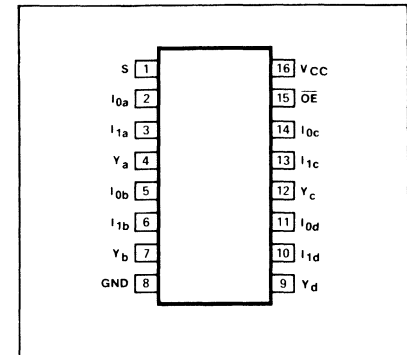
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	N74S257N • N74LS257AN	
Ceramic DIP	N74S257F • N74LS257AF	S54S257F • S54LS257AF
Flatpak		S54S257W • S54LS257AW

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S	Select input	I_{IH} (μA) I_{IL} (mA)		100 -4.0	40 -0.8
\overline{OE}	Output Enable (Active LOW) input	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$I_{0a} - I_{0d}$	Data inputs from Source 0	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$I_{1a} - I_{1d}$	Data inputs from Source 1	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$Y_a - Y_d$	3-State outputs	I_{OH} (mA) I_{OL} (mA)		-2/-6.5 20 (a)	-1/-2.6 (a) 12/24 (a)

NOTE

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "257" has four identical 2-Input Multiplexers with 3-State outputs which select four bits of data from two sources under control of a common Data Select Input (S). The I₀ inputs are selected when the Select Input is LOW and the I₁ inputs are selected when the Select Input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

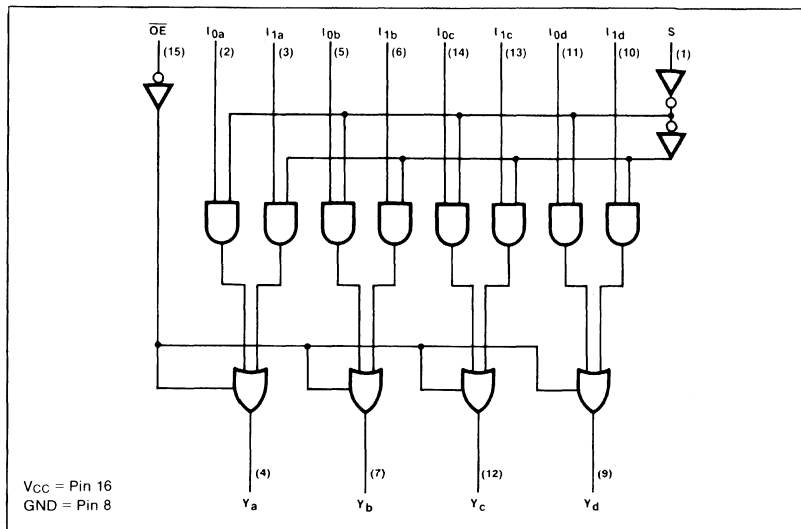
Outputs are forced to a high impedance "off" state when the Output Enable Input (\overline{OE}) is HIGH. All but one device must be in the high impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
\overline{OE}	S	I ₀	I ₁	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance (off) state

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

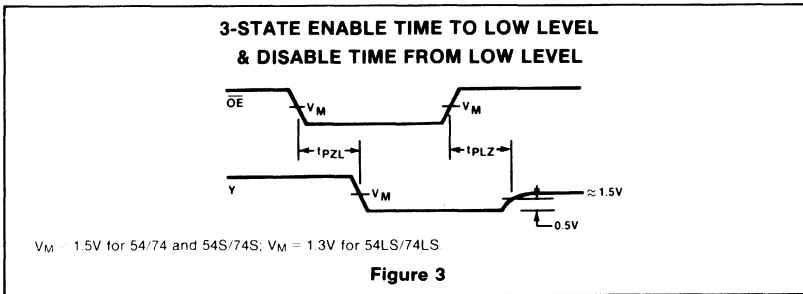
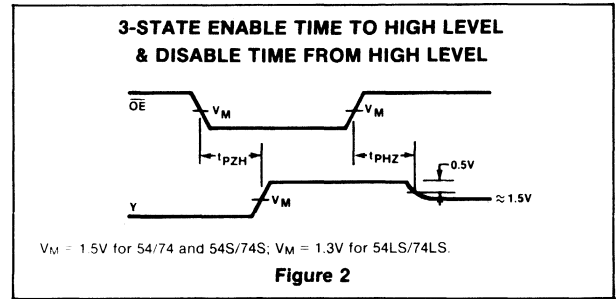
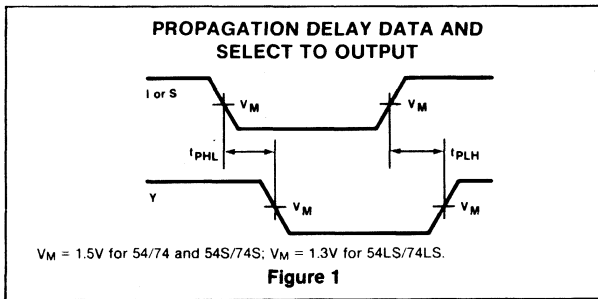
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
VOL Output LOW voltage	VCC = Min	I _{OL} = 20mA			0.5			V
		I _{OL} = 12mA					0.4	V
		I _{OL} = 24mA					0.5 ^(c)	V
VOH Output HIGH voltage	VCC = Min I _{OH} = See Fan Out Table			2.4		2.4		V
Ios Output short circuit current	VCC = Max, V _{OUT} = 0V			-40	-100	-30	-100	mA
Icc Supply current	VCC = Max	Outputs HIGH			68		10	mA
		Outputs LOW			93		16	mA
		Outputs "off"			99		19	mA

NOTE
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
 c. This parameter for Commercial range only.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
				$C_L = 15\text{pF}$ $R_L = 280\Omega$	$C_L = 45\text{pF}$ $R_L = 667\Omega$			
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output				7.5 6.5		18 18	ns
t_{PLH} t_{PHL}	Propagation delay Select to output				15 15		21 24	ns
t_{PZH}	Output enable to HIGH level				19.5		16	ns
t_{PZL}	Output enable to LOW level				21		24	ns
t_{PHZ}	Output disable from HIGH level	Figure 3	$C_L = 5\text{pF}$		8.5		15	ns
			$C_L = 45\text{pF}$				43	ns
t_{PLZ}	Output disable from LOW level	Figure 2	$C_L = 5\text{pF}$		14		15	ns
			$C_L = 45\text{pF}$				19	ns

AC WAVEFORMS



QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (3-STATE) 54/74 SERIES "258"

54S/74S258
54LS/74LS258A

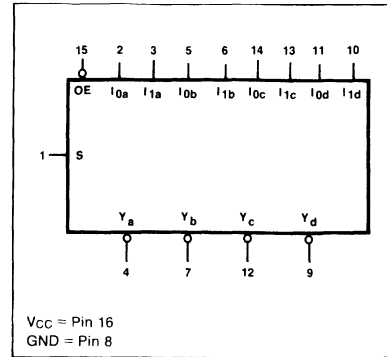
DESCRIPTION

The "258" is a Quad 2-Input Multiplexer with 3-State outputs which can select four bits of data from two sources using a common Data Select input. The four outputs of the device present data in the complementary (inverted) form. The outputs may be set to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) Inputs allowing the outputs to interface directly with 3-State bus-organized systems.

FEATURES

- Multifunction capability
- Inverting data path
- 3-State outputs
- See "257" for non-inverting version

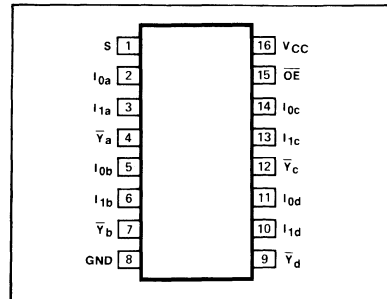
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$		$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $-125^\circ C$	
Plastic DIP	N74S258N	• N74LS258AN		
Ceramic DIP	N74S258F	• N74LS258AF	S54S258F	• S54LS258AF
Flatpak			S54S258W	• S54LS258AW

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S	Select input	I_{IH} (μA) I_{IL} (mA)		100 -4.0	40 -0.8
\overline{OE}	Output Enable (Active LOW) input	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$I_{0a} - I_{0d}$	Data inputs from Source 0	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$I_{1a} - I_{1d}$	Data inputs from Source 1	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$\overline{Y}_a - \overline{Y}_d$	3-State outputs	I_{OH} (mA) I_{OL} (mA)		-2/-6.5 ^(a) 20	-1/-2.6 ^(a) 12/24 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "258" has four identical 2-Input Multiplexers with 3-State outputs which select four bits of data from two sources under control of a common Data Select Input (S). The I₀ inputs are selected when the Select Input is LOW and the I₁ inputs are selected when the Select Input is HIGH. Data appears at the outputs in inverted (complementary) form.

The "258" is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

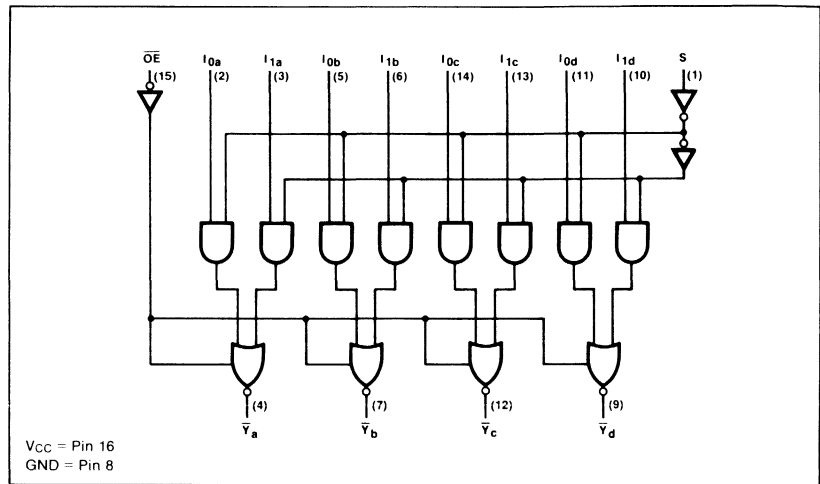
Outputs are forced to a high impedance "off" state when the Output Enable Input (\overline{OE}) is HIGH. All but one device must be in the high impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
\overline{OE}	S	I ₀	I ₁	\overline{Y}
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance (off) state

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min I _{OL} = 20mA				0.5			V
							0.4	V
							0.5 (c)	V
V _{OH} Output HIGH voltage	V _{CC} = Min I _{OH} = See Fan Out Table			2.4		2.4		V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V			-40	-100	-30	-100	mA
I _{CC} Supply current	V _{CC} = Max	Outputs HIGH			56		7.0	mA
		Outputs LOW			81		14	mA
		Outputs "off"			87		19	mA

NOTES

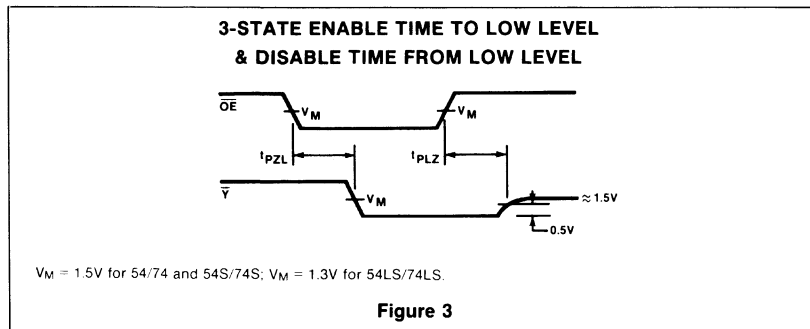
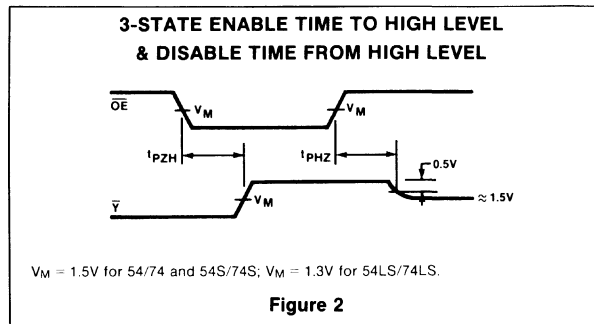
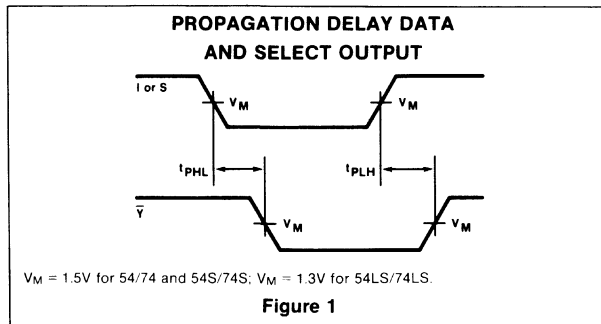
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial range only.

QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (3-STATE) 54/74 SERIES "258"

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
				$C_L = 15\text{pF}$ $R_L = 280\Omega$		$C_L = 45\text{pF}$ $R_L = 667\Omega$			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation delay Data to output				6.0 6.0		14 14	ns	
t_{PLH} t_{PHL}	Propagation delay Select to output				12 12		21 24	ns	
t_{PZH}	Output enable to HIGH level				19.5		16	ns	
t_{PZL}	Output enable to LOW level				21		24	ns	
t_{PHZ}	Output disable from HIGH level	Figure 2	$C_L = 5\text{pF}$			8.5		15	ns
			$C_L = 45\text{pF}$					43	
t_{PLZ}	Output disable from LOW level	Figure 3	$C_L = 5\text{pF}$			14		15	ns
			$C_L = 45\text{pF}$					19	

AC WAVEFORMS



54/74259—See 9334
54LS/74LS259 (Preliminary data)

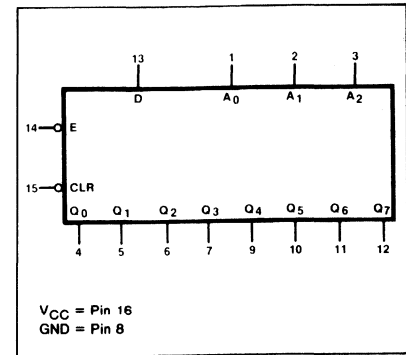
DESCRIPTION

The "259" is an 8-Bit Addressable Latch with these control inputs; three Address inputs (A_0, A_1, A_2), an active LOW Enable input (\bar{E}) and an active LOW Clear input (\bar{CLR}). Each latch has a common D input and a separate Q output. The "259" combines the features of a 1-of-8 demultiplexer and 8-bit transparent latch into one 16 pin package.

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-Parallel capability
- Output from each storage bit available
- Random (Addressable) data entry
- Easily expandable
- Common Clear input
- Useful as dual 1-of-8 active HIGH decoder
- See the NE590 for 250 mA output version

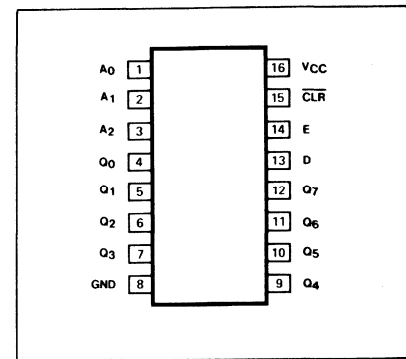
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS259N	
Ceramic DIP	N74LS259F	S54LS259F
Flatpak		S54LS259W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION	54/74	54S/74S	54LS/74LS
A_0, A_1, A_2	Address inputs			$I_{IH} (\mu A)$ $I_{IL} (mA)$ 20 -0.4
D	Data input			$I_{IH} (\mu A)$ $I_{IL} (mA)$ 20 -0.4
\bar{E}	Latch Enable (active LOW) input			$I_{IH} (\mu A)$ $I_{IL} (mA)$ 40 -0.8
\bar{CLR}	Clear (active LOW) input			$I_{IH} (\mu A)$ $I_{IL} (mA)$ 20 -0.4
Q_0-Q_7	Latch outputs			$I_{OH} (\mu A)$ $I_{OL} (mA)$ -400 4/8 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "259" Addressable Latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see the function table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, (CLR = \bar{E} = LOW) addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the address and data inputs.

MODE SELECT—FUNCTION TABLE

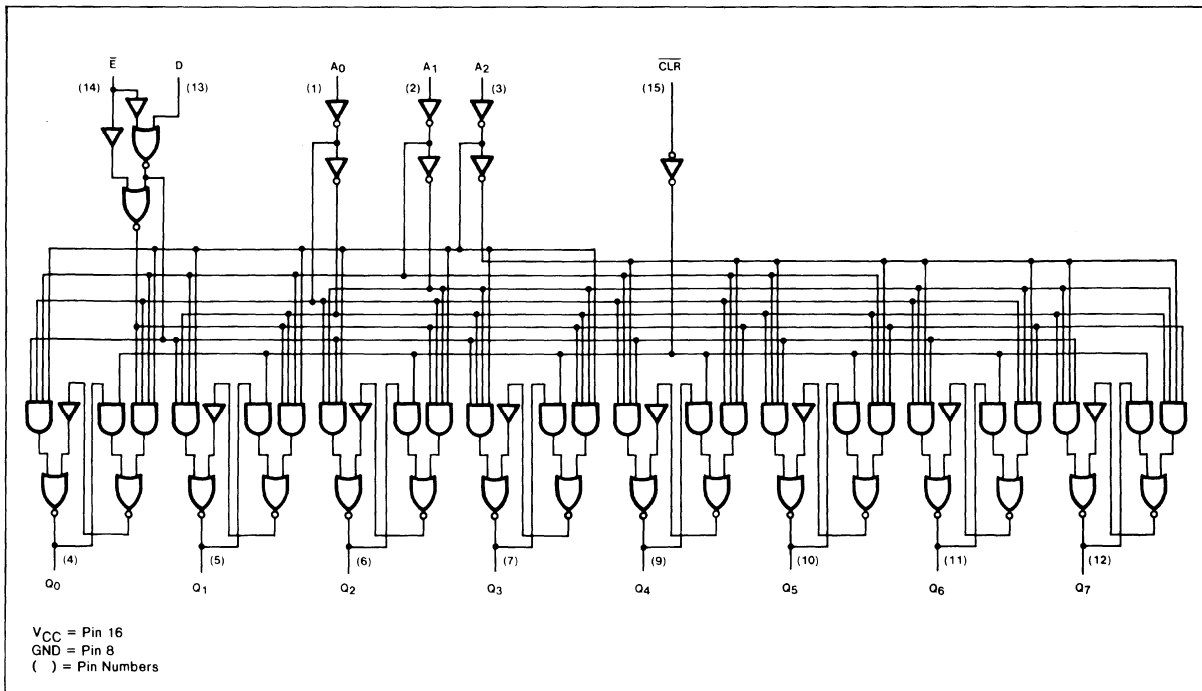
OPERATING MODE	INPUTS						OUTPUTS							
	CLR	\bar{E}	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L

	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q=d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q=d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q=d	q ₃	q ₄	q ₅	q ₆	q ₇

	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q=d

H = HIGH voltage level steady state
 L = LOW voltage level steady state
 X = Don't care
 d = HIGH or LOW data one setup time prior to LOW-to-HIGH Enable transition
 q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						36	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Enable to output	Figure 1						35 24	ns ns
t _{PLH} Propagation delay t _{PHL} Data to output	Figure 2						32 21	ns ns
t _{PLH} Propagation delay t _{PHL} Address to output	Figure 3						38 29	ns ns
t _{PHL} Propagation delay clear to output	Figure 4						27	ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

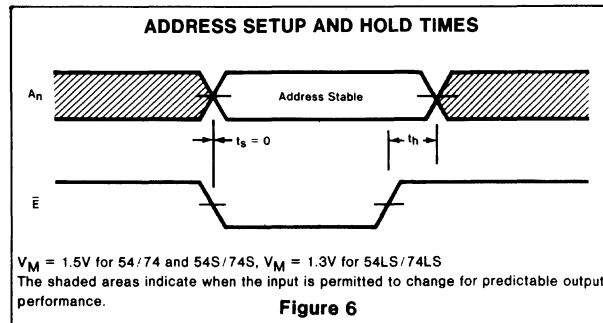
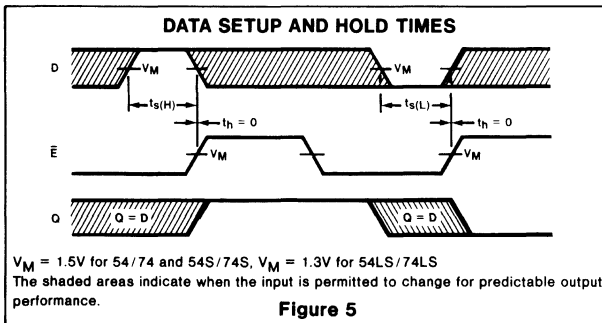
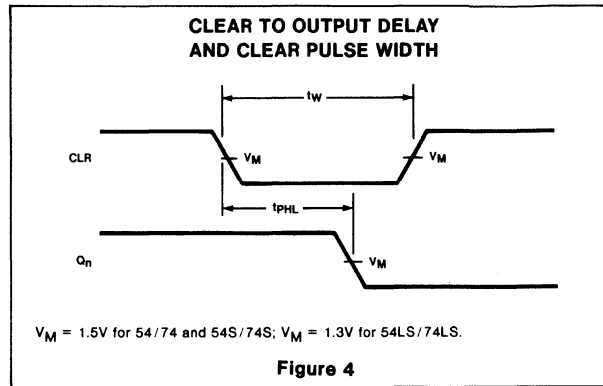
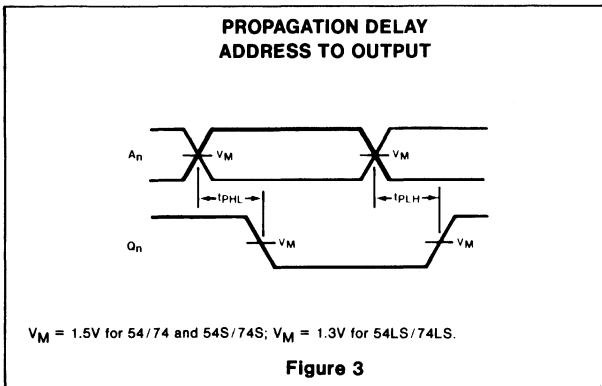
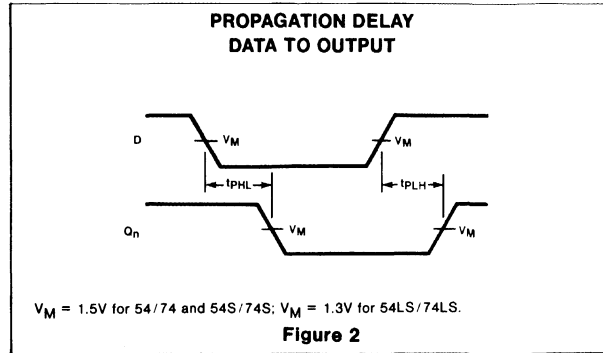
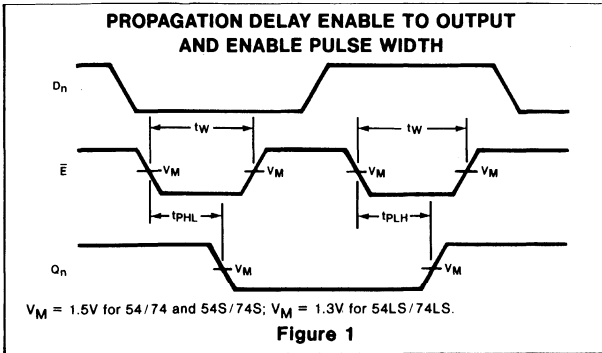
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Enable pulse width	Figure 1					15		ns
t _w Clear pulse width	Figure 4					15		ns
t _s (H) Setup time HIGH Data to Enable	Figure 5					20		ns
t _h (H) Hold time HIGH Data to Enable	Figure 5					0		ns
t _s (L) Setup time LOW Data to Enable	Figure 5					15		ns
t _h (L) Hold time LOW Data to Enable	Figure 5					0		ns
t _s Setup time Address to Enable ^(c)	Figure 6					0		ns
t _h Hold time Address to Enable ^(d)	Figure 6					10		ns

NOTES

- c. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- d. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS



54S/74S260
54LS/74LS260

PIN CONFIGURATION

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74S260N • N74LS260N	
Ceramic DIP	Fig. A	N74S260F • N74LS260F	S54S260F • S54LS260F
Flatpak	Fig. A		S54S260W • S54LS260W

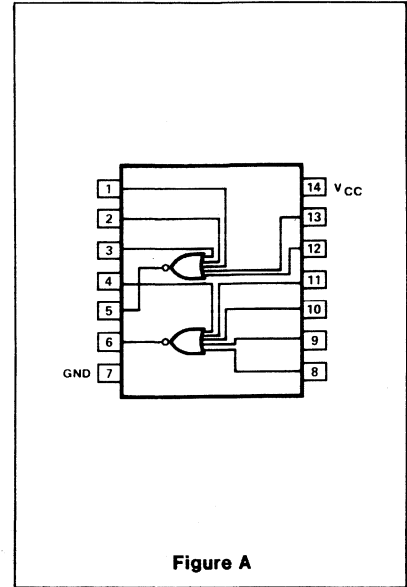


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)			50	20
	I_{IL} (mA)			-2.0	-0.36
Outputs	I_{OH} (μA)			-1000	-400
	I_{OL} (mA)			20	4/8 (a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH} Supply current	$V_{CC} = \text{Max}, V_{IN} = 0V$						29		3.2	mA
I_{CCL} Supply current	$V_{CC} = \text{Max}, V_{IN} \geq 4.5V$						45		5.4	mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
						$C_L = 15pF$ $R_L = 280\Omega$		$C_L = 15pF$ $R_L = 2K\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1						5.5 6.0		15 15	ns ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc Characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54LS/74LS261

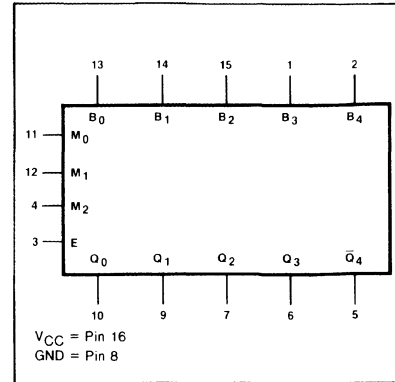
DESCRIPTION

The "261" is a Multiply Decoder circuit designed to be used in parallel multiplication applications. It performs binary multiplication in a two's-complement form, two bits at a time. This device may also be used in a parallel-serial multiplier requiring substantially fewer parts than parallel-parallel multiplication.

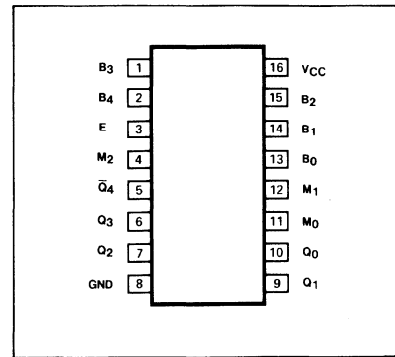
FEATURES

- Multiply 4-bits by 2-bits
- Two's complement multiplication
- Output latch for synchronous operation
- Expandable to n-bits

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS261N	
Ceramic DIP	N74LS261F	S54LS261F
Flatpak		S54LS261W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION	54/74	54S/74S	54LS/74LS
B ₀ -B ₁	Multiplicand inputs	I _{IH} (μA) I _{IL} (mA)		20 -0.4
M ₀ -M ₁	Multiplier inputs	I _{IH} (μA) I _{IL} (mA)		40 -0.8
M ₂	Most significant bit multiplier input	I _{IH} (μA) I _{IL} (mA)		20 -0.4
E	Latch Enable input	I _{IH} (μA) I _{IL} (mA)		20 -0.4
Q ₀ -Q ₃	Partial product outputs	I _{OH} (μA) I _{OL} (mA)		-400 4/8(a)
\bar{Q}_4	Most significant bit (active LOW) output	I _{OH} (μA) I _{OL} (mA)		-400 4/8(a)

NOTE

a The slashed numbers indicate different parametric values for Military / Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "261" is designed to perform binary multiplication in two's complement form, two bits at a time.

The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-Tree (summing) hardware requirements by a factor of two.

The outputs represent partial products in one's-complement notation generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

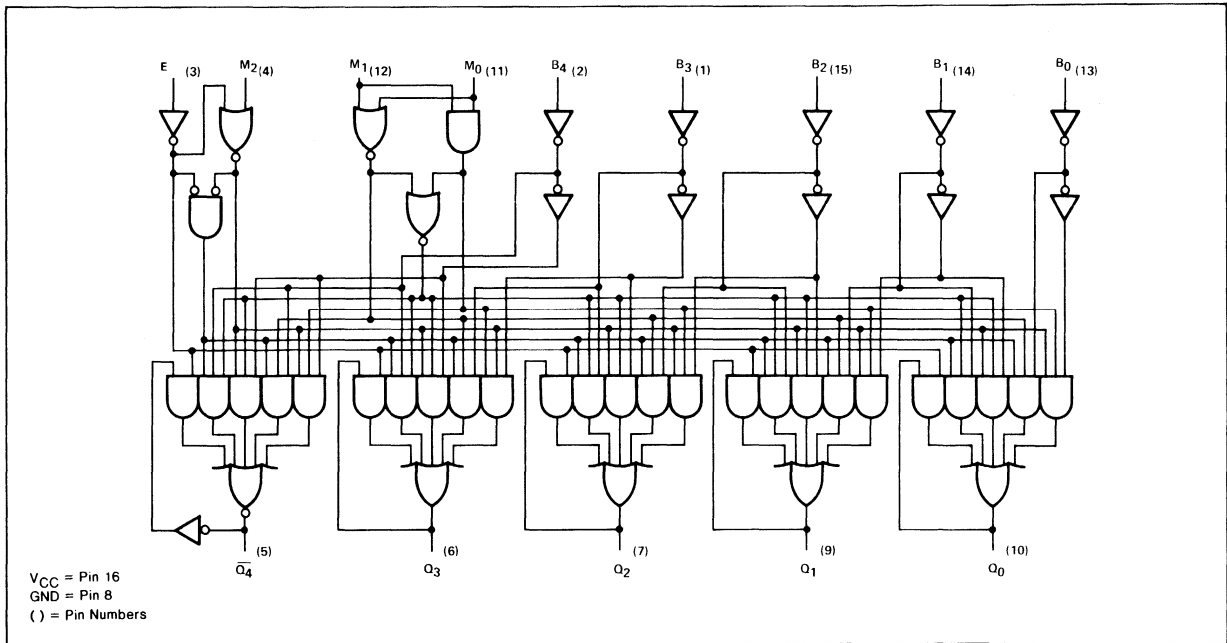
The leading (most significant) bit of the product is inverted for ease in extending the sign to left justify the partial-product bits.

FUNCTION TABLE

INPUTS				OUTPUTS				
E	M ₂	M ₁	M ₀	\bar{Q}_4	Q ₃	Q ₂	Q ₁	Q ₀
L	X	X	X	\bar{q}_4	q ₃	q ₂	q ₁	q ₀
H	L	L	L	H	L	L	L	L
H	L	L	H	\bar{B}_4	B ₄	B ₃	B ₂	B ₁
H	L	H	L	\bar{B}_4	B ₄	B ₃	B ₂	B ₁
H	L	H	H	\bar{B}_4	B ₃	B ₂	B ₁	B ₀
H	H	L	L	B ₄	B ₃	\bar{B}_2	\bar{B}_1	\bar{B}_0
H	H	L	H	B ₄	\bar{B}_4	\bar{B}_3	\bar{B}_2	\bar{B}_1
H	H	H	L	B ₄	B ₄	\bar{B}_3	\bar{B}_2	\bar{B}_1
H	H	H	H	H	L	L	L	L

H = HIGH voltage level
 L = LOW voltage level
 q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Enable transition.
 B_n = The logic level on the referenced multiplicand input.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
I _{CC}	Supply current	V _{CC} = Max,	Mil						38	mA
		V _{IN} = 0V	Com						40	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
								C _L = 15pF R _L = 2kΩ		
				Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation delay	Figure 1							35	ns
t _{PHL}	Enable to output								30	ns
t _{PLH}	Propagation delay	Figure 2 or 3							40	ns
t _{PHL}	M inputs to outputs								35	ns
t _{PLH}	Propagation delay	Figure 2 or 3							42	ns
t _{PHL}	B inputs to outputs								37	ns

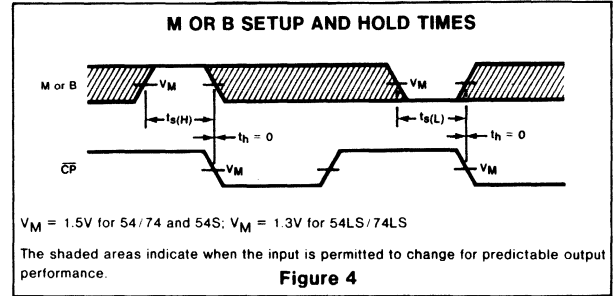
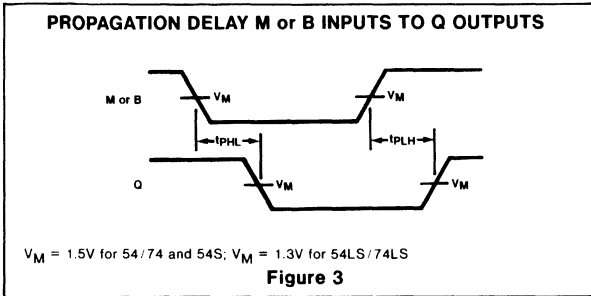
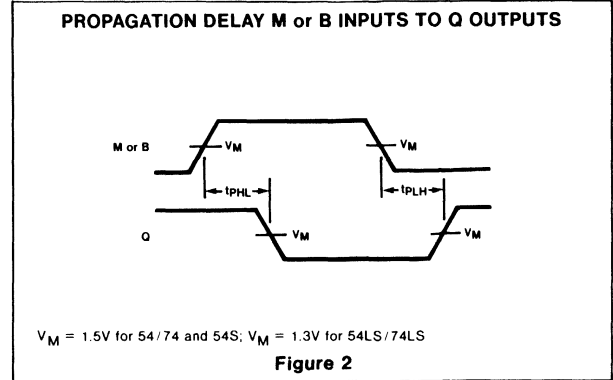
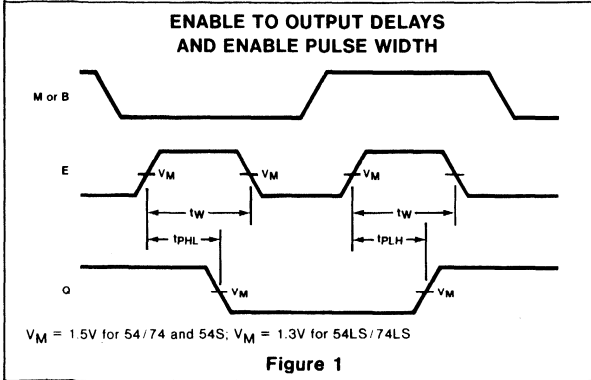
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

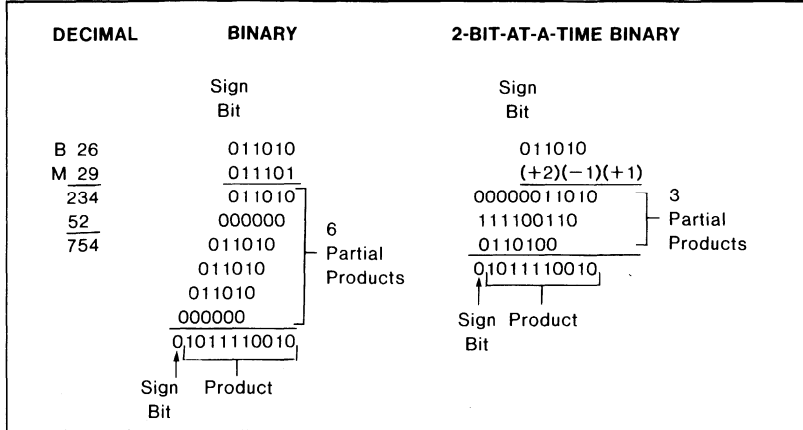
PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
t _w	Enable pulse width	Figure 1						25		ns
t _s	Setup time M input to Enable	Figure 4						17		ns
t _h	Hold time M input to Enable	Figure 4						0		ns
t _s	Setup time B input to Enable	Figure 4						15		ns
t _h	Hold time B input to Enable	Figure 4						0		ns

AC WAVEFORMS



TYPICAL APPLICATION DATA

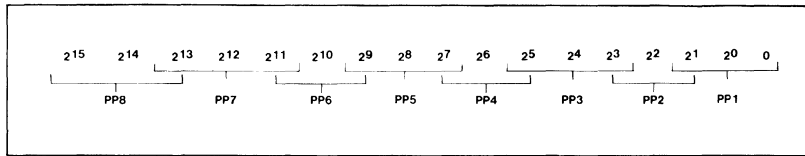
Multiplication of the numbers 26 (multiplcand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:



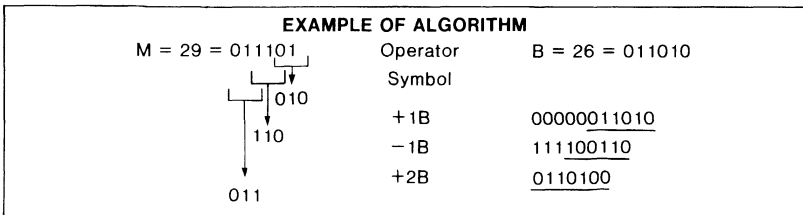
Two points should be noted in the 2-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer. A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.
2. Generate partial product (PPi) as shown in the following table:
3. Weight the partial products by indexing each two places left relative to the next-less-significant product.
4. Extend the most-significant bit of the partial product to the sign-bit place value of the final product.



MULTIPLIER BITS FROM STEP 1			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
2 ²ⁱ⁻¹	2 ²ⁱ⁻²	2 ²ⁱ⁻³		
0	0	0	0	Replace multiplicand by zero
0	0	1	+1B	Copy multiplicand
0	1	0	+1B	Copy multiplicand
0	1	1	+2B	Shift multiplicand left one bit
1	0	0	-2B	Shift two's complement of multiplicand left one bit
1	0	1	-1B	Replace multiplicand by two's complement
1	1	0	-1B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero



The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

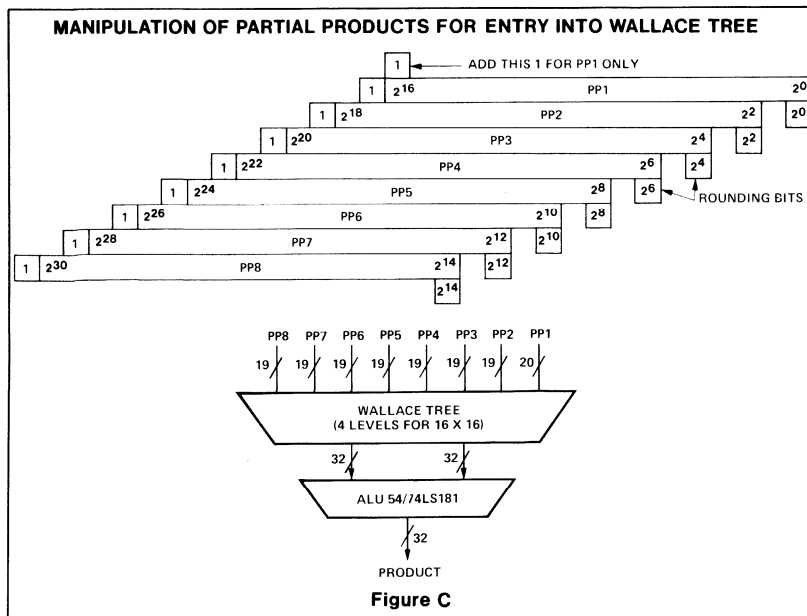
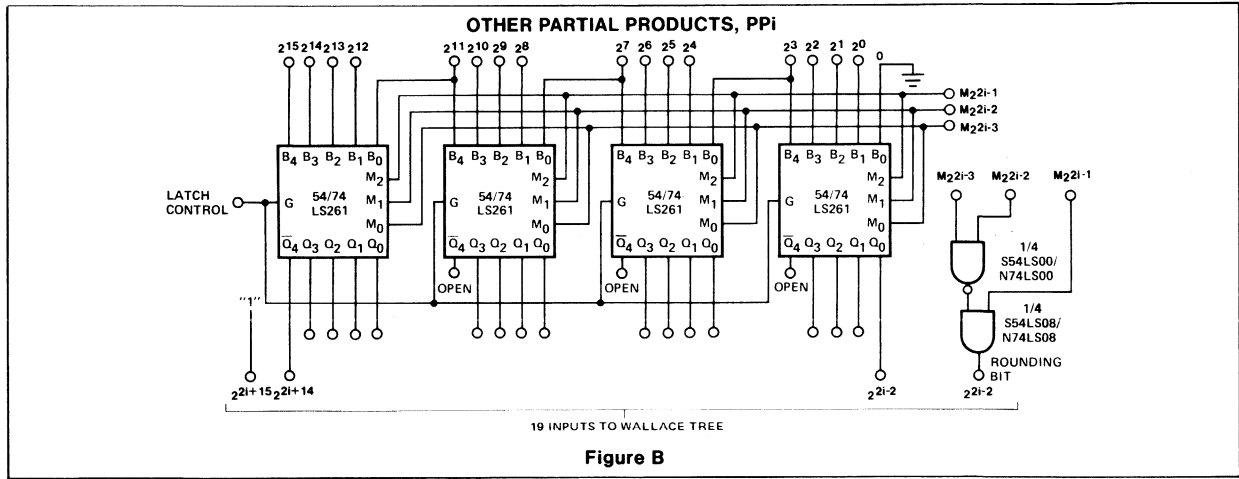
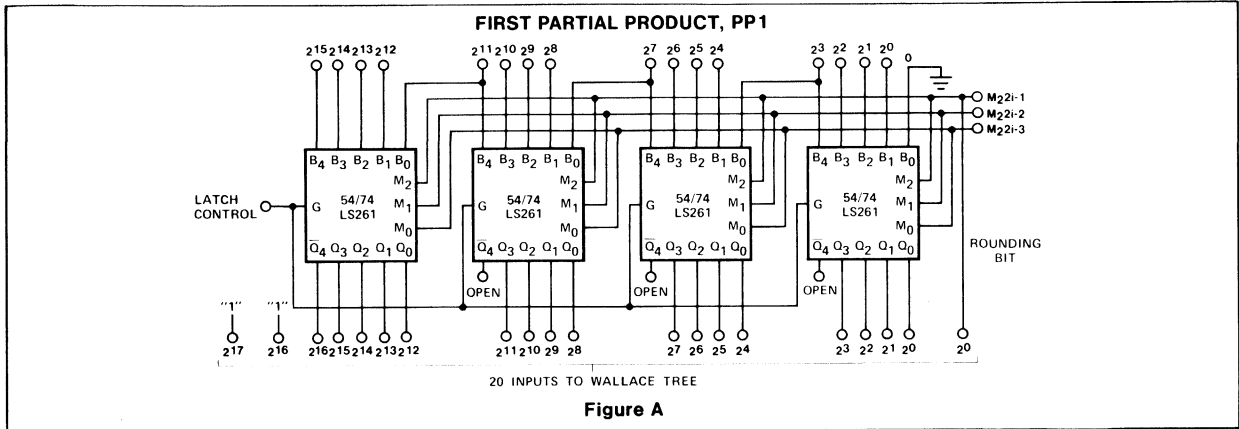
The 54/74LS261 generates partial products according to this algorithm with two exceptions:

1. The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.
2. The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2²¹+15 of each partial product and also in bit position 2¹⁶ of the first partial product (PP1).
3. In general, the 4x2 bit 54/74LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 54/74LS261s, m x n ÷ 16 54/74LS00s, and m x n ÷ 16

54/74LS08s. The size of the Wallace Tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

- 32 S54LS261/N74LS261
- 2 S54LS00/N74LS00
- 2 S54LS08/N74LS08
- 56 54H183/74H183*
- 7 S54LS181/N74LS181
- 2 S54LS182/N74LS182

* Not currently available from Signetics.



54LS/74LS266

PIN CONFIGURATION

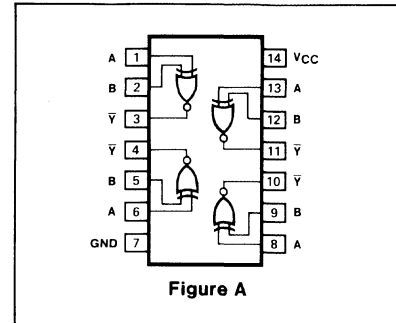


Figure A

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74LS266N	
Ceramic DIP	Fig. A	N74LS266F	S54LS266F
Flatpak	Fig. A		S54LS266W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)				20
	I_{IL} (mA)				-0.36
Outputs	I_{OH} (μA)				-400
	I_{OL} (mA)				4/8(a)

TRUTH TABLE

INPUTS		OUTPUT
A	B	\bar{Y}
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_A = 0V$ $V_B = 4.5V$								13	mA

AC CHARACTERISTICS: $T_A=25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} A or B to output	Waveform 1, other input LOW								30 30	ns ns
t_{PLH} Propagation delay t_{PHL} A or B to output	Waveform 2, other input HIGH								30 30	ns ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc Characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

74S273
54LS/74LS273

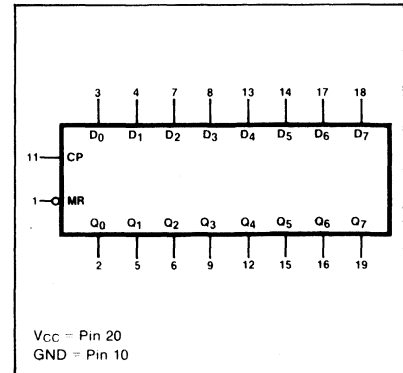
DESCRIPTION

The "273" is an Octal D Flip-Flop used primarily as an 8-bit positive-edge-triggered storage register. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the clock pulse. The Master Reset (\overline{MR}) input asynchronously clears all flip-flops when LOW.

FEATURES

- Ideal buffer for MOS Microprocessor or Memory
- Eight edge-triggered D flip-flops
- High speed Schottky version available
- Buffered common clock
- Buffered, asynchronous Master Reset
- Slim 20-Pin plastic and ceramic DIP packages
- See "377" for Clock Enable version
- See "373" for transparent latch version
- See "374" for 3-state version

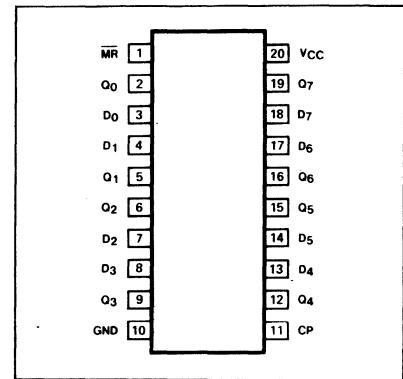
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	N74S273N	• N74LS273N		
Ceramic DIP	N74S273F	• N74LS273F		S54LS273F
Flatpak				

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
D ₀ - D ₇	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
\overline{MR}	Master Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
Q ₀ - Q ₇	Outputs	I_{OH} (μA) I_{OL} (mA)		-1000 20	-400 4/8(a)

NOTES

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "273" has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

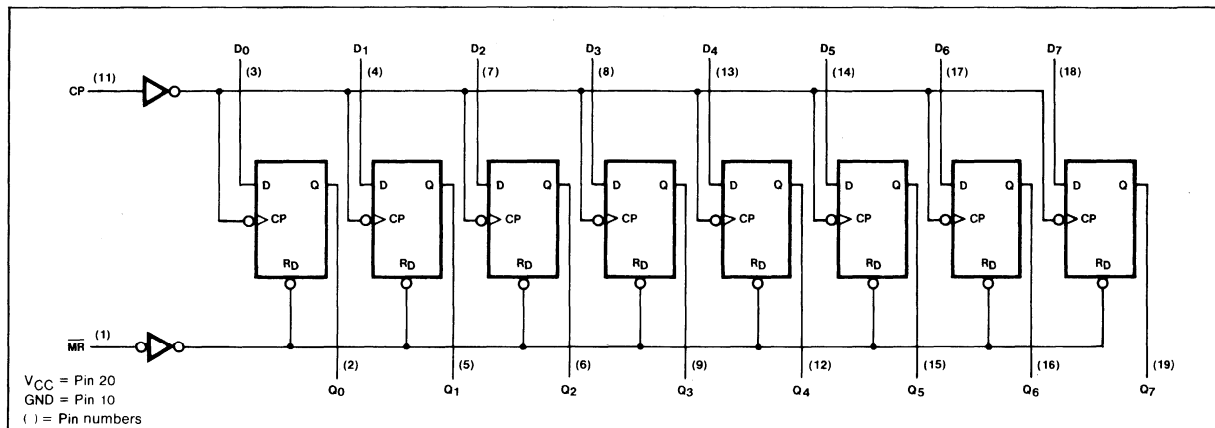
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	\overline{MR}	CP	D _n	Q _n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max				150		27	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 2KΩ		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1			75		30		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Figure 1				15 15		21 23	ns
t _{PHL} Propagation delay \overline{MR} to output	Figure 2				15		30	ns

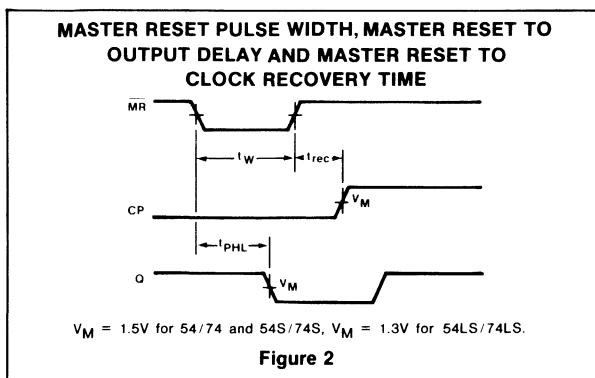
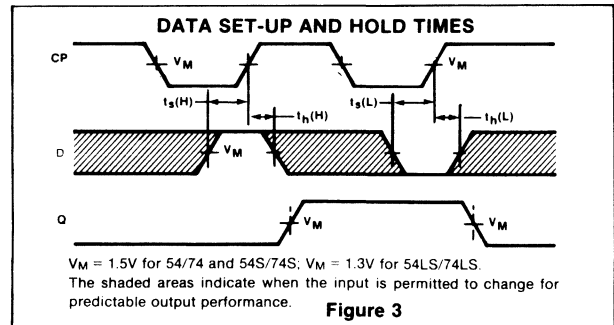
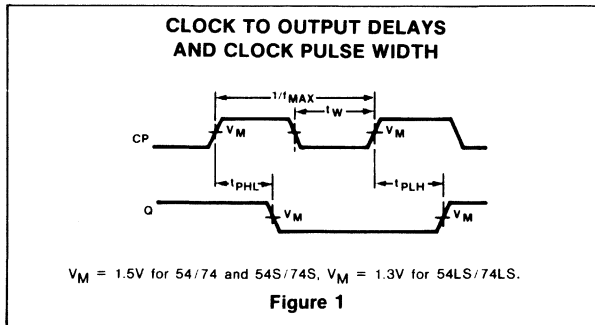
NOTE

b. For family dc characteristics, see inside front cover 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Figure 1			7.0		20		ns
t_W Master Reset pulse width	Figure 2			10		20		ns
$t_S(H)$ Setup time HIGH data to CP	Figure 3			5.0		15		ns
$t_H(H)$ Hold time HIGH data to CP	Figure 3			3.0		0		ns
$t_S(L)$ Setup time LOW data to CP	Figure 3			5.0		15		ns
$t_H(L)$ Hold time LOW data to CP	Figure 3			3.0		0		ns
t_{rec} Recovery time \overline{MR} to CP	Figure 2			5.0		15		ns

AC WAVEFORMS

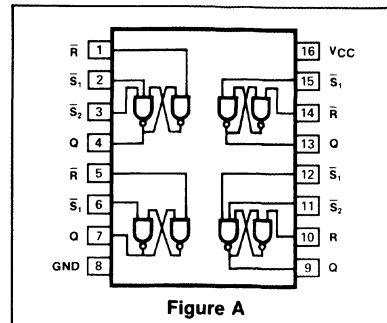


**54/74279
54LS/74LS279**

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N74279N	• N74LS279N		
Ceramic DIP	Fig. A	N74279F	• N74LS279F	S54279F	• S54LS279F
Flatpak	Fig. A			S54279W	• S54LS279W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.4
Outputs	I_{OH} (μA)	-800			-400
	I_{OL} (mA)	16			4/8 (a)

TRUTH TABLE

INPUTS			OUTPUT
\bar{S}_1	\bar{S}_2	R	Q
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No change

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
h = The output is HIGH as long as S_1 or S_2 is LOW.
If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise it follows the truth table.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_R = 0V$, $V_S = 4.5V$		30						7.0	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions.)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15pF$ $R_L = 400\Omega$						$C_L = 15pF$ $R_L = 2k\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Set to output			22 15						22 15	ns ns
t_{PHL} Propagation delay Reset to output			27						27	ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54S/74S280

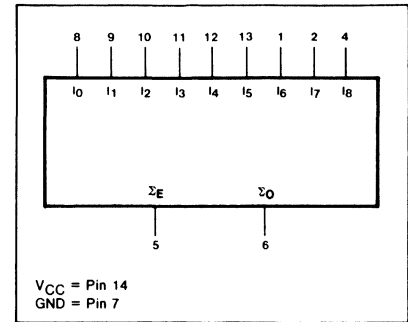
DESCRIPTION

The "280" is a 9-Bit Parity Generator / Checker with Odd and Even parity outputs to facilitate operation of either odd or even parity application. It is used for detecting errors in high speed data transmission and retrieval systems. Expansion is easily accomplished by serial or parallel cascading of any number of stages.

FEATURES

- Buffered inputs - one normalized load
- Word-length easily expanded by cascading
- Similar pin configuration to "180" for easy system up-grading

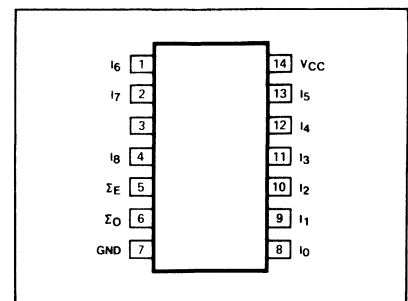
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74S280N	
Ceramic DIP	N74S280F	S54S280F
Flatpak		S54S280W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
I ₀ -I ₈	Data inputs	I _{IH} (μA) I _{IL} (mA)		50 -2.0	
Σ _E	Even parity output	I _{OH} (μA) I _{OL} (mA)		-1000 20	
Σ _O	Odd parity output	I _{OH} (μA) I _{OL} (mA)		-1000 20	

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil			99			mA
		Com			105			mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

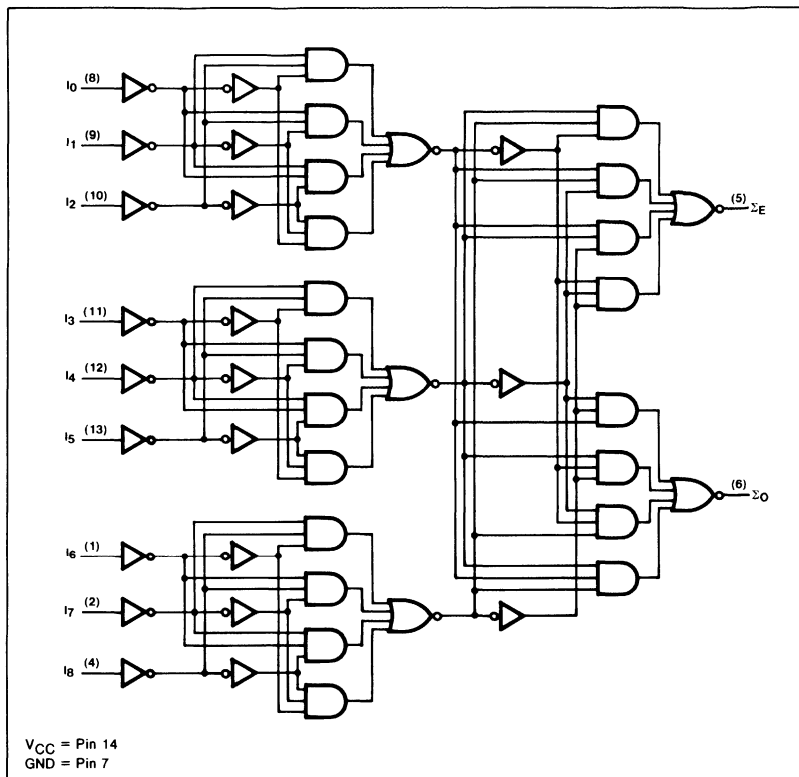
FUNCTIONAL DESCRIPTION

The "280" is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to nine bits.

The Even parity output (Σ_E) is HIGH when an even number of data inputs (I_0-I_8) are HIGH. The Odd parity output (Σ_O) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E) of up to nine parallel devices to the data inputs of the final stage. This expansion scheme allows an 81 bit data word to be checked in less than 40ns with the "S280".

LOGIC DIAGRAM



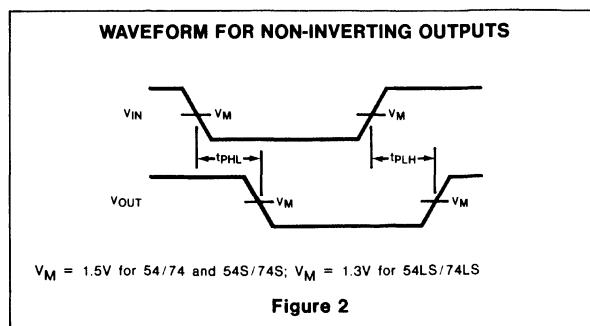
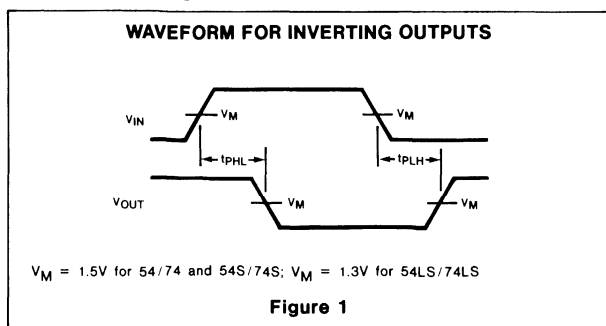
TRUTH TABLE

INPUTS	OUTPUTS	
Number of HIGH data inputs (I_0-I_8)	Σ_E	Σ_O
Even	H	L
Odd	L	H

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L=15\text{pF}$ $R_L=280\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Figures 1 & 2				21			ns
t_{PHL} Data to Even output					18			ns
t_{PLH} Propagation delay	Figures 1 & 2				21			ns
t_{PHL} Data to Odd output					18			ns

AC WAVEFORMS



54LS/74LS283

DESCRIPTION

The "283" is a high speed 4-bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1 - A_4 , B_1 - B_4) and a Carry input (C_{IN}). The sum of the two 4-bit words is combined with the carry input and presented at the four Sum outputs (Σ_1 - Σ_4) and the Carry output (C_{OUT}). It operates with either HIGH or LOW operands (positive or negative logic).

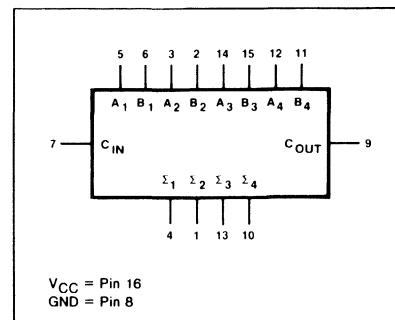
FEATURES

- High speed 4-bit binary addition
- Cascadeable in 4-bit increments
- Fast internal carry lookahead
- Power pins located on corner pins

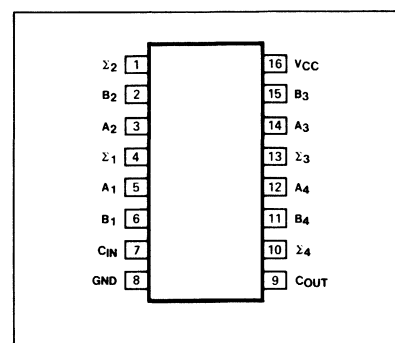
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS283N	
Ceramic DIP	N74LS283F	S54LS283F
Flatpak		S54LS283W

LOGIC SYMBOL



PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
A_1 - A_4	Operand A inputs	I_{IH} (μA) I_{IL} (mA)			40 -0.8
B_1 - B_4	Operand B inputs	I_{IH} (μA) I_{IL} (mA)			40 -0.8
C_{IN}	Carry input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Σ_1 - Σ_4	Sum outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)
C_{OUT}	Carry output	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "283" adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs (Σ_1 - Σ_4) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2 \Sigma_2 + 4 \Sigma_3 + 8 \Sigma_4 + 16C_{OUT}$$

Where (+) = plus

Due to the symmetry of the binary add function the "283" can be used with either all active HIGH operands (positive logic) or with all active LOW operands (negative logic)—see Table "A". With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN} , A_1 , B_1 can arbitrarily be assigned to pins 5, 6, 7 etc.

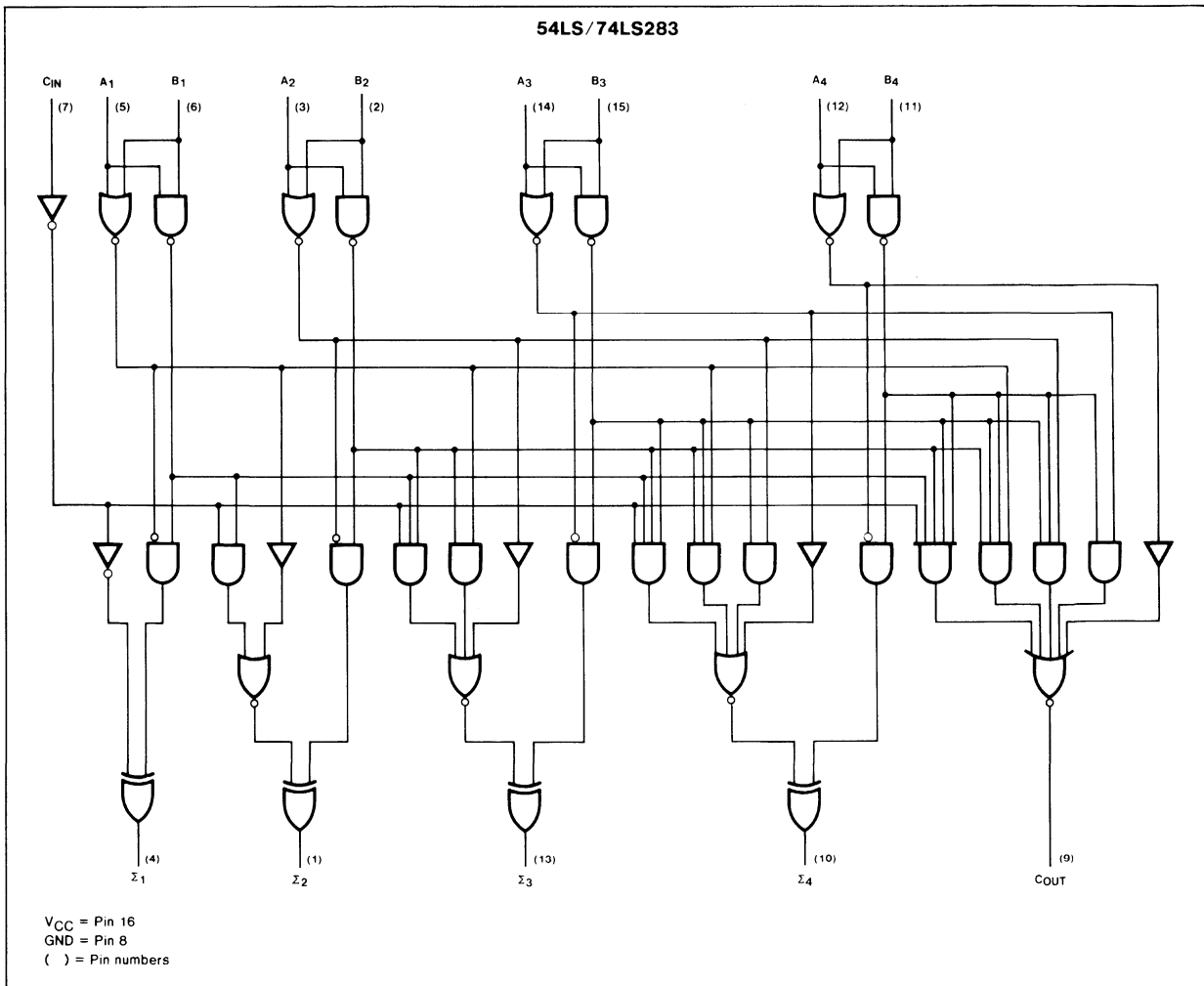
PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10 + 9 = 19)

(carry + 5 + 6 = 12)

Table A

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT		
		Min	Max	Min	Max	Min	Max			
I _{OS}	Short circuit current	V _{CC} = Max						-15	-100	mA
I _{CC}	Supply current	V _{CC} = Max		V _{IN} = 0V				39		mA
				V _{IN} = 4.5V				34		mA

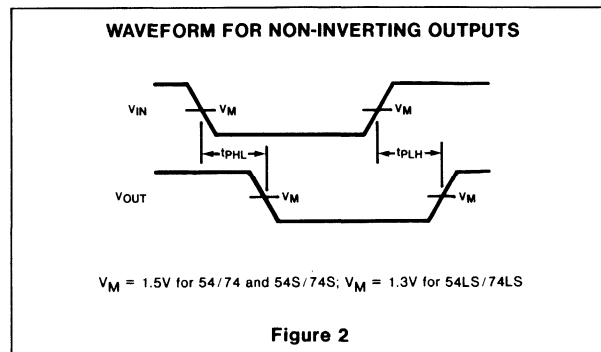
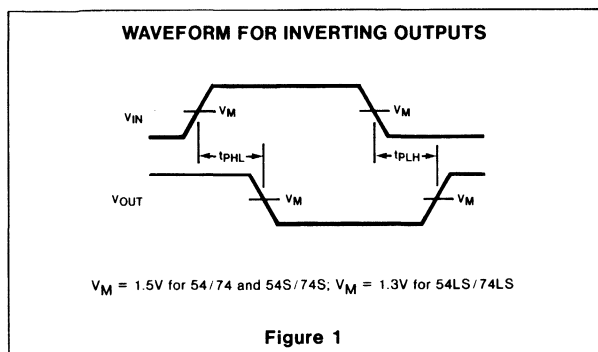
AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						C _L = 15pF R _L = 2kΩ		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay C _{IN} to Σ ₁	Figures 1 & 2					24 24	ns ns
t _{PLH} t _{PHL}	Propagation delay C _{IN} to Σ ₂	Figures 1 & 2					24 24	ns ns
t _{PLH} t _{PHL}	Propagation delay C _{IN} to Σ ₃	Figures 1 & 2					24 24	ns ns
t _{PLH} t _{PHL}	Propagation delay C _{IN} to Σ ₄	Figures 1 & 2					24 24	ns ns
t _{PLH} t _{PHL}	Propagation delay A _i or B _i to Σ _i	Figures 1 & 2					24 24	ns ns
t _{PLH} t _{PHL}	Propagation delay C _{IN} to C _{OUT}	Figure 2					17 17	ns ns
t _{PLH} t _{PHL}	Propagation delay A _i or B _i to C _{OUT}	Figures 1 & 2					17 17	ns ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54S/74S289 (3101A)
54LS/74LS289 (Preliminary data)

See Signetics Memory Data Manual for
 3101A Specifications

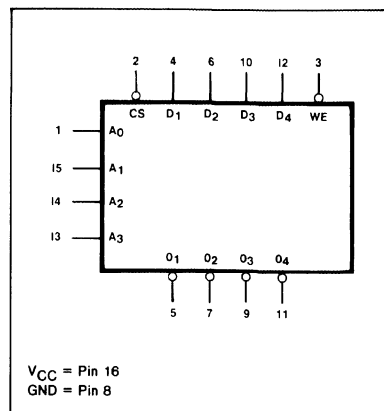
DESCRIPTION

The "289" is a 64-Bit high-speed Read/Write Random Access Memory for use as a "scratch pad" memory with non-destructive read-out. Memory cells are organized in a matrix to provide 16 words of four bits each. Four buffered Address (A₀-A₃) inputs are decoded on the chip to select one of the 16 memory words for read or write operations. Four buffered data inputs (D₁-D₄) and four open-collector data outputs are provided for versatile memory expansion. Data at the outputs is inverted from the data which was written into the memory. When the write mode is selected the outputs are HIGH.

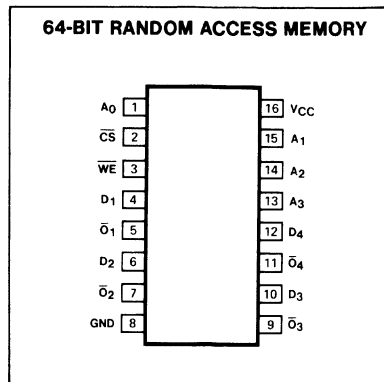
FEATURES

- 16-words by 4-bit memory
- On-chip address decoding
- Inverted data at outputs
- Open collector outputs for easy expansion

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS289N	
Ceramic DIP	N74LS289F	S54LS289F
Flatpak		S54LS289W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	3101A	54LS/74LS
A ₀ -A ₃	Address inputs	I _H (μA) I _L (μA)		25/10 (a) -150/-100 (a)	20 -100
\overline{CS}	Chip Select (active LOW) enable input	I _H (μA) I _L (μA)		25/10 (a) -150/-100 (a)	20 -400
\overline{WE}	Write Enable (active LOW) input	I _H (μA) I _L (μA)		25/10 (a) -150/-100 (a)	20 -400
D ₁ -D ₄	Data inputs	I _H (μA) I _L (μA)		25/10 (a) -150/-100 (a)	20 -400
\overline{O}_1 - \overline{O}_4	Data (inverting) outputs	I _{OH} (μA) I _{OL} (mA)		+100 16	+100 12/24 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "289" is a high-speed array of 64 memory cells organized as 16 words of four bits each. A one-of-sixteen address decoder selects a single word which is specified by the four Address inputs (A₀-A₃). A READ operation is initiated after the address lines are stable when the Write Enable (\overline{WE}) input is HIGH and the Chip Select-Memory Enable (\overline{CS}) input is LOW. Data is read at the outputs inverted from the data which was written into the memory.

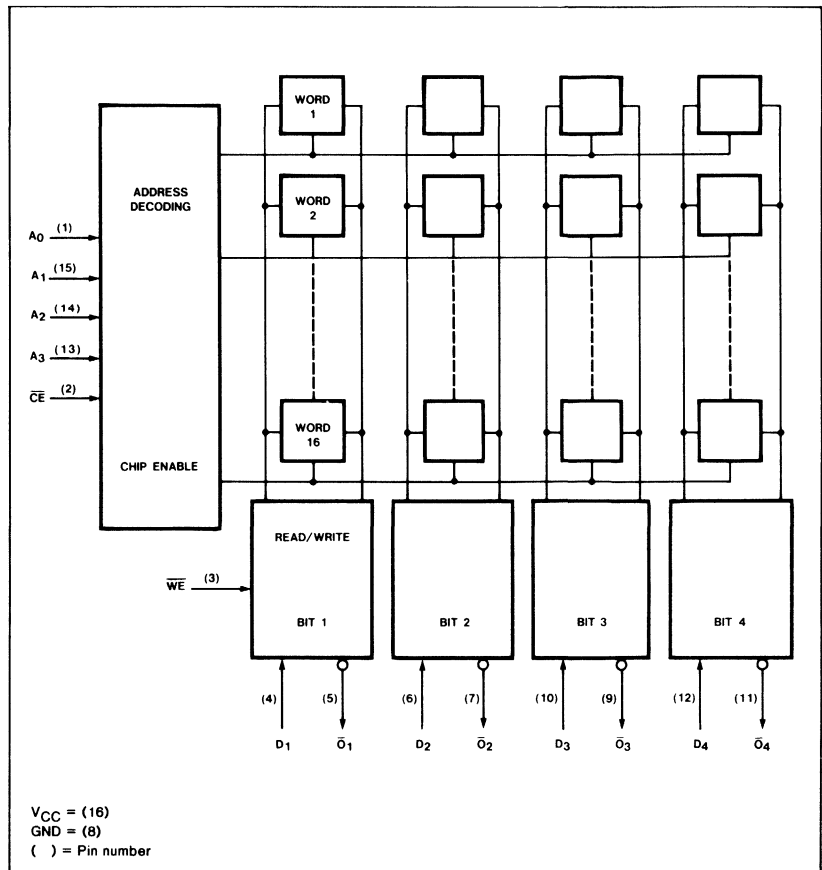
A WRITE operation requires that the \overline{WE} and \overline{CS} inputs be LOW. The address inputs must be stable during the WRITE mode for predictable operation. When the write mode is selected the outputs are HIGH. The selected memory cells are transparent to changes in the data during the WRITE mode. Therefore, data must be stable one setup time before the LOW-to-HIGH transition of \overline{CE} or \overline{WE} .

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CS	WE	D _n	\overline{O}_n
Write—Disable Outputs	L	L	L	H
	L	L	H	H
Read	L	H	X	$\overline{\text{Data}}$
Store-Disable Outputs	H	X	X	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 $\overline{\text{Data}}$ = Read complement of data from addressed word location

BLOCK DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min I _{OL} = 12mA						0.4	V
							0.5 (c)	V
I _{CC} Supply current	V _{CC} = Max	Mil					45	mA
		Com					37	mA

NOTES

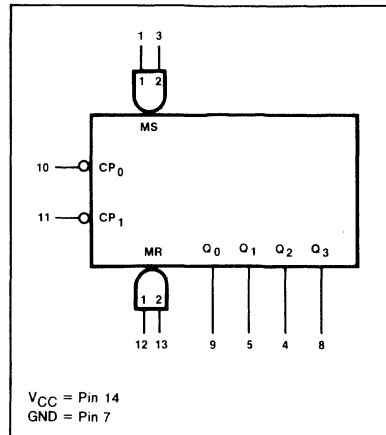
- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial Range only.

54LS/74LS290

LOGIC SYMBOL

DESCRIPTION

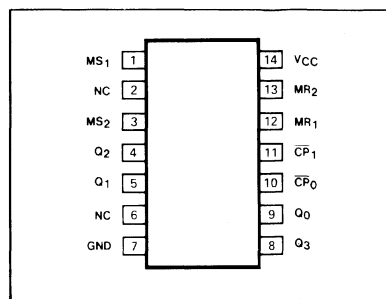
The "290" is a high-speed 4-bit ripple type decade counter divided into two sections. The counter has a divide-by-two section and a divide-by-five section which are triggered by HIGH-to-LOW transitions on the clock inputs. Either section can be used separately or tied together (Q to \overline{CP}) to form a BCD or a bi-quinary counter. The counter has a 2-input gated Master Reset (Clear) and also a 2-input gated Master Set (Preset 9).



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PIN CONFIGURATION

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	N74LS290N	
Ceramic DIP	N74LS290F	S54LS290F
Flatpak		S54LS290W



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}_0	Clock (active LOW going edge) input to $\div 2$ section	I_{IH} (μA) I_{IL} (mA)			40 -2.4
\overline{CP}_1	Clock (active LOW going edge) input to $\div 5$ section	I_{IH} (μA) I_{IL} (mA)			80 -3.2
MR ₁ , MR ₂	Master Reset (Clear) inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
MS ₁ , MS ₂	Master Set (Preset-9) inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q ₀	Output from $\div 2$ section	I_{OH} (μA) I_{OL} (mA)			-400 4/8 ^(a)
Q ₁ , Q ₂ , Q ₃	Outputs from $\div 5$ section	I_{OH} (μA) I_{OL} (mA)			-400 4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "290" is a 4-bit ripple type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output is designed and specified to drive the rate fan-out plus the CP₁ input of the device.

A gated AND asynchronous Master Reset (MR₁ • MR₂) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set (MS₁ • MS₂) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) Counter the CP₁ input must be externally connected to the Q₀ output. The CP₀ input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the Q₃ output must be connected externally to the CP₀ input. The input count is then applied to the CP₁ input and a divide-by-ten square wave is obtained at output Q₀. To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (CP₀ as the input and Q₀ as the output). The CP₁ input is used to obtain divide-by-five operation at the Q₃ output.

MODE SELECTION—TRUTH TABLE

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X				Count
X	L	X	L				Count
L	X	X	L				Count
X	L	L	X				Count

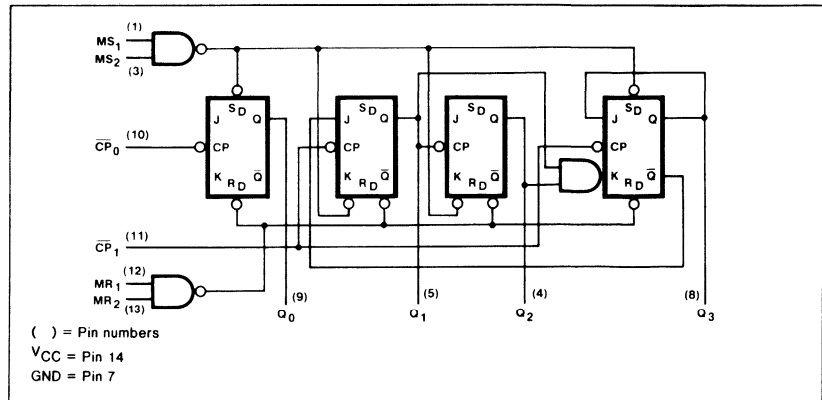
H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE—TRUTH TABLE

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q₀ connected to input CP₁.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil					15	mA
		Com					15	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

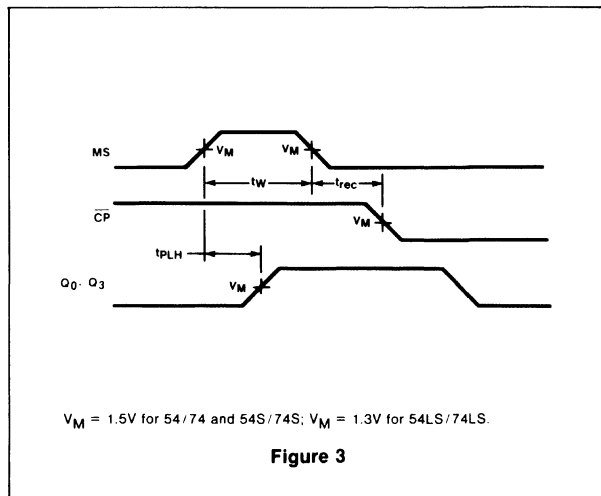
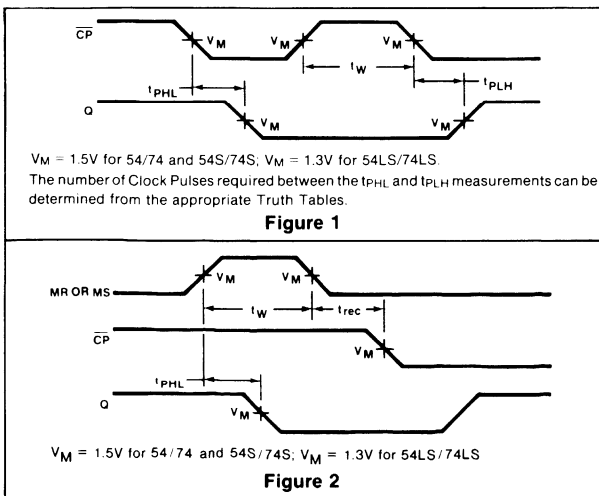
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	$\overline{\text{CP}}_0$ Input count frequency					30		MHz
f_{MAX}	$\overline{\text{CP}}_1$ Input count frequency					15		MHz
t_{PLH}	Propagation delay						16	ns
t_{PHL}	$\overline{\text{CP}}_0$ Input to Q_0 Output						18	ns
t_{PLH}	Propagation delay						16	ns
t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_1 Output						21	ns
t_{PLH}	Propagation delay						32	ns
t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_2 Output						35	ns
t_{PLH}	Propagation delay						32	ns
t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_3 Output						35	ns
t_{PLH}	Propagation delay						48	ns
t_{PHL}	$\overline{\text{CP}}_0$ Input to Q_3 Output						50	ns
t_{PHL}	MR Input to any Output						40	ns
t_{PLH}	MS Input to Q_0 and Q_3 Outputs						30	ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs						40	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w	$\overline{\text{CP}}_0$ Pulse width					15		ns
t_w	$\overline{\text{CP}}_1$ Pulse width					30		ns
t_w	MR Pulse width					15		ns
t_{rec}	Recovery time MR to $\overline{\text{CP}}$					25		ns
t_{rec}	Recovery time MS to $\overline{\text{CP}}$					25		ns

AC WAVEFORMS

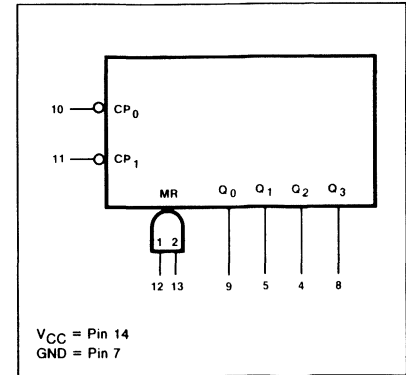


54LS/74LS293

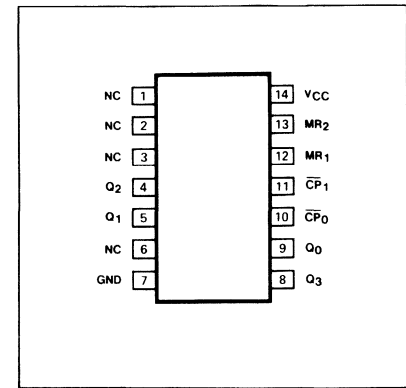
DESCRIPTION

The "293" is a high-speed 4-bit ripple type counter divided into two sections. The counter has a divide-by-two section and a divide-by-eight section which are triggered by HIGH-to-LOW transitions on the clock inputs. Either section can be used separately or tied together (Q_0 to \overline{CP}_1) to form a modulo-16 counter. The counter has a 2-input gated Master Reset (Clear).

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	N74LS293N	
Ceramic DIP	N74LS293F	S54LS293F
Flatpak		S54LS293W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION	54/74	54S/74S	54LS/74LS
\overline{CP}_0	Clock (Active LOW going edge) input (to $\div 2$ Section)	I_{IH} (μA) I_{IL} (mA)		40 -2.4
\overline{CP}_1	Clock (Active LOW going edge) input (to $\div 8$ Section)	I_{IH} (μA) I_{IL} (mA)		40 -1.6
MR ₁ , MR ₂	Master Reset (Clear) inputs	I_{IH} (μA) I_{IL} (mA)		20 -0.4
Q ₀	Output from $\div 2$ section	I_{OH} (μA) I_{OL} (mA)		-400 4/8 ^(a)
Q ₁ , Q ₂ , Q ₃	Outputs from $\div 8$ section	I_{OH} (μA) I_{OL} (mA)		-400 4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "293" is a 4-bit ripple type Binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output is designed and specified to drive the rated fan-out plus the \overline{CP}_1 input of the device.

A gated AND asynchronous Master Reset (MR₁ MR₂) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q₀ must be connected externally to input \overline{CP}_1 . The input count pulses are applied to input \overline{CP}_0 . Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q₀, Q₁, Q₂ and Q₃ outputs as shown in the truth table. As a 3-bit ripple counter the input count pulses are applied to input \overline{CP}_1 . Simultaneous frequency divisions of 2, 4 and 8 are available at the Q₁, Q₂ and Q₃ outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H		Count		
H	L		Count		
L	L		Count		

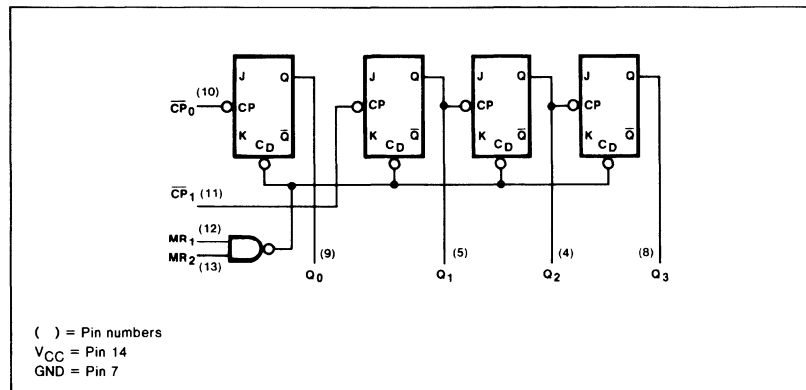
H = HIGH voltage level
L = LOW voltage level
X = Don't care

TRUTH TABLE

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q₀ connected to Input \overline{CP}_1 .

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max	Mil					15	mA
		Com					15	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

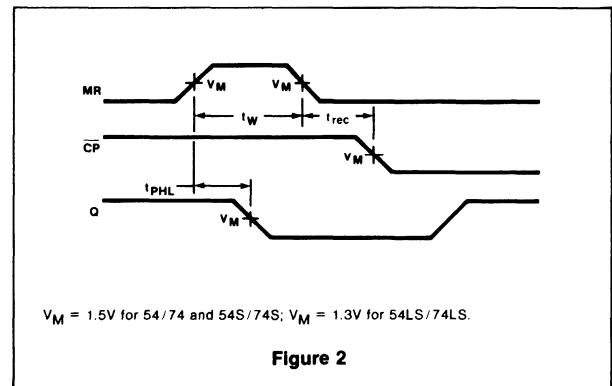
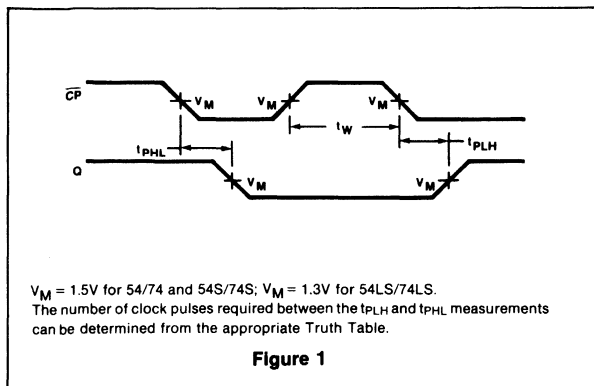
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{ pF}$ $R_L = 2\text{ k}\Omega$						
		Min	Max	Min	Max	Min	Max	
f_{MAX}	\overline{CP}_0 Input count frequency					32		MHz
f_{MAX}	\overline{CP}_1 Input count frequency					16		MHz
t_{PLH}	Propagation delay						16	ns
t_{PHL}	\overline{CP}_0 input to Q_0 output						18	ns
t_{PLH}	Propagation delay						16	ns
t_{PHL}	\overline{CP}_1 input to Q_1 output						21	ns
t_{PLH}	Propagation delay						32	ns
t_{PHL}	\overline{CP}_1 input to Q_2 output						35	ns
t_{PLH}	Propagation delay						51	ns
t_{PHL}	\overline{CP}_1 input to Q_3 output						51	ns
t_{PLH}	Propagation delay						70	ns
t_{PHL}	\overline{CP}_0 input to Q_3 output						70	ns
t_{PHL}	MR Input to any output						40	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w	\overline{CP}_0 Pulse width					15		ns
t_w	\overline{CP}_1 Pulse width					30		ns
t_w	MR Pulse width					15		ns
t_{rec}	Recovery time MR to \overline{CP}					25		ns

AC WAVEFORMS



54LS/74LS295B

DESCRIPTION

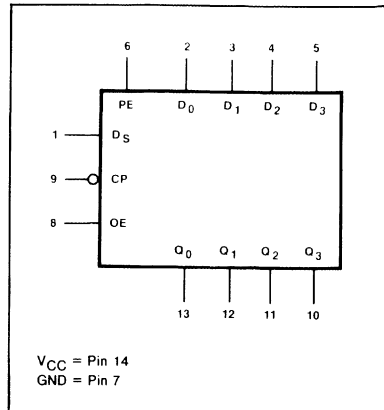
The "295" is a 4-Bit Shift Register with serial and parallel synchronous operating modes and independent 3-state output buffers. The active HIGH Parallel Enable (PE) input determines the parallel load or shift right operating modes. The PE and data inputs are edge-triggered, responding only to the HIGH-to-LOW transition of the Clock (\overline{CP}) input.

The 3-state output buffers are controlled by an active HIGH Output Enable (OE) input. A LOW on the OE input forces all four outputs to the high impedance "off" state. When OE is HIGH the data in the register appears at the outputs.

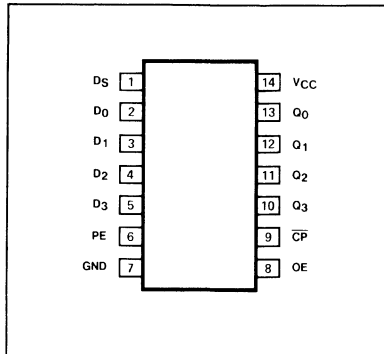
FEATURES

- 4-Bit parallel load shift register
- Independent 3-state buffer outputs
- See "395" for serial expansion and Master Reset version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS295BN	
Ceramic DIP	N74LS295BF	S54LS295BF
Flatpak		S54LS295BW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}	Clock (active LOW going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D ₀ -D ₃	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D _S	Serial Data input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
PE	Parallel Enable input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
OE	Output Enable input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q ₀ -Q ₃	3-State outputs	I_{OH} (mA) I_{OL} (mA)			-1 / -2.6 ^(a) 12/24 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "295" is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs (D₀-D₃) into the register synchronous with the HIGH-to-LOW transition of the Clock input (CP). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q₀ flip-flop, and the data in the register is shifted one bit to the right in the direction (Q₀→Q₁→Q₂→Q₃) synchronous with the negative transition of the clock. The PE and data inputs are fully edge triggered and must be stable only one setup time prior to the HIGH-to-LOW transition of the Clock.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads. The active HIGH Output Enable (OE) controls all four 3-state buffers independent of the register operation. When OE is HIGH the data in the register appears at the outputs. When OE is LOW the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

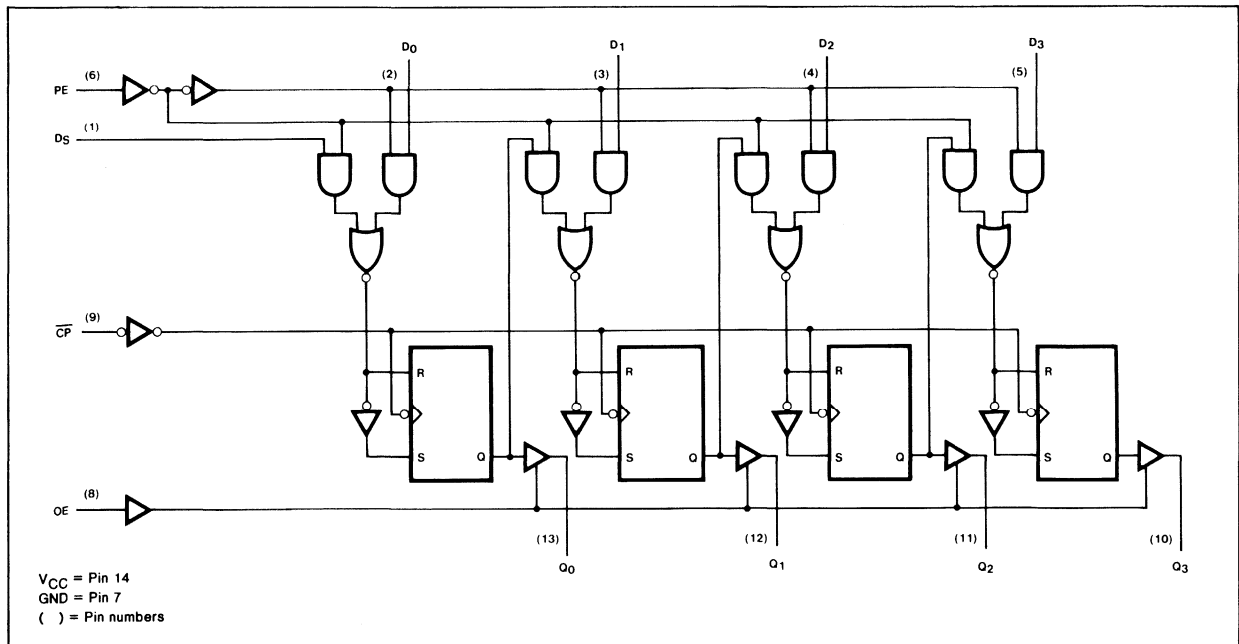
MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS				REGISTER OUTPUTS			
	CP	PE	D _S	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Parallel Load	↓	l	l	X	L	q ₀	q ₁	q ₂
	↓	l	h	X	H	q ₀	q ₁	q ₂
Shift right	↓	h	X	l	L	L	L	L
	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	OE	Q _n (Register)	Q ₀ , Q ₁ , Q ₂ , Q ₃
Read	H	L	L
	H	H	H
Disabled	L	X	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition
 q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition
 X = Don't care
 (Z) = High impedance "off" state
 ↓ = HIGH-to-LOW clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = Min, V _{OE} = V _{IH} I _{OH} = See Fan Out Table					2.4		V
V _{OL} Output LOW voltage	V _{CC} = Min, I _{OL} = 12mA						0.4	V
	V _{OE} = V _{IH} , I _{OL} = 24mA						0.5(c)	V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V					-30	-100	mA
I _{CC} Supply current	V _{CC} = Max						29	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 45pF R _L = 667Ω						
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1					30		MHz
t _{PLH} Propagation delay	Figure 1						23	ns
t _{PHL} Clock to output							30	ns
t _{PZH} Enable time to HIGH level	Figure 2						26	ns
t _{PZL} Enable time to LOW level	Figure 3						30	ns
t _{PHZ} Disable time from HIGH level	Figure 2						37	ns
	Figure 2, C _L = 5pF(d)						20	ns
t _{PLZ} Disable time from LOW level	Figure 3						25	ns
	Figure 3, C _L = 5pF(d)						20	ns

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Clock pulse width	Figure 1					25		ns
t _s Setup time Data to clock	Figure 4					10		ns
t _h Hold time Data to clock	Figure 4					5.0		ns
t _s Setup time PE to clock	Figure 4					20		ns
t _h Hold time PE to clock	Figure 4					10		ns

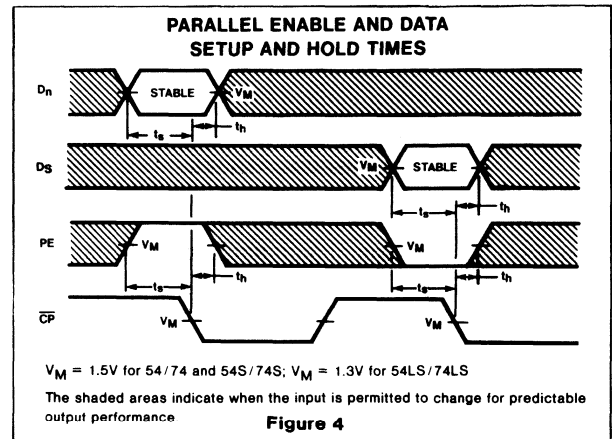
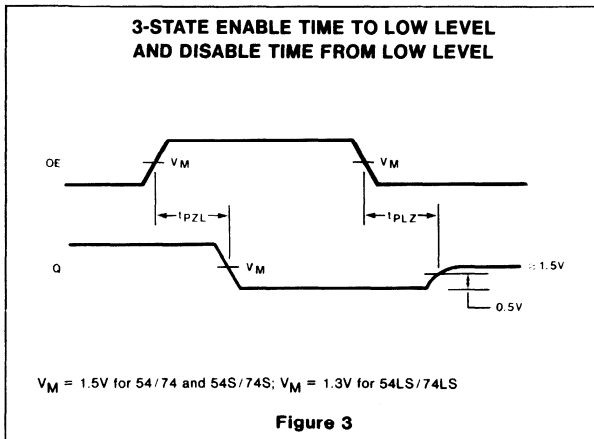
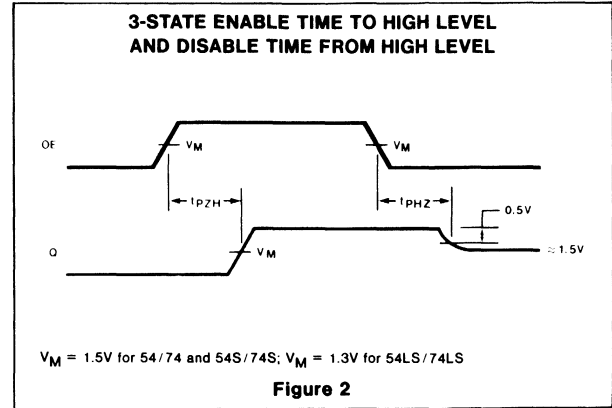
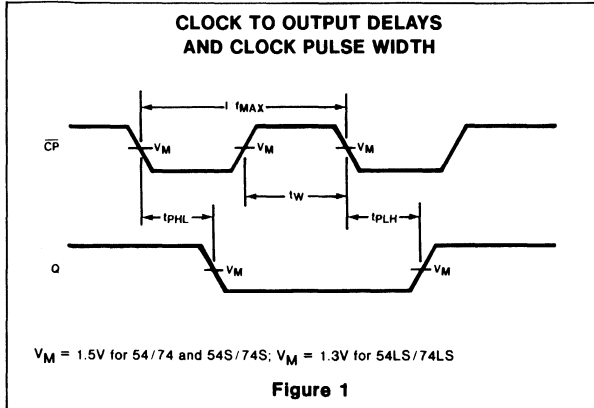
NOTES

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

c. This parameter for Commercial Range only.

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC WAVEFORMS



**54/74298
54LS/74LS298**

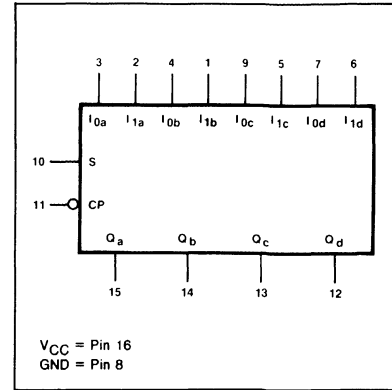
DESCRIPTION

The "298" is a Quad 2-Port Register which combines the functions of a quad 2-input multiplexer and a 4-bit negative edge triggered register. The state of the common Select input (S) determines the source of the data loaded into the register synchronous with the HIGH-to-LOW Clock (\overline{CP}) transition.

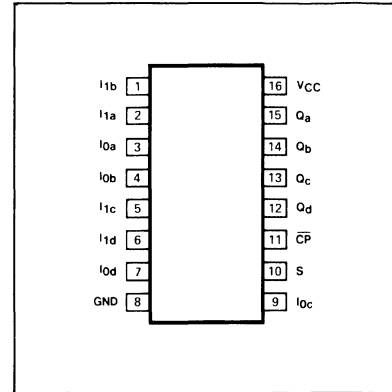
FEATURES

- Fully synchronous operation
- Select from two data sources
- Buffered, negative edge triggered clock
- See "398" and "399" for positive edge triggered versions

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	V _{CC} =5V ± 5%; T _A =0°C to +70°C		V _{CC} =5V ± 10%; T _A =-55°C to +125°C	
Plastic DIP	N74298N	• N74LS298N		
Ceramic DIP	N74298F	• N74LS298F	S54298F	• S54LS298F
Flatpak			S54298W	• S54LS298W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}	Clock (active LOW going edge) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
S	Select input	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
I _{0a} -I _{0d}	Data inputs from Source 0	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
I _{1a} -I _{1d}	Data inputs from Source 1	I _{IH} (μA) I _{IL} (mA)	40 -1.6		20 -0.4
Q _a -Q _d	Register outputs	I _{OH} (μA) I _{OL} (mA)	-800 16		-400 4/8 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

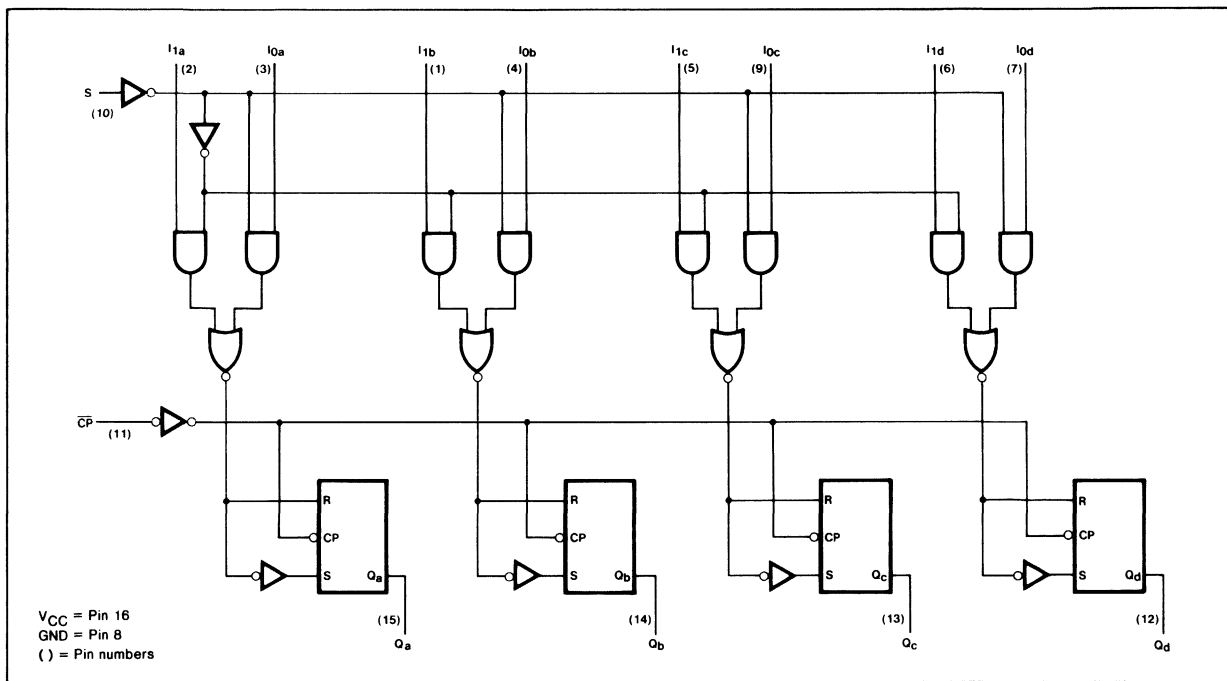
This device is a high-speed Quad 2-Port Register. It selects four bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input (CP). The 4-bit output register is fully edge-triggered. The Data inputs (I₀ & I₁) and Select input (S) must be stable only one set-up time prior to the HIGH-to-LOW transition of the clock for predictable operation.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	CP	S	I ₀	I ₁	Q _n
Load Source "0"	↓	l	l	X	L
Load Source "0"	↓	l	h	X	H
Load Source "1"	↓	h	X	l	L
Load Source "1"	↓	h	X	h	H

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition
 X = Don't care
 ↓ = HIGH-to-LOW clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max		65				21	mA

NOTE

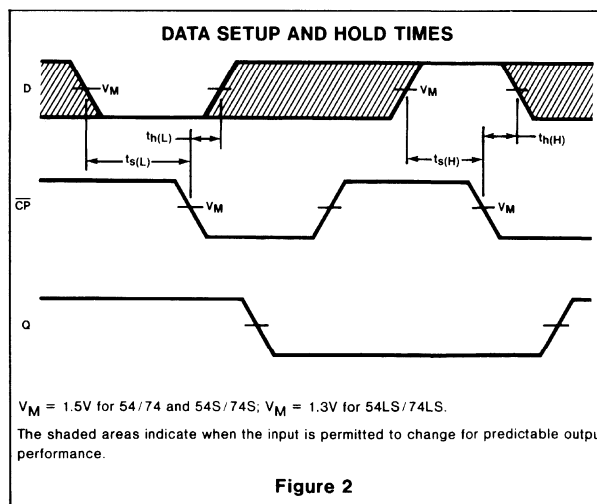
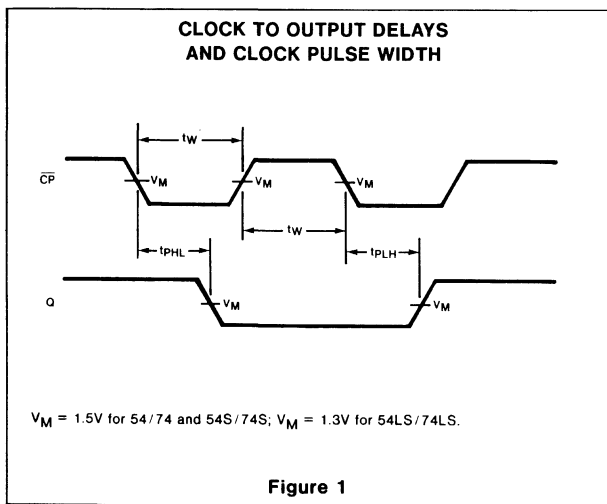
b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$				$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Figure 1		27				27	ns
t_{PHL} Clock to output			32				32	ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W Clock pulse width	Figure 1	20				20		ns
t_s Setup time Data to Clock	Figure 2	15				15		ns
t_h Hold time Data to Clock	Figure 2	5				5		ns
t_s Setup time Select to Clock	Figure 2	25				25		ns
t_h Hold time Select to Clock	Figure 2	0				0		ns



54LS/74LS299

DESCRIPTION

The "299" is an 8-Bit Bidirectional Universal Shift/Storage Register with a 3-state bidirectional Input/Output port. The register has four operating modes: shift right, shift left, parallel load, and hold (do nothing). The register has serial inputs and outputs for bidirectional cascading without interfering with the 3-state I/O port operation.

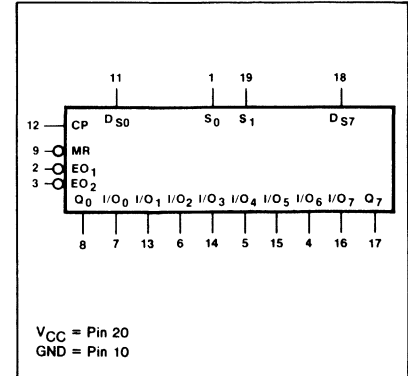
Parallel data is loaded into and read from the register through a 3-state I/O port controlled by two Output Enable (\overline{OE}) inputs and the Select inputs. The 3-state buffer outputs can drive heavily loaded buses, but present a light load to the bus when disabled or loading data.

The Master Reset overrides the clock and all other inputs and clears the register when LOW.

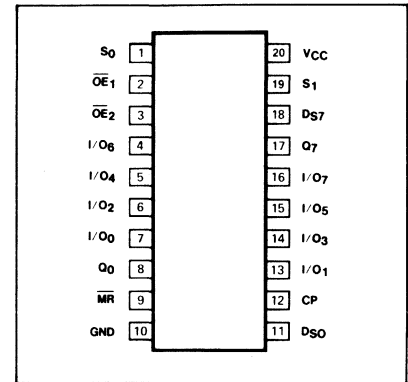
FEATURES

- 8-Bit universal shift register
- 8-Bit bidirectional 3-state I/O port
- Space saving 20-pin package
- Separate serial inputs and outputs for easy cascading
- Asynchronous Master Reset
- See "323" for Synchronous Reset version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS299N	
Ceramic DIP	N74LS299F	S54LS299F
Flatpak		

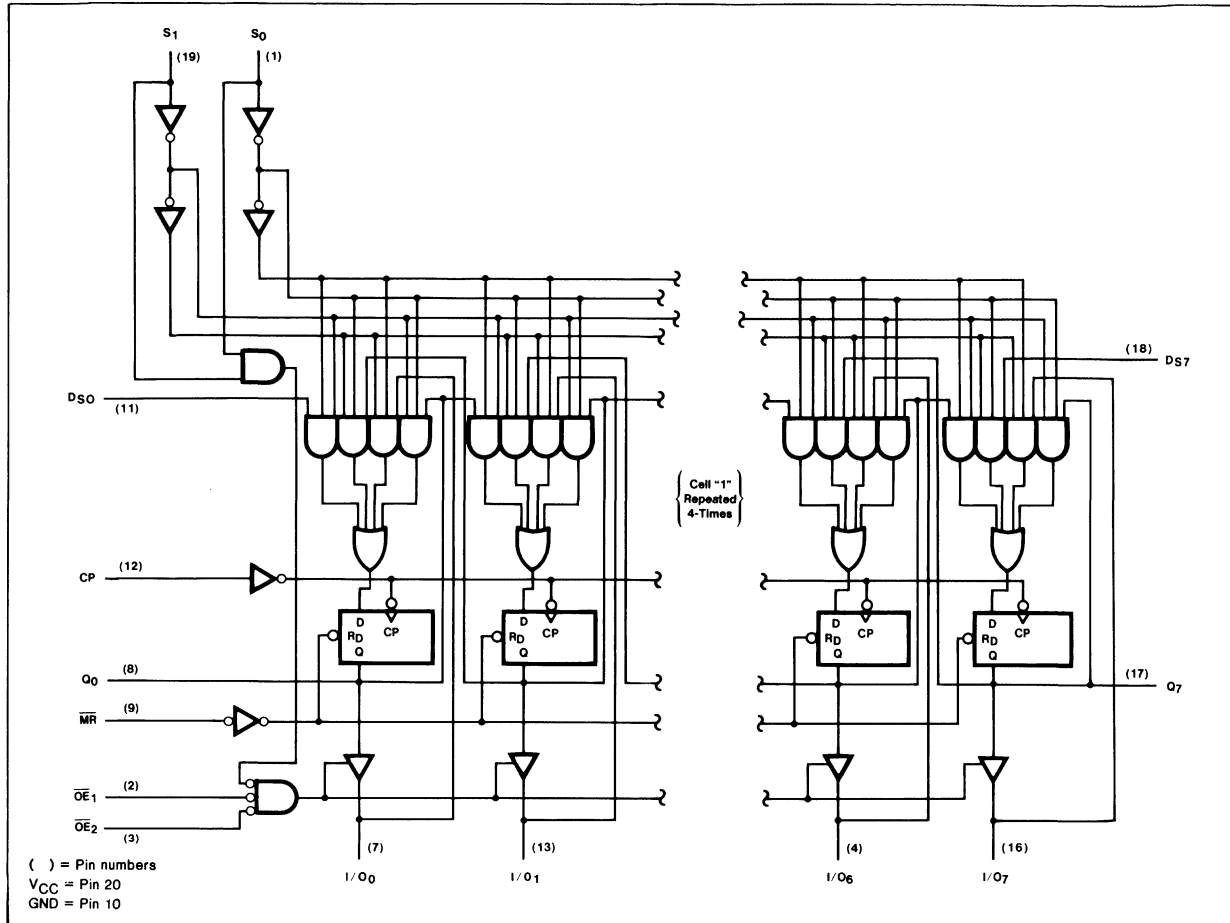
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
S_0, S_1	Mode Select inputs	I_{IH} (μA) I_{IL} (mA)			40 -0.8
DS_0, DS_7	Serial Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
$\overline{OE}_1, \overline{OE}_2$	Output Enable (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{MR}	Master Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
I/O_n	Parallel data input	I_{IH} (μA) I_{IL} (mA)			40 -0.4
I/O_n	3-State outputs	I_{OH} (mA) I_{OL} (mA)			-1/-2.6 (a) 12/24 (a)
Q_0, Q_7	Serial outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8 (a)

Note

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage I/O port	V _{CC} = Min, V _{OE} = V _{IL} I _{OH} = See Fan Out Table					2.4		V
V _{OL} Output LOW voltage I/O port	V _{CC} = Min, I _{OL} = 12mA V _{OE} = V _{IL} , I _{OL} = 24mA					0.4	0.5 ^(c)	V
I _{OS} Output short circuit current I/O port	V _{CC} = Max, V _{OUT} = 0V					-30	-100	mA
I _{CC} Supply current	V _{CC} = Max					60		mA
I _{OZH} Output "off" current HIGH	V _{CC} = Max, V _{OUT} = 2.7V					40		μA
I _{OZL} Output "off" current LOW	V _{CC} = Max, V _{OUT} = 0.4V					-400		μA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

FUNCTIONAL DESCRIPTION

The "299" is an 8-bit general purpose shift/storage register useful in a wide variety of shifting and 3-state bus interface applications. The register has four synchronous operating modes controlled by the two Select inputs as shown in the Mode Select-Function Table. The Mode Select (S_0, S_1) inputs, the Serial Data (DS_0, DS_7) inputs and the parallel data ($I/O_0-I/O_7$) inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP) input. Therefore, the only timing restriction is that the S_0, S_1 and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The Master Reset (\overline{MR}) is an asynchronous active LOW input. When LOW, the \overline{MR} overrides the clock and all other inputs and clears the register.

Serial mode expansion of the register is accomplished by tying the Q_0 serial output to the DS_7 input of the preceding register, and tying the Q_7 serial output to the DS_0 input of the following register. Recirculating the ($n \times 8$) bit words is accomplished by tying the Q_7 output of the last stage to the DS_0 input of the first stage.

The 3-state bidirectional Input Output port has three modes of operation. When the two Output Enable (\overline{OE}_1 & \overline{OE}_2) inputs are LOW, and one or both of the Select inputs are LOW, the data in the register is presented at the eight outputs. When both Select inputs are HIGH, the 3-state outputs are forced to the high impedance "off" state and the register is prepared to load data from the 3-state bus coincident with the next LOW-to-HIGH clock transition. In this parallel load mode, the Select inputs disable the outputs even if \overline{OE}_1 and \overline{OE}_2 are both LOW. A HIGH level on one of the Output Enable inputs will force the outputs to the high impedance "off" state. When disabled, the 3-state I/O ports present one unit load to the bus, since an input is tied to the I/O node. The enabled 3-state output is designed to drive heavy capacitive loads or heavily loaded 3-state buses.

MODE SELECT—FUNCTION TABLES

REGISTER OPERATING MODES	INPUTS							REGISTER OUTPUTS			
	\overline{MR}	CP	S_0	S_1	DS_0	DS_7	I/O _n	Q_0	$Q_1 \dots Q_6$	Q_7	
Reset (clear)	L	X	X	X	X	X	X	L	L ... L	L	
Shift right	H	↑	h	l	l	X	X	L	$q_0 \dots q_5$	q_6	
	H	↑	h	l	h	X	X	H	$q_0 \dots q_5$	Q_6	
Shift left	H	↑	l	h	X	l	X	q_1	$q_2 \dots q_7$	L	
	H	↑	l	h	X	h	X	q_1	$q_2 \dots q_7$	H	
Hold (do nothing)	H	↑	l	l	X	X	X	q_0	$q_1 \dots q_6$	q_7	
Parallel load	H	↑	h	h	X	X	l	L	L ... L	L	
	H	↑	h	h	X	X	h	H	H ... H	H	

3-STATE I/O PORT OPERATING MODE	INPUTS					INPUTS/OUTPUTS	
	\overline{OE}_1	\overline{OE}_2	S_0	S_1	Q_n (Register)	$I/O_0 \dots I/O_7$	
Read register	L	L	L	X	L	L	
	L	L	L	X	H	H	
	L	L	X	L	L	L	
	L	L	X	L	H	H	
Load register	X	X	H	H	$Q_n = I/O_n$	$I/O_n = \text{inputs}$	
Disable I/O	H	X	X	X	X	(Z)	
	X	H	X	X	X	(Z)	

H = HIGH voltage level
h = HIGH voltage level one setup time prior to LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 q_n = Lower case letters indicate the state of the referenced output one setup prior to the LOW-to-HIGH clock transition
X = Don't care
(Z) = High impedance "off" state
↑ = LOW-to-HIGH clock transition

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 45\text{pF}$ $R_L = 667\Omega$						
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Figure 1					35		MHz
t_{PLH} Propagation delay t_{PHL} Clock to I/O outputs	Figure						25 39	ns ns
t_{PLH} Propagation delay t_{PHL} Clock to Q_0 & Q_7 outputs	Figure 1 $R_L = 2\text{K}\Omega$, $C_L = 15\text{pF}$						33 39	ns ns
t_{PHL} Propagation delay $\overline{\text{MR}}$ to output	Figure 2						40	ns
t_{PZH} Enable time to HIGH level	Figure 3						21	ns
t_{PZL} Enable time to LOW level	Figure 4						30	ns
t_{PHZ} Disable time from HIGH level	Figure 3						33	ns
	Figure 3, $C_L = 5\text{pF}(d)$						15	ns
t_{PLZ} Disable time from LOW level	Figure 4						20	ns
	Figure 4, $C_L = 5\text{pF}(d)$						15	ns

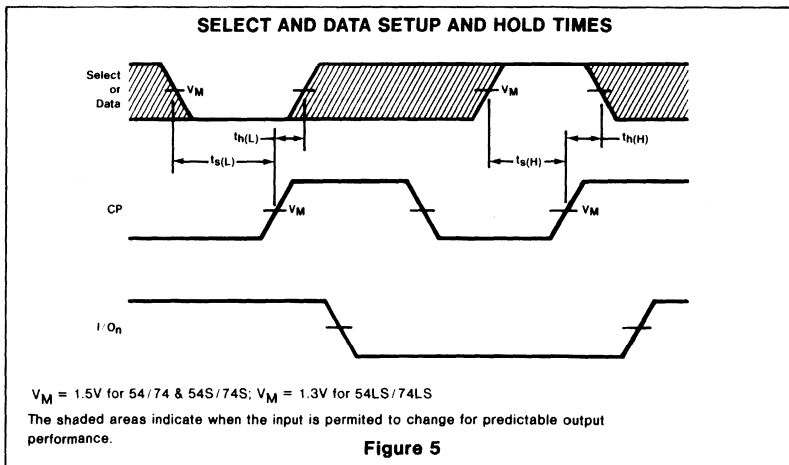
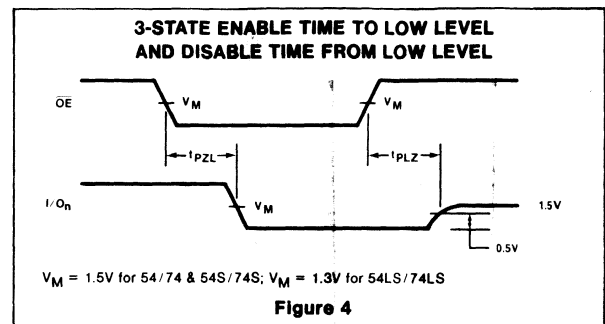
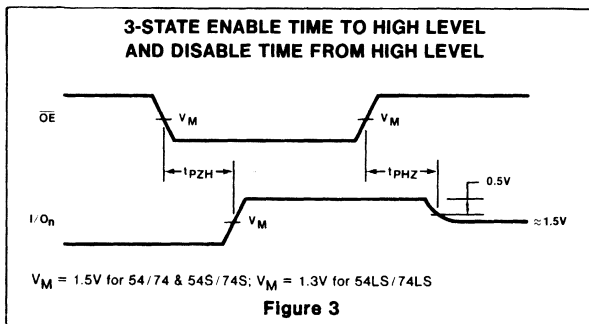
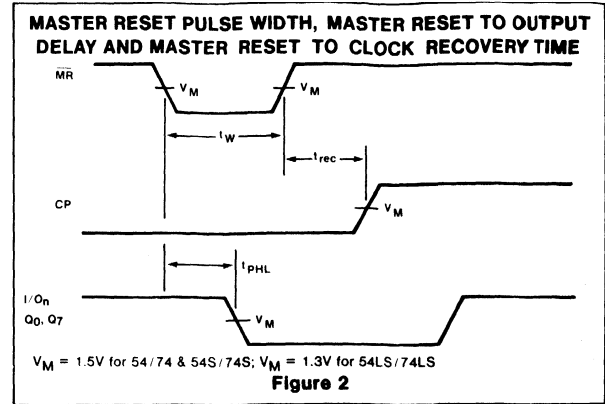
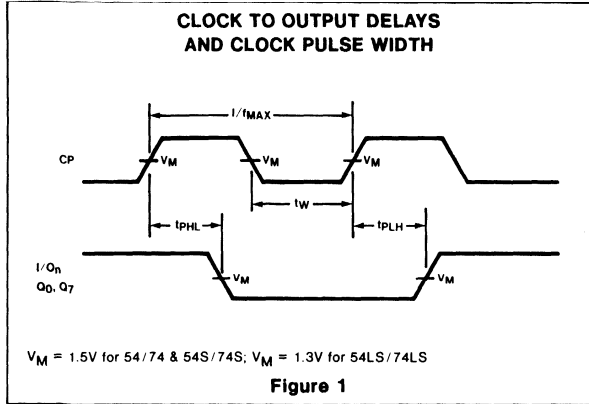
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_{W} Clock pulse width	Figure 1					20		ns
t_{W} Master Reset pulse width	Figure 2					20		ns
t_{S} Setup time D_{S0} , D_{S7} , I/O_n to clock	Figure 5					20		ns
t_{H} Hold time D_{S0} , D_{S7} , I/O_n to clock	Figure 5					3.0		ns
t_{S} Setup time Select to clock	Figure 5					20		ns
t_{H} Hold time Select to clock	Figure 5					3.0		ns
t_{rec} Recovery time $\overline{\text{MR}}$ to clock	Figure 2					20		ns

Notes

- c. This parameter for Commercial range only.
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC WAVEFORMS



54LS/74LS323 (Preliminary data)

DESCRIPTION

The "323" is an 8-Bit Bidirectional Universal Shift/Storage Register with a 3-state bidirectional Input/Output port. The register has four operating modes: shift right, shift left, parallel load, and hold (do nothing). The register has serial inputs and outputs for bidirectional cascading without interfering with the 3-state I/O port operation.

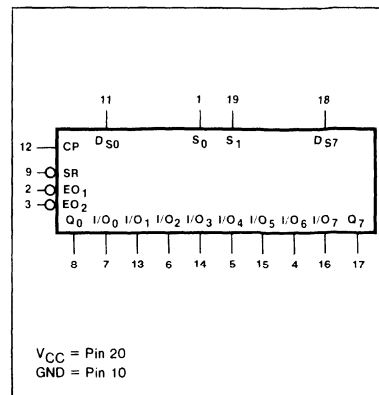
Parallel data is loaded into and read from the register through a 3-state I/O port controlled by two Output Enable (\overline{OE}) inputs and the Select inputs. The 3-state buffer outputs can drive heavily loaded buses, but present a light load to the bus when disabled or loading data.

The Synchronous Reset overrides the other inputs and clears the register coincident with the next LOW-to-HIGH clock transition.

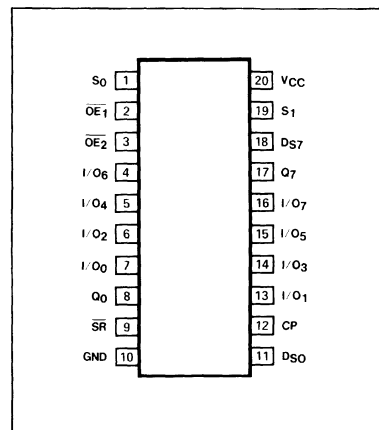
FEATURES

- 8-Bit universal shift register
- 8-Bit bidirectional 3-state I/O port
- Space saving 20-pin package
- Separate serial inputs and outputs for easy cascading
- Synchronous Reset
- See "299" for Asynchronous Master Reset version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS323N	
Ceramic DIP	N74LS323F	S54LS323F
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
S_0, S_1	Mode Select inputs	I_{IH} (μA) I_{IL} (mA)			40 -0.8
DS_0, DS_7	Serial Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
$\overline{OE}_1, \overline{OE}_2$	Output Enable (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{SR}	Synchronous Reset (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
I/O_n	Parallel data input	I_{IH} (μA) I_{IL} (mA)			40 -0.4
I/O_n	3-State outputs	I_{OH} (mA) I_{OL} (mA)			-1/-2.6(a) 12/24(a)
Q_0, Q_7	Serial outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "323" is an 8-bit general purpose shift/storage register useful in a wide variety of shifting and 3-state bus interface applications. The register has five synchronous operating modes controlled by the Two Select inputs and the Synchronous Reset as shown in the Mode Select-Function Table. The Mode Select (S_0, S_1) inputs, the Synchronous Reset (\overline{SR}) input the Serial Data (D_{S0}, D_{S7}) inputs and the parallel data ($I/O_0 - I/O_7$) inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP) input. Therefore, the only timing restriction is that the \overline{SR}, S_0, S_1 and selected data inputs must be stable one setup time prior to the positive transition of the clock pulse. The \overline{SR} input overrides the select and data inputs when LOW, and clears the register coincident with the next positive clock transition.

Serial mode expansion of the register is accomplished by tying the Q_0 serial output to the D_{S7} input of the preceding register, and tying the Q_7 serial output to the D_{S0} input of the following register. Recirculating the ($n \times 8$) bit words is accomplished by tying the Q_7 output of the last stage to the D_{S0} input of the first stage.

The 3-state bidirectional Input/Output port has three modes of operation. When the two Output Enable (\overline{OE}_1 and \overline{OE}_2) inputs are LOW, and one or both of the Select inputs are LOW, the data in the register is presented at the eight outputs. When both Select inputs are HIGH, the 3-state outputs are forced to the high impedance "off" state and the register is prepared to load data from the 3-state bus coincident with the next LOW-to-HIGH clock transition. In this parallel load mode, the Select inputs disable the outputs even if \overline{OE}_1 and \overline{OE}_2 are both LOW. A HIGH level on one of the Output Enable inputs will force the outputs to the high impedance "off" state. When disabled, the 3-state I/O ports present one unit load to the bus, since an input is tied to the I/O mode. The enabled 3-state output is designed to drive heavy capacitive loads or heavily loaded 3-state buses.

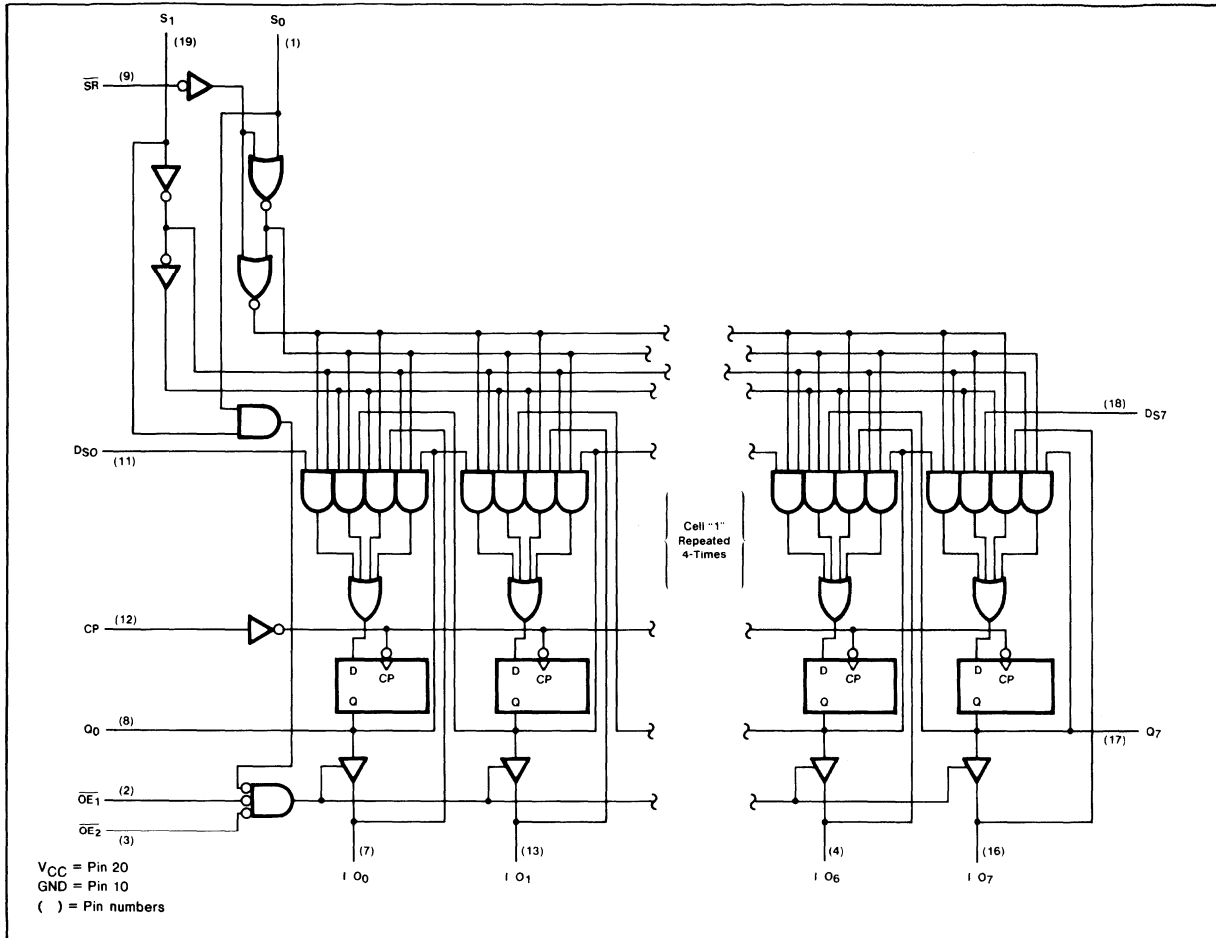
MODE SELECT—FUNCTION TABLES

REGISTER OPERATING MODES	INPUTS							REGISTER OUTPUTS			
	\overline{SR}	CP	S_0	S_1	D_{S0}	D_{S7}	I/O_n	Q_0	$Q_1 \dots Q_6$	Q_7	
Reset (clear)	l	↑	X	X	X	X	X	L	L ... L	L	
Shift right	h	↑	h	l	l	X	X	L	$q_0 \dots q_5$	q_6	
	h	↑	h	l	h	X	X	H	$q_0 \dots q_5$	Q_6	
Shift left	h	↑	l	h	X	l	X	q_1	$q_2 \dots q_7$	L	
	h	↑	l	h	X	h	X	q_1	$q_2 \dots q_7$	H	
Hold (do nothing)	h	↑	l	l	X	X	X	q_0	$q_1 \dots q_6$	q_7	
Parallel load	h	↑	h	h	X	X	l	L	L ... L	L	
	h	↑	h	h	X	X	h	H	H ... H	H	

3-STATE I/O PORT OPERATING MODE	INPUTS					INPUTS/OUTPUTS	
	\overline{OE}_1	\overline{OE}_2	S_0	S_1	Q_n (REGISTER)	$I/O_0 \dots I/O_7$	
Read register	L	L	L	X	L	L	
	L	L	L	X	H	H	
	L	L	X	L	L	L	
	L	L	X	L	H	H	
Load register	X	X	H	H	$Q_n = I/O_n$	$I/O_n = \text{inputs}$	
Disable I/O	H	X	X	X	X	(Z)	
	X	H	X	X	X	(Z)	

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 q_n = Lower case letters indicate the state of the referenced output one setup prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 (Z) = High impedance "off" state.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage I/O Port	$V_{CC} = \text{Min}, V_{OE} = V_{IL}$ $I_{OH} = \text{See Fan Out Table}$					2.4		V
V_{OL} Output LOW voltage I/O Port	$V_{CC} = \text{Min}, V_{OE} = V_{IL}$ $I_{OL} = 12\text{mA}$ $I_{OL} = 24\text{mA}$						0.4	V
							0.5(c)	V
I_{OS} Output short circuit	$V_{CC} = \text{Max}, V_{OUT} = 0\text{V}$					-30	-100	mA
I_{CC} Supply current	$V_{CC} = \text{Max}$						60	mA
I_{OZH} Output "off" current HIGH	$V_{CC} = \text{Max}, V_{OUT} = 2.7\text{V}$						40	μA
I_{OZL} Output "off" current LOW	$V_{CC} = \text{Max}, V_{OUT} = 0.4\text{V}$						-400	μA

NOTES

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial Range only.

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 45\text{pf}$ $R_L = 667\Omega$						
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Figure 1					35		MHz
t_{PLH} Propagation delay t_{PHL} Clock to I/O outputs	Figure 1					25 39		ns ns
t_{PLH} Propagation delay t_{PHL} Clock to Q_0 & Q_7 outputs	Figure 1 $R_L = 2k\Omega$, $C_L = 15\text{pF}$					33 39		ns ns
t_{PZH} Enable time to HIGH level	Figure 2					21		ns
t_{PZL} Enable time to LOW level	Figure 3					30		ns
t_{PHZ} Disable time from HIGH level	Figure 2					33		ns
	Figure 2, $C_L = 5\text{pF}(d)$					15		ns
t_{PLZ} Disable time from LOW level	Figure 3					20		ns
	Figure 3, $C_L = 5\text{pF}(d)$					15		ns

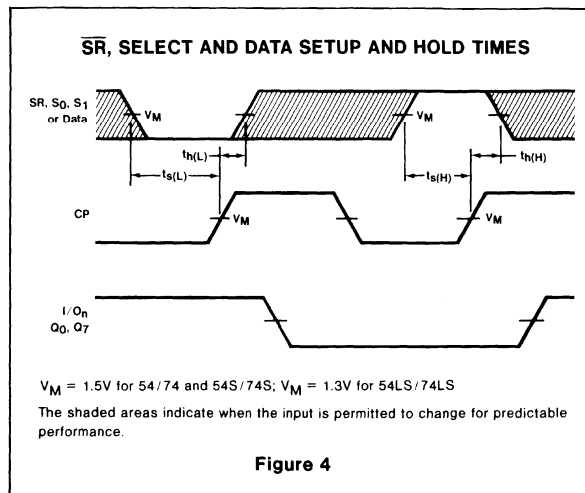
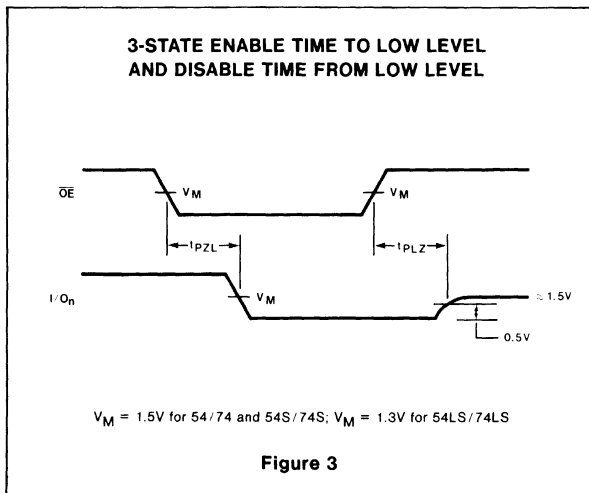
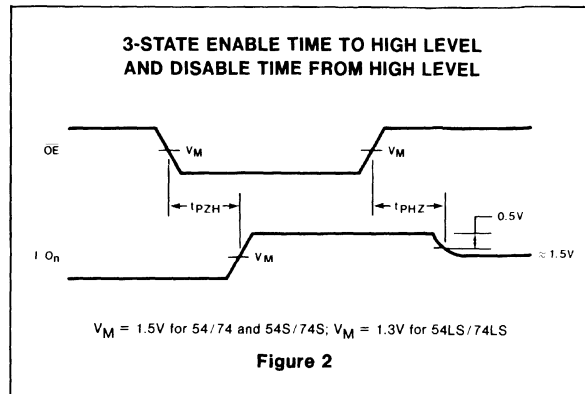
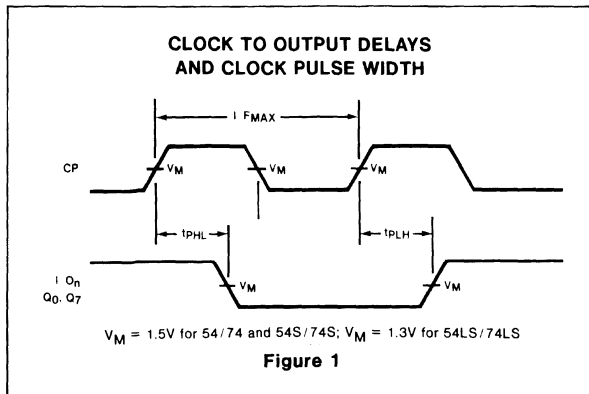
NOTE

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_{W} Clock pulse width	Figure 1					20		ns
t_{S} Set-up time $\overline{\text{SR}}$ to Clock	Figure 4					25		ns
t_{H} Hold time $\overline{\text{SR}}$ to Clock	Figure 4					0		ns
t_{S} Set-up time D_{SR} , D_{SL} , I/O _n to Clock	Figure 4					20		ns
t_{H} Hold time D_{SR} , D_{SL} , I/O _n to Clock	Figure 4					3.0		ns
t_{S} Set-up time Select to Clock	Figure 4					20		ns
t_{H} Hold time Select to Clock	Figure 4					3.0		ns

AC WAVEFORMS



54S/74S350
(AM25S10)

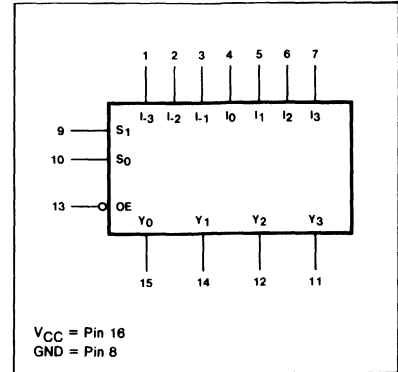
DESCRIPTION

The "350" is a combinatorial logic circuit that accepts a 4-bit data word and shifts the word 0, 1, 2, or 3 places. The number of places to be shifted is determined by two Select inputs S_0 and S_1 . The 3-state outputs allow expansion of shifting over a larger number of places.

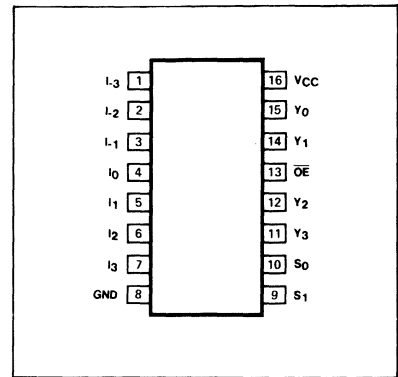
FEATURES

- Shifts 4-bits of data to 0, 1, 2, 3 places under control of two select lines
- 3-State outputs for bus organized systems
- Alternate source AM25S10

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S350N	
Ceramic DIP	N74S350F	S54S350F
Flatpak		S54S350W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S_0, S_1	Select inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0	
$I_0, I_1, I_2, I-1, I-2$	Data inputs	I_{IH} (μA) I_{IL} (mA)		75 -3.0	
$I_3, I-3$	Data inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0	
\overline{OE}	Output Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)		50 -2.0	
$Y_0 - Y_3$	3-State outputs	I_{OH} (mA) I_{OL} (mA)		-2 / -6.5 20	

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

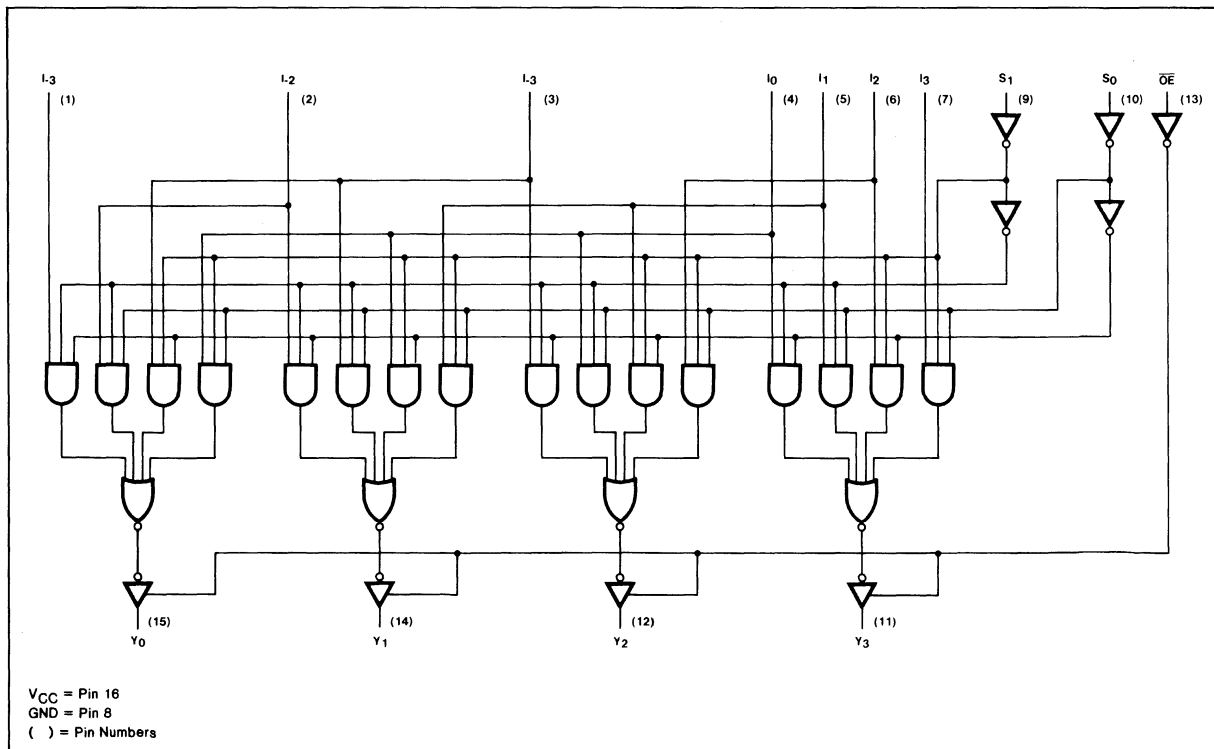
FUNCTIONAL DESCRIPTION

The "350" is a combination logic circuit that shifts a 4-bit word from "0" to "3" places. No clocking is required as with shift registers.

The "350" can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical - with logic zeros filled in at either end of the shifting field
2. Arithmetic - where the sign bit is extended during a shift down
3. End around - where the data word forms a continuous loop.

The 3-state outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active LOW Output Enable (\overline{OE}) input controls the state of the outputs. The outputs are in the high impedance "off" state when \overline{OE} is HIGH, and they are active when \overline{OE} is LOW.

LOGIC DIAGRAM

TRUTH TABLE

OE	S ₁	S ₀	I ₃	I ₂	I ₁	I ₀	L ₁	L ₂	L ₃	Y ₃	Y ₂	Y ₁	Y ₀
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D ₃	D ₂	D ₁	D ₀	X	X	X	D ₃	D ₂	D ₁	D ₀
L	L	H	X	D ₂	D ₁	D ₀	D ₁	X	X	D ₂	D ₁	D ₀	D ₁
L	H	L	X	X	D ₁	D ₀	D ₁	D ₂	X	D ₁	D ₀	D ₁	D ₂
L	H	H	X	X	X	D ₀	D ₁	D ₂	D ₃	D ₀	D ₁	D ₂	D ₃

H = HIGH voltage level
 L = Low voltage level
 X = Don't care
 (Z) = High impedance (off) state
 D_n = HIGH or LOW state of the referenced I_n input

LOGIC EQUATIONS

$$Y_0 = S_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot L_1 + S_0 \cdot S_1 \cdot I_2 + S_0 \cdot S_1 \cdot I_3$$

$$Y_1 = S_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot L_1 + S_0 \cdot S_1 \cdot L_2$$

$$Y_2 = S_0 \cdot S_1 \cdot I_2 + S_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot L_1$$

$$Y_3 = S_0 \cdot S_1 \cdot I_3 + S_0 \cdot S_1 \cdot I_2 + S_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = Min, I _{OH} = See Fan Out Table			2.4				V
I _{CC} Supply current	V _{CC} = Max, V _{IN} = 0V				85			mA

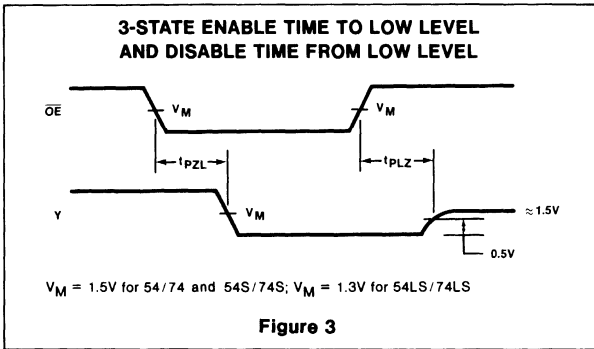
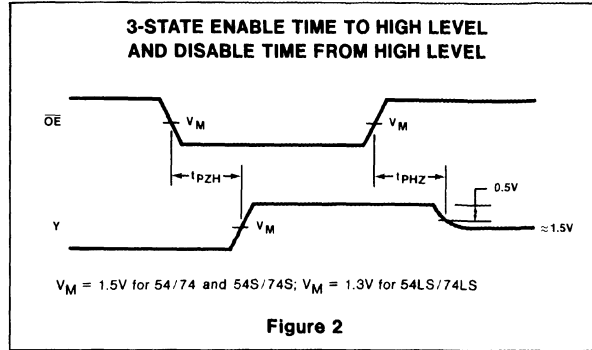
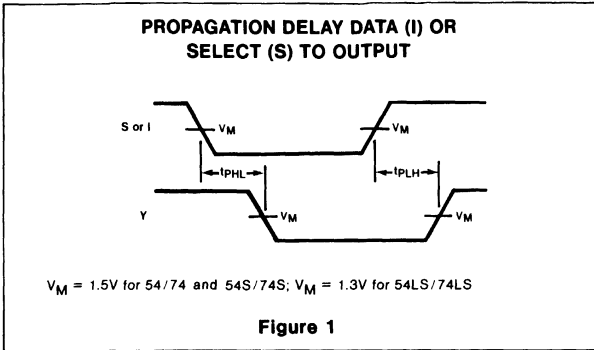
AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
				C _L = 15pF R _L = 280Ω				
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Data to output	Figure 1				10.5			ns ns
t _{PLH} Propagation delay t _{PHL} Select to output	Figure 1				17 20			ns ns
t _{pZH} Enable time to HIGH level	Figure 2				19.5			ns
t _{pZL} Enable time to LOW level	Figure 3				21			ns
t _{PHZ} Disable time from HIGH level	Figure 2, C _L = 5pF				8.0			ns
t _{PLZ} Disable time from LOW level	Figure 3, C _L = 5pF				15			ns

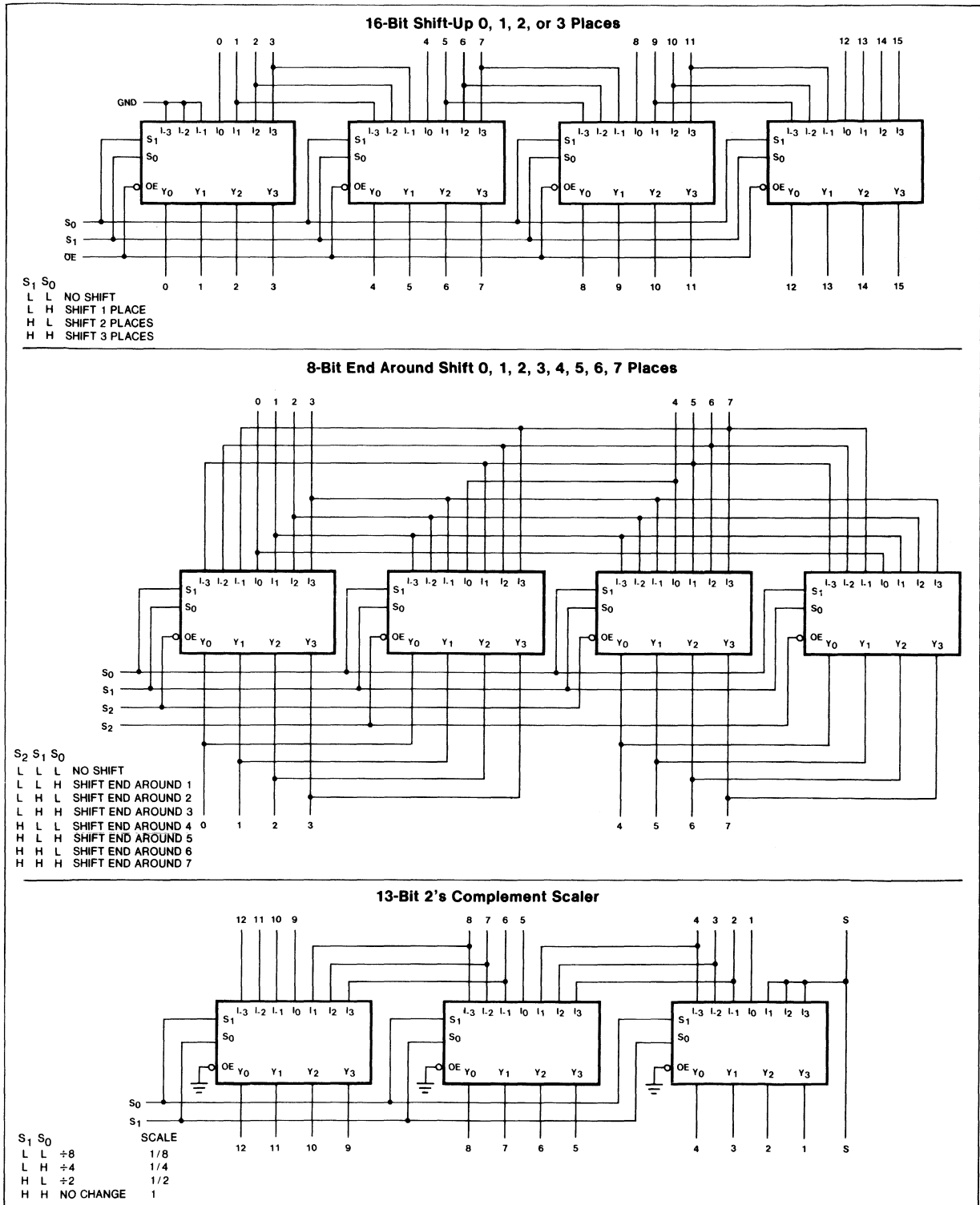
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



APPLICATIONS



54LS/74LS363

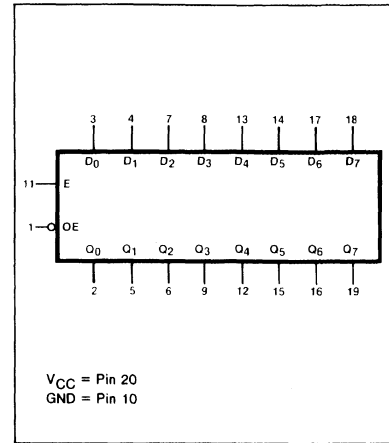
DESCRIPTION

The "363" is an 8-Bit Transparent Latch with 3-state buffered outputs. The latch is used primarily for driving MOS memories or MOS microprocessors which require higher than normal V_{IH} levels. The latch outputs follow the data inputs when the latch Enable is HIGH, and they are stable when the Enable is LOW. The 3-state output buffers are controlled by an active LOW Output Enable (\overline{OE}) input. A HIGH on the \overline{OE} input forces the eight outputs to the high impedance "off" state. When \overline{OE} is LOW, the latched or transparent data appears at the outputs.

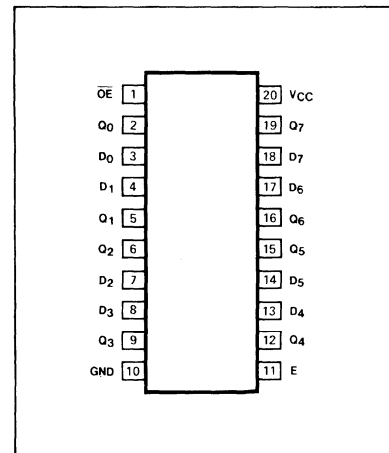
FEATURES

- 8-Bit transparent latch
- 3-State MOS compatible output buffers
- Common Latch Enable input with hysteresis
- Common 3-state Output Enable control
- Independent latch and 3-state buffer operation

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS363N	
Ceramic DIP	N74LS363F	S54LS363F
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
E	Latch Enable (active HIGH) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D ₀ -D ₇	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{OE}	Output Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q ₀ -Q ₇	3-State outputs	I_{OH} (mA) I_{OL} (mA)			-1 / -2.6 (a) 12 / 24 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "363" is Octal Transparent Latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs is transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about one volt closer to V_{CC} , or to over 3.5V at minimum V_{CC} . This feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V.

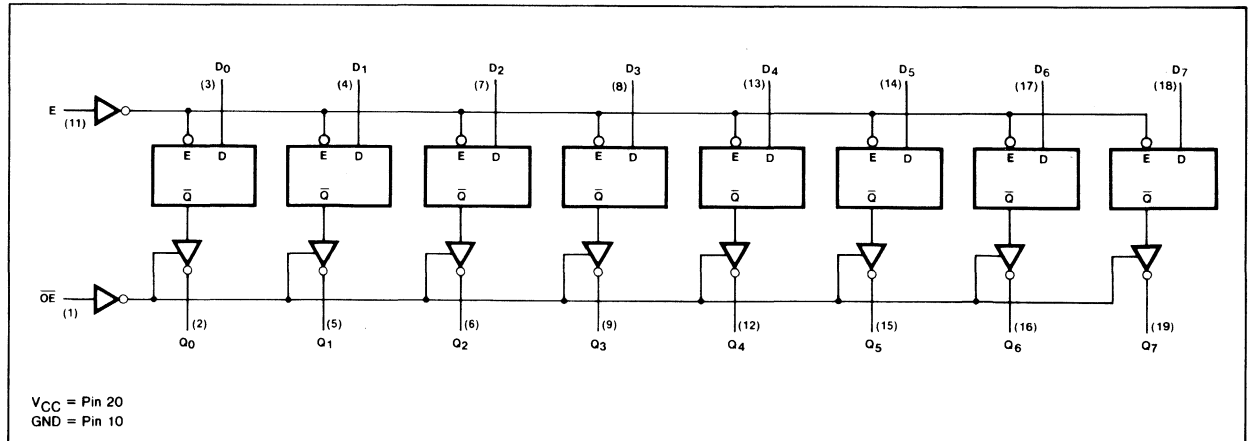
The active LOW Output Enable (\overline{OE}) controls all eight 3-state buffers independent of the latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS Q ₀ - Q ₇
	\overline{OE}	E	D _n		
Enable & read register	L	H	L	L	L
	L	H	H	H	H
Latch & read register	L	L	L	L	L
	L	L	h	H	H
Latch register & disable outputs	H	L	L	L	(Z)
	H	L	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
 (Z) = High impedance "off" state

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min, I _{OL} = 12mA						0.4	V
	V _{OE} = V _{IL} , I _{OL} = 24mA						0.5 (c)	V
V _{OH} Output HIGH voltage	V _{CC} = Min, I _{OH} = -1.0mA Mil					3.45		V
	V _{OE} = V _{IL} , I _{OH} = -2.6mA Com					3.65		V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V					-40	-120	mA
I _{CC} Supply current	V _{CC} = Max						70	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 45pF R _L = 667Ω						
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Latch Enable to output	Figure 1						30 40	ns ns
t _{PLH} Propagation delay t _{PHL} Data to output	Figure 4						18 32	ns ns
t _{PZH} Enable time to HIGH level	Figure 2						20	ns
t _{PZL} Enable time to LOW level	Figure 3						28	ns
t _{PHZ} Disable time from HIGH level	Figure 2						35	ns
	Figure 2, C _L = 5pF(d)						18	ns
t _{PLZ} Disable time from LOW level	Figure 3						20	ns
	Figure 3, C _L = 5pF(d)						18	ns

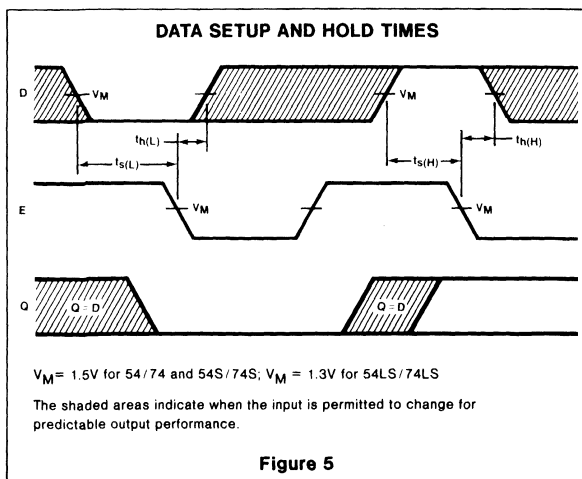
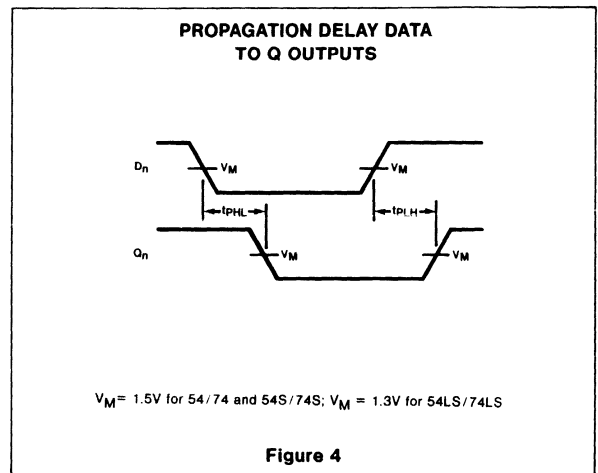
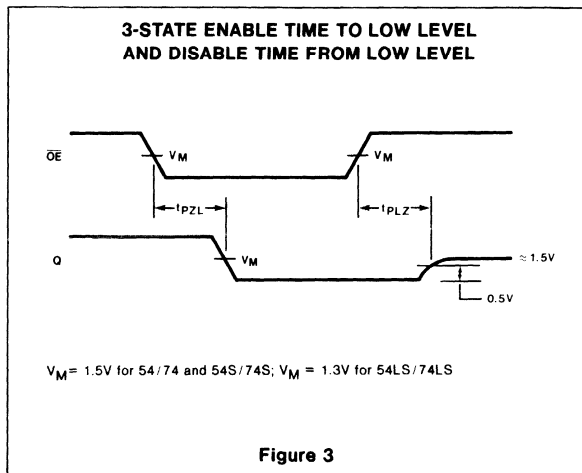
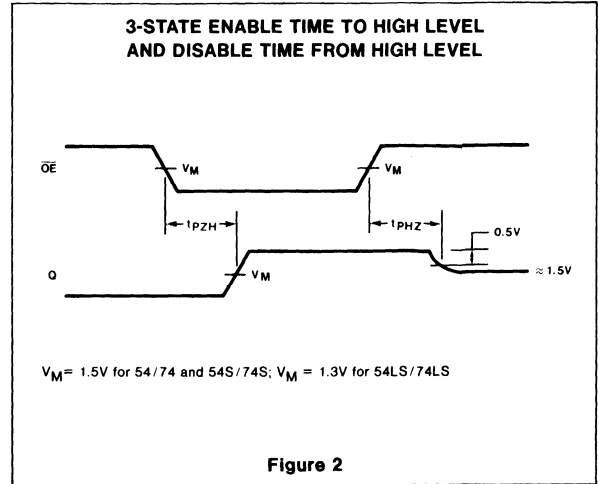
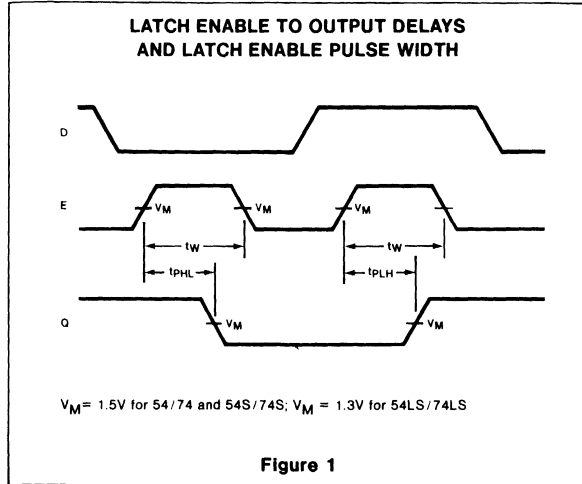
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Latch Enable pulse width	Figure 1					15		ns
t _s Setup time Data to Latch Enable	Figure 5					3.0		ns
t _h Hold time Data to Latch Enable	Figure 5					10		ns

NOTES

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial Range only.
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC WAVEFORMS



54LS/74LS364

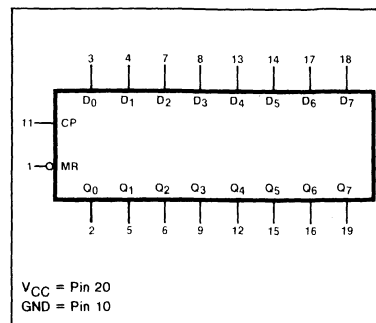
DESCRIPTION

The "364" is an Octal D Flip-Flop with 3-state buffered outputs. The device is used primarily as an 8-bit positive edge triggered storage register for interfacing with MOS memories or MOS microprocessors which require higher than normal V_{IH} levels. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the Clock (CP) input. The 3-state output buffers are controlled by an active LOW Output Enable (\overline{OE}) input. A HIGH on the \overline{OE} input forces the eight outputs to the high impedance "off" state. When \overline{OE} is LOW, the data in the register appears at the outputs.

FEATURES

- 8-Bit positive edge triggered register
- 3-State MOS compatible output buffers
- Common Clock input with hysteresis
- Common 3-state Output Enable control
- Independent register and 3-state buffer operation

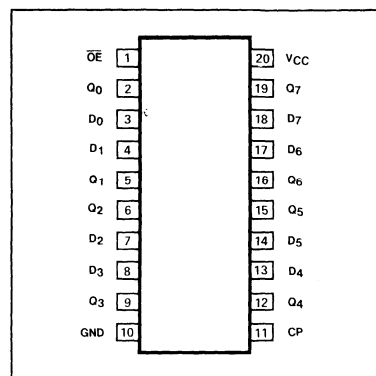
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS364N	
Ceramic DIP	N74LS364F	S54LS364F
Flatpak		

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D ₀ -D ₇	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{OE}	Output Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q ₀ -Q ₇	3-State outputs	I_{OH} (mA) I_{OL} (mA)			-1 / -2.6 ^(a) 12/24 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "363" is Octal Transparent Latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs is transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about one volt closer to V_{CC} , or to over 3.5V at minimum V_{CC} . This feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V.

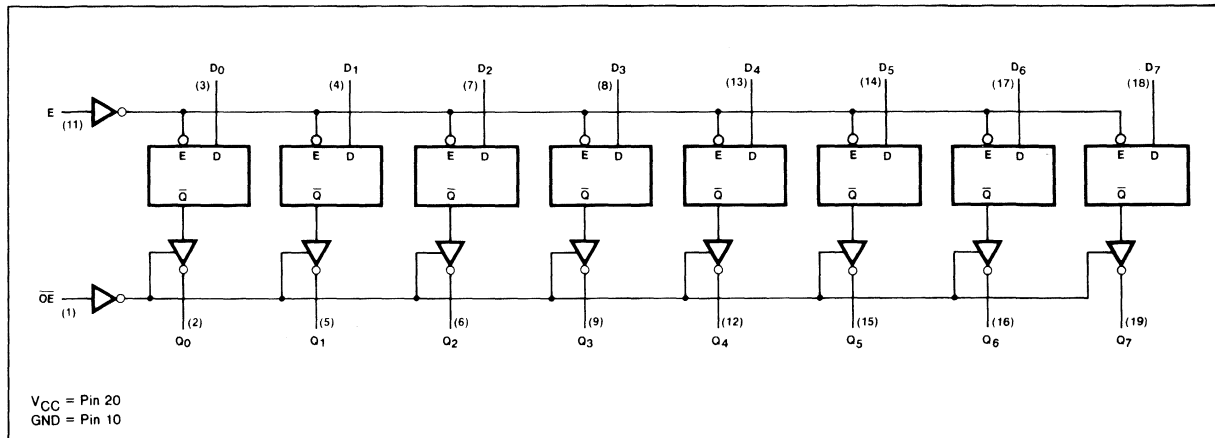
The active LOW Output Enable (\overline{OE}) controls all eight 3-state buffers independent of the latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS Q ₀ - Q ₇
	\overline{OE}	E	D _n		
Enable & read register	L L	H H	L H	L H	L H
Latch & read register	L L	L L	l h	L H	L H
Latch register & disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltage level
 h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
 (Z) = High impedance "off" state

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min I _{OL} = 12mA						0.4	V
	V _{OE} = V _{IL} I _{OL} = 24mA						0.5 (c)	V
V _{OH} Output HIGH voltage	V _{CC} = Min I _{OH} = -1.0mA Mil					3.45		V
	V _{OE} = V _{IL} I _{OH} = -2.6mA Com					3.65		V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V					-40	-120	mA
I _{CC} Supply current	V _{CC} = Max						70	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	C _L = 45pF R _L = 667Ω		
						Min	Max	
t _{PLH} Propagation delay	Figure 1						30	ns
t _{PHL} Latch Enable to output							40	ns
t _{PLH} Propagation delay	Figure 4						18	ns
t _{PHL} Data to output							32	ns
t _{PZH} Enable time to HIGH level	Figure 2						20	ns
t _{PZL} Enable time to LOW level	Figure 3						28	ns
t _{PHZ} Disable time from HIGH level	Figure 2						35	ns
	Figure 2, C _L = 5pF(d)						18	ns
t _{PLZ} Disable time from LOW level	Figure 3						20	ns
	Figure 3, C _L = 5pF(d)						18	ns

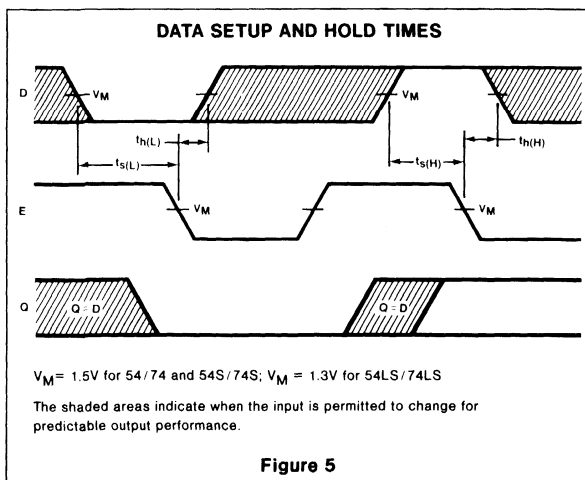
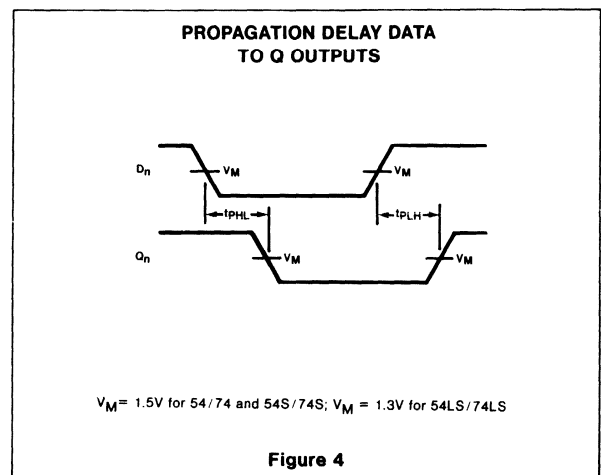
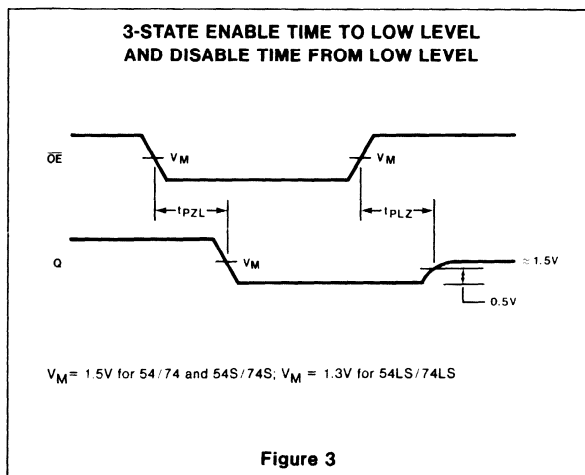
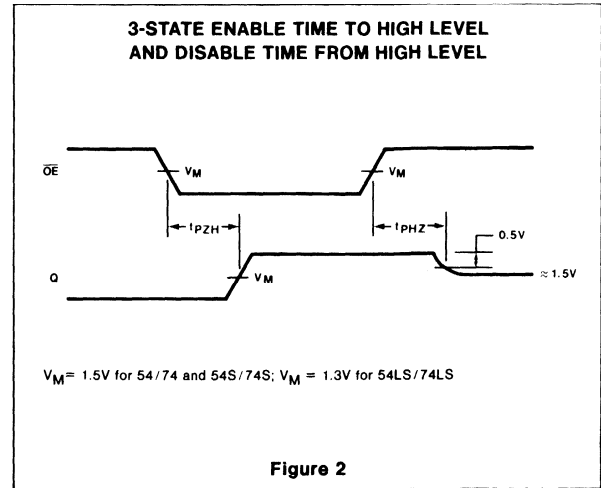
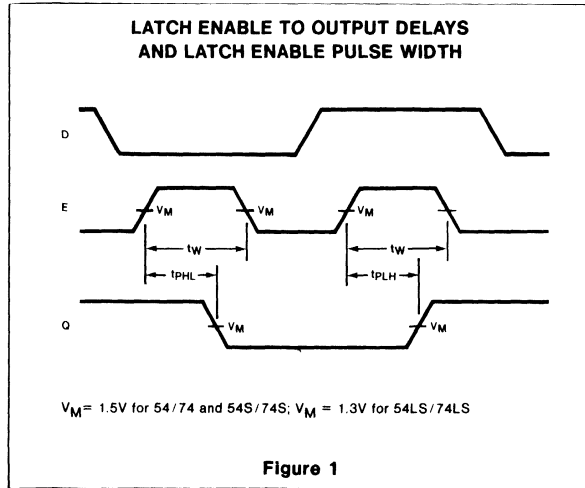
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _W Latch Enable pulse width	Figure 1					15		ns
t _s Setup time Data to Latch Enable	Figure 5					3.0		ns
t _h Hold time Data to Latch Enable	Figure 5					10		ns

NOTES

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial Range only.
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC WAVEFORMS



54LS/74LS364

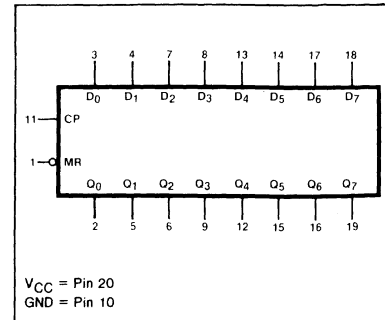
DESCRIPTION

The "364" is an Octal D Flip-Flop with 3-state buffered outputs. The device is used primarily as an 8-bit positive edge triggered storage register for interfacing with MOS memories or MOS microprocessors which require higher than normal V_{IH} levels. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the Clock (CP) input. The 3-state output buffers are controlled by an active LOW Output Enable (\overline{OE}) input. A HIGH on the \overline{OE} input forces the eight outputs to the high impedance "off" state. When \overline{OE} is LOW, the data in the register appears at the outputs.

FEATURES

- 8-Bit positive edge triggered register
- 3-State MOS compatible output buffers
- Common Clock input with hysteresis
- Common 3-state Output Enable control
- Independent register and 3-state buffer operation

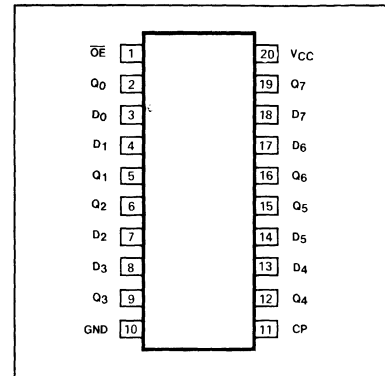
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ\text{C to } +70^\circ\text{C}$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ\text{C to } +125^\circ\text{C}$
Plastic DIP	N74LS364N	
Ceramic DIP	N74LS364F	S54LS364F
Flatpak		

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D_0 - D_7	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{OE}	Output Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q_0 - Q_7	3-State outputs	I_{OH} (mA) I_{OL} (mA)			-1 / -2.6 ^(a) 12/24 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "364" is an 8-bit edge triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about one volt closer to V_{CC} , or to over 3.5V at minimum V_{CC} . This feature makes these de-

vices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V. The active LOW Output Enable (\overline{OE}) controls all eight 3-state buffers independent of the register operation. When \overline{OE} is

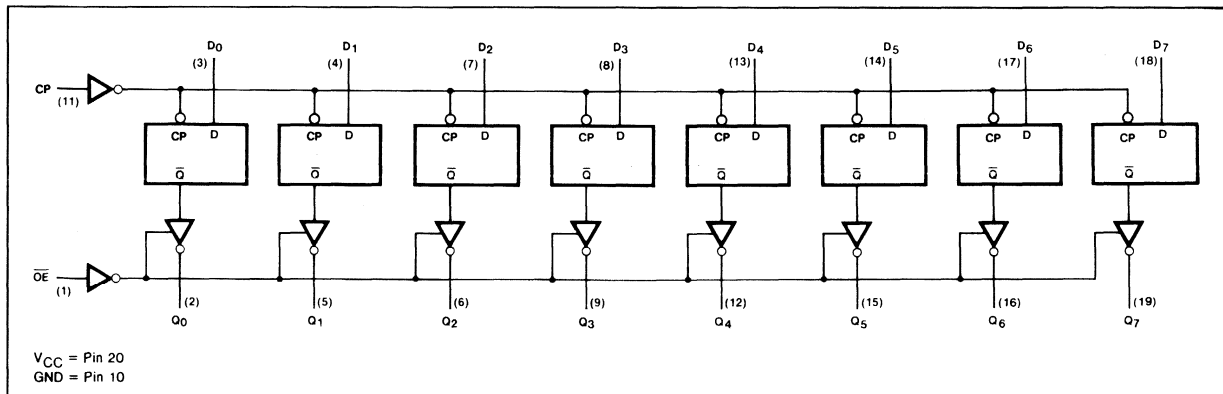
LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		Q ₀ -Q ₇
Load & read register	L	↑	l	L	L
	L	↑	h	H	H
Load register & disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 (Z) = High impedance "off" state
 ↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	$V_{CC} = \text{Min}$ $I_{OL} = 12\text{mA}$						0.4	V
	$V_{\overline{OE}} = V_{IL}$ $I_{OL} = 21\text{mA}$						0.5 (c)	V
V _{OH} Output HIGH Voltage	$V_{CC} = \text{Min}$ $I_{OH} = -1.0\text{mA}$ Mil					3.45		V
	$V_{\overline{OE}} = V_{IL}$ $I_{OH} = -2.6\text{mA}$ Com					3.65		V
I _{OS} Output short	$V_{CC} = \text{Max}, V_{OUT} = 0\text{V}$					-40	-120	mA
I _{CC} Supply current	$V_{CC} = \text{Max}$						70	mA

NOTES

- b. For family dc characteristics, see inside front cover for 54/74H, and see inside back cover for 54S/74LS specifications.
- c. This parameter for Commercial Range only.

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Figure 1					35		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Figure 1						28 38	ns ns
t_{PZH} Enable time to HIGH level	Figure 2						20	ns
t_{PZL} Enable time to LOW level	Figure 3						28	ns
t_{PHZ} Disable time from HIGH level	Figure 2						35	ns
	Figure 2, $C_L = 5\text{pF}(d)$						18	ns
t_{PLZ} Disable time from LOW level	Figure 3						20	ns
	Figure 3, $C_L = 5\text{pF}(d)$						18	ns

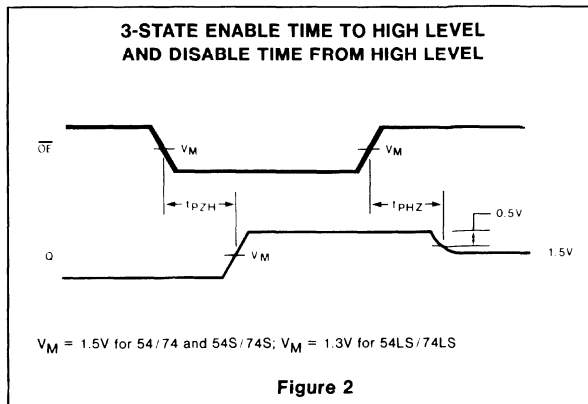
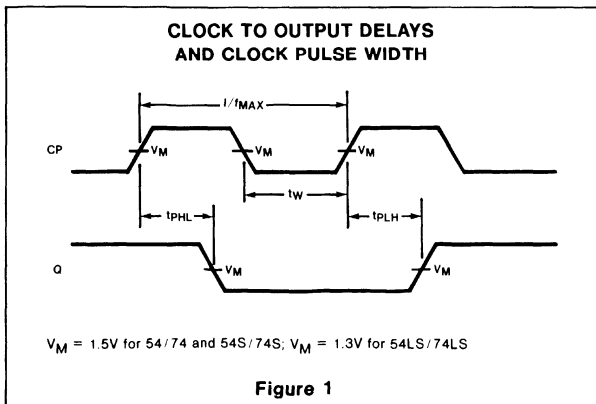
NOTE

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

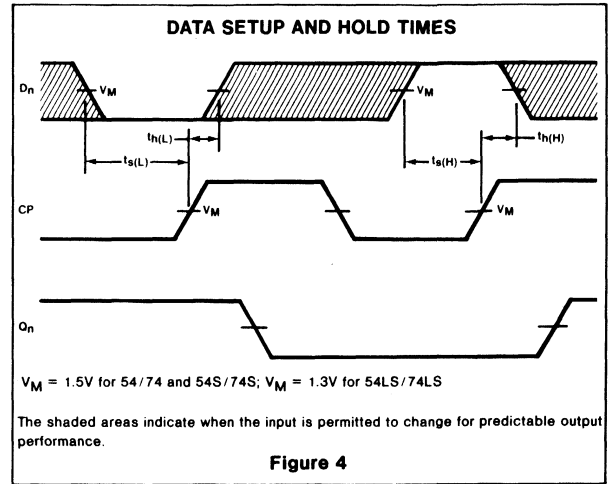
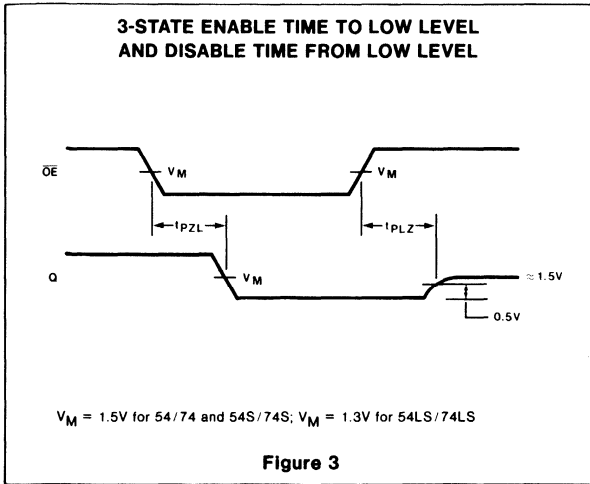
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w Clock pulse width	Figure 1					15		ns
t_s Setup time data to clock	Figure 4					10		ns
t_h Hold time data to clock	Figure 4					3.0		ns

AC WAVEFORMS



AC WAVEFORMS (Cont'd)

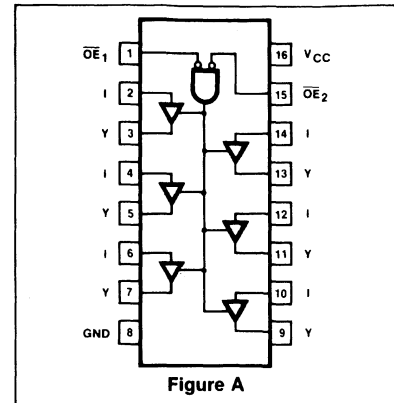


54/74365A (70/8095)
54LS/74LS365A
(See 8T95 for Schottky version)

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74365AN • N74LS365AN (DM8095N)	
Ceramic DIP	Fig. A	N74365AF • N74LS365AF (DM8095J)	S54365AF • S54LS365AF (DM7095J)
Flatpak	Fig. A		S54365AW • S54LS365AW (DM7095W)

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.36
Outputs	I_{OH} (μA)	-2/-5.2 ^(a)			-1/-2.6 ^(a)
	I_{OL} (mA)	32			12/24 ^(a)

TRUTH TABLE

INPUTS			OUTPUTS
\overline{OE}_1	\overline{OE}_2	I	Y
L	L	L	L
L	L	H	H
X	H	X	(Z)
H	X	X	(Z)

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
(Z) = High impedance (off) state.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH voltage $V_{CC} = \text{Min}$, $V_I = 2.0V$, $V_{\overline{OE}} = V_{IL}$, $I_{OH} = \text{See above table}$	2.4						2.4		V
V_{OL}	Output LOW voltage $V_{CC} = \text{Min}$, $V_I = V_{IL}$, $V_{\overline{OE}} = V_{IL}$		0.4							V
								0.4		V
								0.5 ^(c)		V
I_{OS}	Output short circuit current $V_{CC} = \text{Max}$, $V_{OUT} = 0V$	-30	-115					-30	-100	mA
I_{CC}	Supply current $V_{CC} = \text{Max}$, $V_I = 0V$, $V_{\overline{OE}} = 4.5V$		85					24		mA
I_{IL}	Input LOW current when disabled $V_{CC} = \text{Max}$, $V_{\overline{OE}} = 2.0V$, $V_I = 0.5V$		-40						-20	μA

NOTES

- The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- This parameter for Commercial Range only.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 50\text{pF}$ $R_L = 400\Omega$						$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 2		16						15	ns
			22						12	ns
t_{PZH} Enable to HIGH	Waveform 6		35						18	ns
t_{PZL} Enable to LOW	Waveform 7		37						24	ns
t_{PHZ} Disable from HIGH	Waveform 6								37	ns
	Waveform 6 $C_L = 5\text{pF}^{(d)}$		11						20	ns
t_{PLZ} Disable from LOW	Waveform 7								23	ns
	Waveform 7 $C_L = 5\text{pF}^{(d)}$		27						18	ns

NOTE

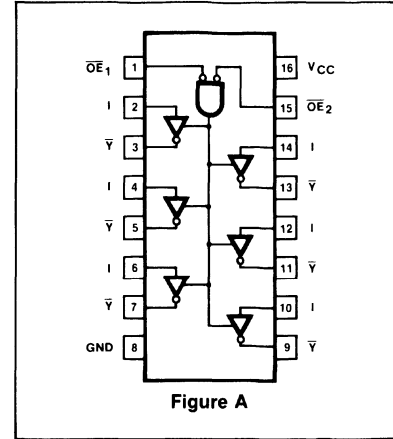
d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

**54/74366A (70/8096)
54LS/74LS366A
(See 8T96 for Schottky version)**

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74366AN • N74LS366AN (DM8096N)	
Ceramic DIP	Fig. A	N74366AF • N74LS366AF (DM8096J)	S54366AF • S54LS366AF (DM7096J)
Flatpak	Fig. A		S54366AW • S54LS366AW (DM7096W)

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.36
Outputs	I_{OH} (μA)	-2/-5.2 ^(a)			-1/-2.6 ^(a)
	I_{OL} (mA)	32			12/24 ^(a)

TRUTH TABLE

INPUTS			OUTPUTS
\overline{OE}_1	\overline{OE}_2	I	\overline{Y}
L	L	L	H
L	L	H	L
X	H	X	(Z)
H	X	X	(Z)

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
(Z) = High impedance (off) state.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}, V_I = V_{IL}, V_{\overline{OE}} = V_{IL}, I_{OH} = \text{See above table}$	2.4						2.4		V
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}, V_I = 2.0V, V_{\overline{OE}} = V_{IL}$		0.4						0.4	V
									0.5 ^(c)	V
I_{OS} Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$	-30	-115					-30	-100	mA
I_{CC} Supply current	$V_{CC} = \text{Max}, V_I = 0V, V_{\overline{OE}} = 4.5V$		77						21	mA
I_{IL} Input LOW current when disabled	$V_{CC} = \text{Max}, V_{\overline{OE}} = 2.0V, V_I = 0.5V$		-40						-20	μA

NOTES

- The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- This parameter for Commercial Range only.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 50\text{pF}$ $R_L = 400\Omega$						$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay		17						10	ns
			16						12	ns
t_{PZH}	Enable to HIGH		35						18	ns
t_{PZL}	Enable to LOW		37						24	ns
t_{PHZ}	Disable from HIGH								37	ns
	Waveform 6 $C_L = 5\text{pF}^{(d)}$		11						20	ns
t_{PLZ}	Disable from LOW								23	ns
	Waveform 7 $C_L = 5\text{pF}^{(d)}$		27						18	ns

NOTE

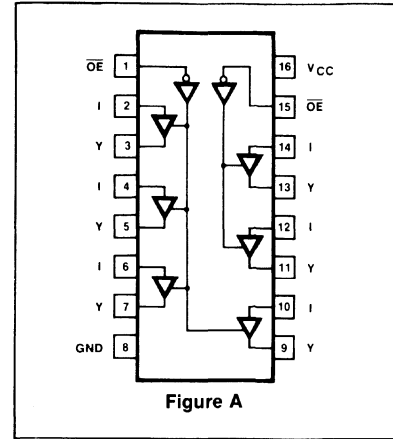
d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54/74367A (70/8097)
54LS/74LS367A
(See 8T97 for Schottky version)

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $-70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $-125^\circ C$
Plastic DIP	Fig. A	N74367AN • N74LS367AN (DM8097N)	
Ceramic DIP	Fig. A	N74367AF • N74LS367AF (DM8097J)	S54367AF • S54LS367AF (DM7097J)
Flatpak	Fig. A		S54367AW • S54LS367AW (DM7097W)

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.36
Outputs	I_{OH} (μA)	-2/-5.2 ^(a)			-1/-2.6 ^(a)
	I_{OL} (mA)	32			12/24 ^(a)

TRUTH TABLE

INPUTS		OUTPUTS
\overline{OE}	I	Y
L	L	L
L	H	H
H	X	(Z)

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
(Z) = High impedance (off) state.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}$, $V_I = 2.0V$, $V_{\overline{OE}} = V_{IL}$, $I_{OH} = \text{See above table}$	2.4						2.4		V
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$, $V_I = V_{IL}$, $V_{\overline{OE}} = V_{IL}$	$I_{OL} = 32mA$	0.4							V
		$I_{OL} = 12mA$						0.4		V
		$I_{OL} = 24mA$						0.5 ^(c)		V
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$, $V_{OUT} = 0V$	-30	-115					-30	-100	mA
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_I = 0V$, $V_{\overline{OE}} = 4.5V$		85						24	mA
I_{IL} Input LOW current when disabled	$V_{CC} = \text{Max}$, $V_{\overline{OE}} = 2.0V$ $V_I = 0.5V$		-40						-20	μA

NOTES

- The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- This parameter for Commercial range only.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 50\text{pF}$ $R_L = 400\Omega$						$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay		16						15	ns
			22						12	ns
t_{PZH}	Enable to HIGH		35						18	ns
t_{PZL}	Enable to LOW		37						24	ns
t_{PHZ}	Disable from HIGH	Waveform 6							37	ns
		Waveform 6 $C_L = 5\text{pF}^{(d)}$			11				20	ns
t_{PLZ}	Disable from LOW	Waveform 7							23	ns
		Waveform 7 $C_L = 5\text{pF}^{(d)}$			27				18	ns

NOTE

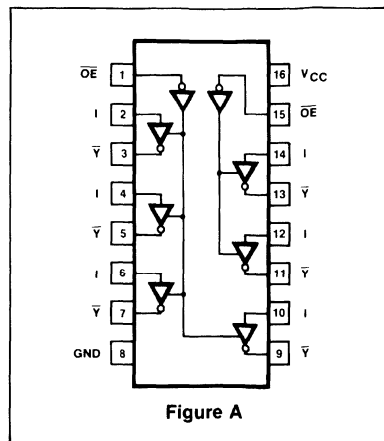
d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54/74368A (70/8098)
 54LS/74LS368A
 (See 8T98 for Schottky version)

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	Fig. A	N74368AN • N74LS368AN (DM8098N)	
Ceramic DIP	Fig. A	N74368AF • N74LS368AF (DM8098J)	S54368AF • S54LS368AF (DM7098J)
Flatpak	Fig. A		S54368AW • S54LS368AW (DM7098W)

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE ^(a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)	40			20
	I_{IL} (mA)	-1.6			-0.36
Outputs	I_{OH} (μA)	-2/-5.2 ^(a)			-1/-2.6 ^(a)
	I_{OL} (mA)	32			12/24 ^(a)

TRUTH TABLE

INPUTS		OUTPUTS
OE	I	Y
L	L	H
L	H	L
H	X	(Z)

L = LOW voltage level.
 H = HIGH voltage level.
 X = Don't care.
 (Z) = High impedance (off) state.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE ^(b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}$, $V_I = V_{IL}$, $V_{OE} = V_{IL}$, $I_{OH} = \text{See above table}$	2.4						2.4		V
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$, $V_I = 2.0V$, $V_{OE} = V_{IL}$		0.4							V
								0.4		V
								0.5 ^(c)		V
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$, $V_{OUT} = 0V$	-30	-115					-30	-100	mA
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_I = 0V$, $V_{OE} = 4.5V$		77						21	mA
I_{IL} Input LOW current when disabled	$V_{CC} = \text{Max}$, $V_{OE} = 2.0V$, $V_I = 0.5V$		-40						-20	μA

NOTES

- The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- This parameter for Commercial Range only.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 50\text{pF}$ $R_L = 400\Omega$						$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		17					10	ns
				16					12	ns
t_{PZH}	Enable to HIGH	Waveform 6		35					18	ns
t_{PZL}	Enable to LOW	Waveform 7		37					24	ns
t_{PHZ}	Disable from HIGH	Waveform 6							37	ns
		Waveform 6 $C_L = 5\text{pF}$ (d)		11					20	ns
t_{PLZ}	Disable from LOW	Waveform 7							23	ns
		Waveform 7 $C_L = 5\text{pF}$ (d)		27					18	ns

NOTE

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

54LS/74LS373

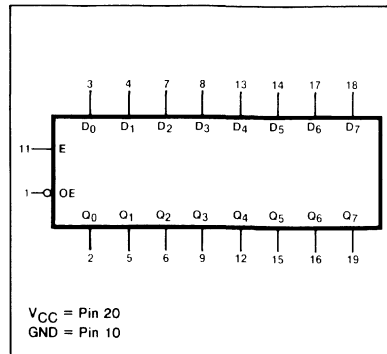
DESCRIPTION

The "373" is an 8-Bit Transparent Latch with 3-state buffered outputs. The latch outputs follow the data inputs when the latch Enable is HIGH, and they are stable when the Enable is LOW. The 3-state output buffers are controlled by an active LOW Output Enable (\overline{OE}) input. A HIGH on the \overline{OE} input forces the eight outputs to the high impedance "off" state. When \overline{OE} is LOW, the latched or transparent data appears at the outputs.

FEATURES

- 8-Bit transparent latch
- 3-State output buffers
- Common Latch Enable input with hysteresis
- Common 3-state Output Enable control
- Independent latch and 3-state buffer operation
- See "363" for MOS compatible output version

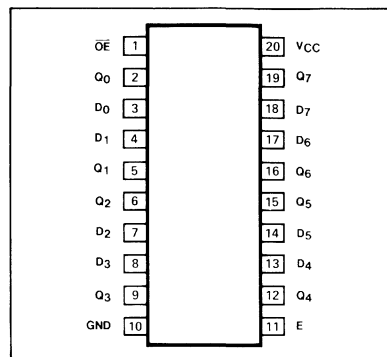
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS373N	
Ceramic DIP	N74LS373F	S54LS373F
Flatpak		

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
E	Latch Enable (active HIGH) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
D ₀ -D ₇	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{OE}	Output Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
Q ₀ -Q ₇	3-State outputs	I _{OH} (mA) I _{OL} (mA)			-1 / -2.6(a) 12 / 24(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "373" is Octal Transparent Latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

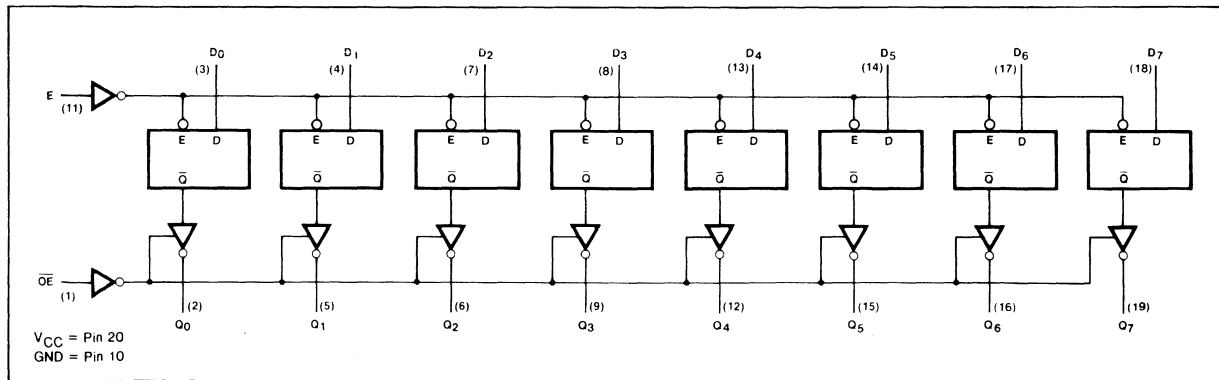
The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-state buffers independent of the latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS Q ₀ -Q ₇
	\overline{OE}	E	D _n		
Enable & read register	L	H	L	L	L
	L	H	H	H	H
Latch & read register	L	L	l	L	L
	L	L	h	H	H
Latch register & disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
 (Z) = High impedance "off" state

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} Min						0.4	V
	V _{OE} = V _{IL}						0.5 ^(c)	V
V _{OH} Output HIGH voltage	V _{CC} = Min, V _{OE} = V _{IL} I _{OH} = See Fan Out Table					2.4		V
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V					-30	-100	mA
I _{CC} Supply current	V _{CC} = Max	Mil					44	mA
		Com					40	mA

NOTES

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

c. This parameter for Commercial Range only.

AC CHARACTERISTICS: $T_A=25^{\circ}\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT	
		$C_L = 45\text{pF}$ $R_L = 667\Omega$							
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation delay						30	ns	
t_{PHL}	Latch Enable to output						40	ns	
t_{PLH}	Propagation delay						18	ns	
t_{PHL}	Data to output						32	ns	
t_{PZH}	Enable time to HIGH level						20	ns	
t_{PZL}	Enable time to LOW level						28	ns	
t_{PHZ}	Disable time from HIGH level	Figure 2						45	ns
		Figure 2, $C_L = 5\text{pF(d)}$						22	ns
t_{PLZ}	Disable time from LOW level	Figure 3						24	ns
		Figure 3, $C_L = 5\text{pF(d)}$						22	ns

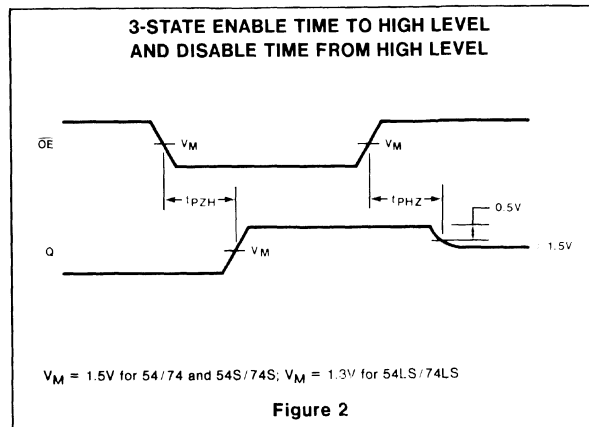
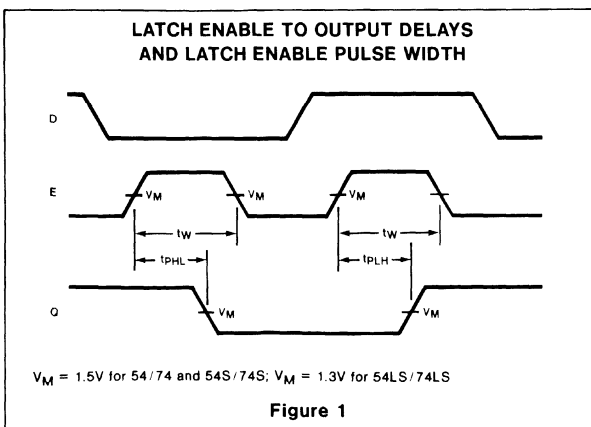
AC SETUP REQUIREMENTS: $T_A = 25^{\circ}\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W	Latch Enable pulse width					15		ns
t_S	Setup time Data to Latch Enable					3.0		ns
t_H	Hold time Data to Latch Enable					10		ns

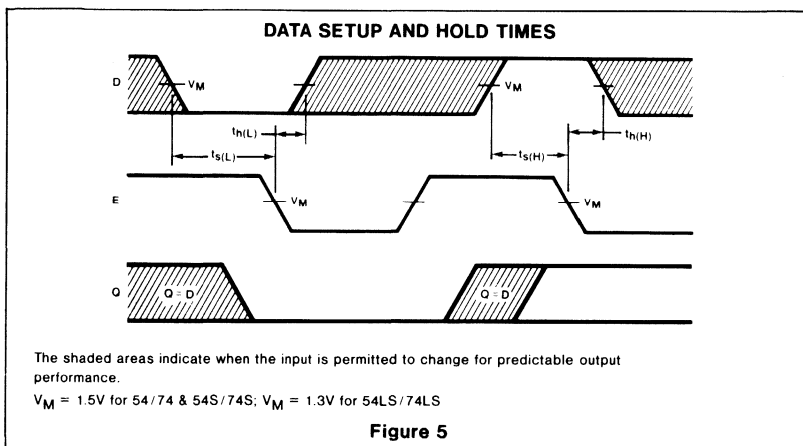
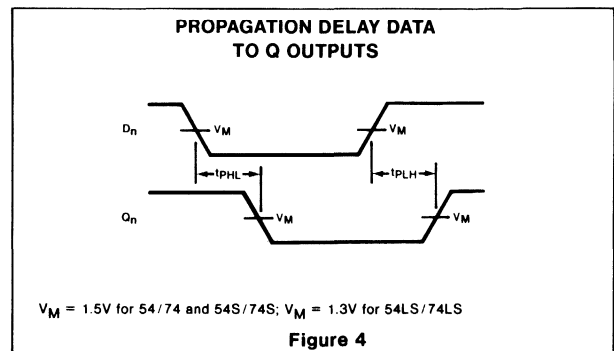
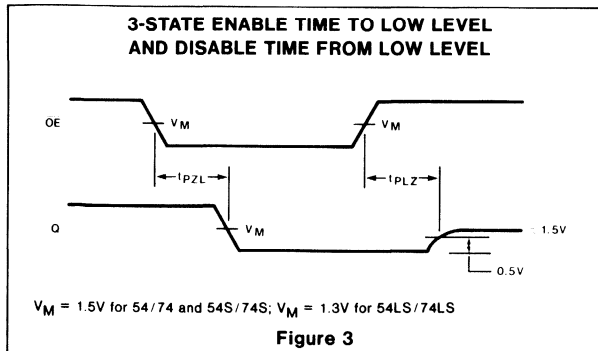
Note

d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



54LS/74LS374

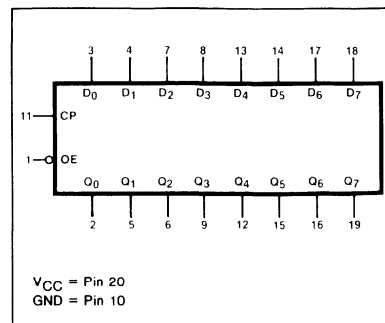
DESCRIPTION

The "374" is an Octal D Flip-Flop with 3-State buffered outputs. The device is used primarily as an 8-bit positive edge triggered storage register for interfacing with a 3-State bus. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the Clock (CP) input. The 3-State output buffers are controlled by an active LOW Output Enable (\overline{OE}) input. A HIGH on the \overline{OE} input forces the eight outputs to the high impedance "off" state. When \overline{OE} is LOW, the data in the register appears at the outputs.

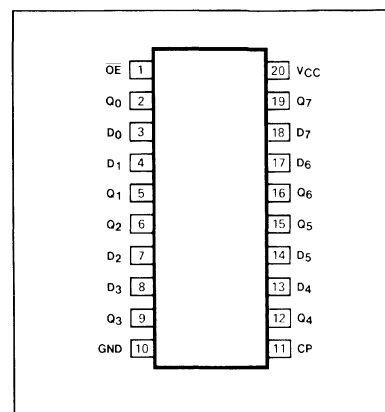
FEATURES

- 8-Bit positive edge triggered register
- 3-State output buffers
- Common Clock input with hysteresis
- Common 3-State Output Enable control
- Independent register and 3-State buffer operation
- See "364" for MOS compatible output version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS374N	
Ceramic DIP	N74LS374F	S54LS374F
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D ₀ -D ₇	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{OE}	Output Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q ₀ -Q ₇	3-State outputs	I_{OH} (mA) I_{OL} (mA)			-1 / -2.6(a) 12 / 24(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "374" is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

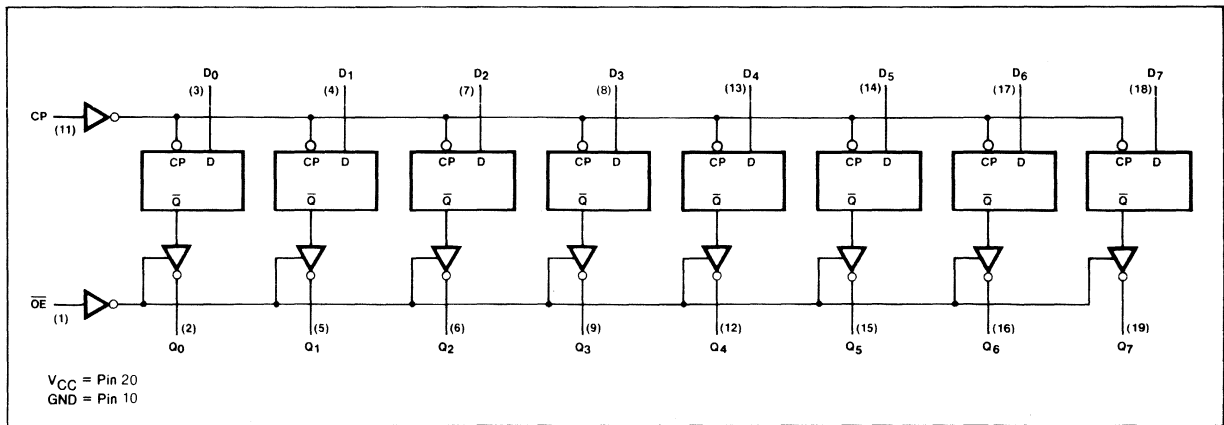
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		Q ₀ -Q ₇
Load & read register	L	↑	l	L	L
	L	↑	h	H	H
Load register & disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 (Z) = HIGH impedance "off" state
 ↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
V _{OL}	Output LOW voltage	V _{CC} = Min	I _{OL} = 12mA						0.4	V
		V _{OE} = V _{IL}	I _{OL} = 24mA						0.5 (c)	V
V _{OH}	Output HIGH voltage	V _{CC} = Min, V _{OE} = V _{IL} I _{OH} = See Fan Out Table						2.4		V
I _{OS}	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V						-30	-100	mA
I _{CC}	Supply current	V _{CC} = Max	Min						49	mA
			Com						45	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
								C _L = 45pF R _L = 667Ω		
				Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency	Figure 1						35		MHz
t _{PLH}	Propagation delay	Figure 1						28		ns
t _{PHL}	Clock to output	Figure 1						38		ns
t _{PZH}	Enable time to HIGH level	Figure 2						20		ns
t _{PZL}	Enable time to LOW level	Figure 3						28		ns
t _{PHZ}	Disable time from HIGH level	Figure 2						45		ns
		Figure 2, C _L = 5pF(d)						22		ns
t _{PLZ}	Disable time from LOW level	Figure 3						24		ns
		Figure 3, C _L = 5pF(d)						22		ns

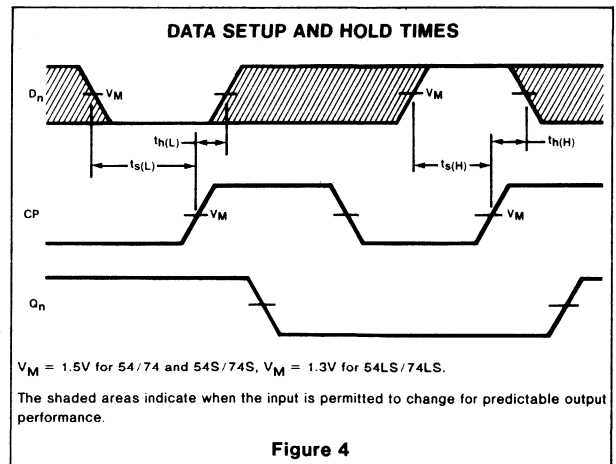
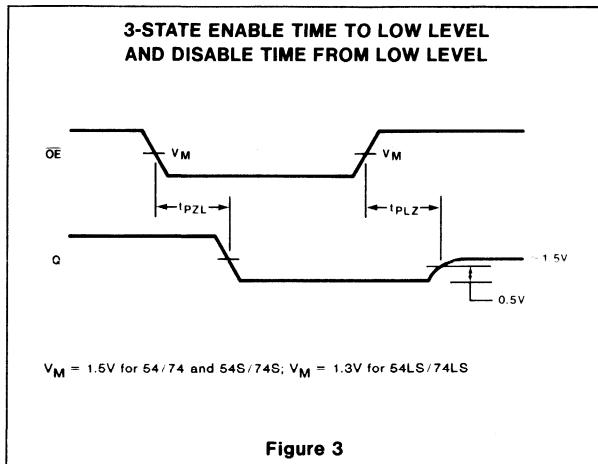
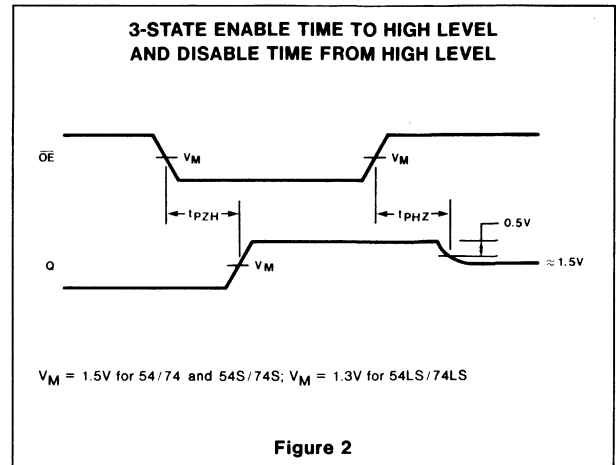
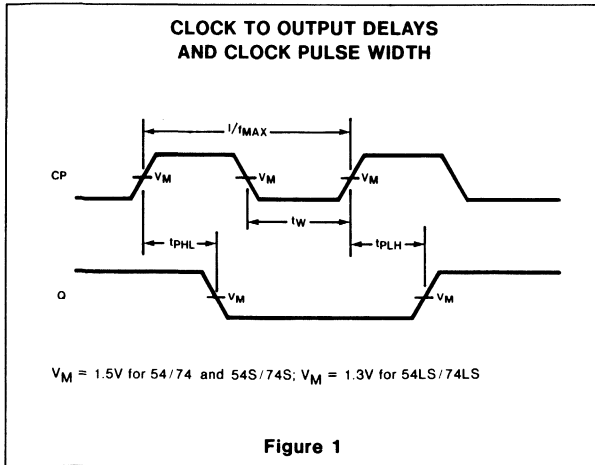
AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
t _w	Clock pulse width	Figure 1						15		ns
t _s	Setup time Data to Clock	Figure 4						10		ns
t _h	Hold time Data to Clock	Figure 4						3.0		ns

NOTES

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial Range only.
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC WAVEFORMS



54LS/74LS375

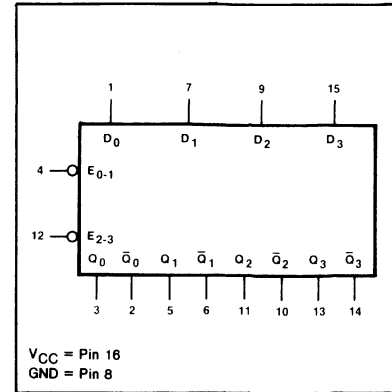
DESCRIPTION

The "375" is a Dual 2-Bit D-Latch with complementary Q and \bar{Q} outputs. Two Enable inputs are provided; each controls two latches. When the Enable (E) is HIGH, information present at a Data (D) input is transferred to the Q and \bar{Q} (inverted) outputs, and the outputs will follow the data input as long as the Enable remains HIGH. The information that is present at the data input one setup time prior to the HIGH-to-LOW Enable transition is stored in the latch until the Enable returns to a HIGH level.

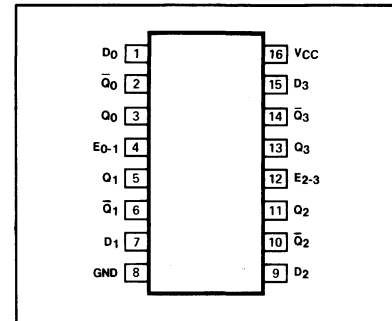
FEATURES

- 4-Bit transparent latch
- VCC and GND on corner pins
- Electrically identical to 54LS/74LS75

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS375N	
Ceramic DIP	N74LS375F	S54LS375F
Flatpak		S54LS375W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D ₀ -D ₃	Data inputs	I _{IH} (μA) I _{IL} (mA)			20 -0.4
E ₀₋₁	Enable (active LOW) input, Latches 0, 1	I _{IH} (μA) I _{IL} (mA)			80 -1.6
E ₂₋₃	Enable (active LOW) input, Latches 2, 3	I _{IH} (μA) I _{IL} (mA)			80 -1.6
Q ₀ -Q ₃	Latch outputs	I _{OH} (μA) I _{OL} (mA)			-400 4/8 (a)
\bar{Q}_0 - \bar{Q}_3	Complimentary Latch outputs	I _{OH} (μA) I _{OL} (mA)			-400 4/8 (a)

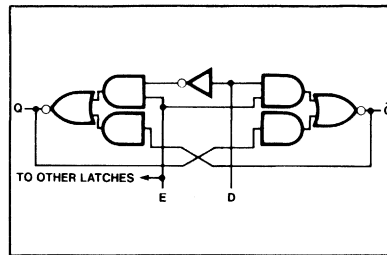
NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "375" has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the data inputs as long as E is HIGH. The data on the D inputs one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

LOGIC DIAGRAM (each latch)



MODE SELECT- FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	E	D	Q	\bar{Q}
Data Enabled	H	L	L	H
	H	H	H	L
Data Latched	L	X	q	\bar{q}

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$						12	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay Data to Q output	Figure 1						27 17	ns ns
t_{PLH} t_{PHL} Propagation delay Data to \bar{Q} output	Figure 2						20 15	ns ns
t_{PLH} t_{PHL} Propagation delay Enable to Q output	Figure 3						27 25	ns ns
t_{PLH} t_{PHL} Propagation delay Enable to \bar{Q} output	Figure 3						30 15	ns ns

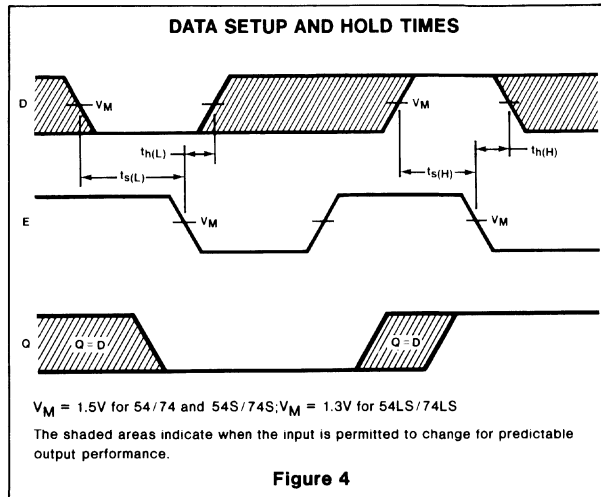
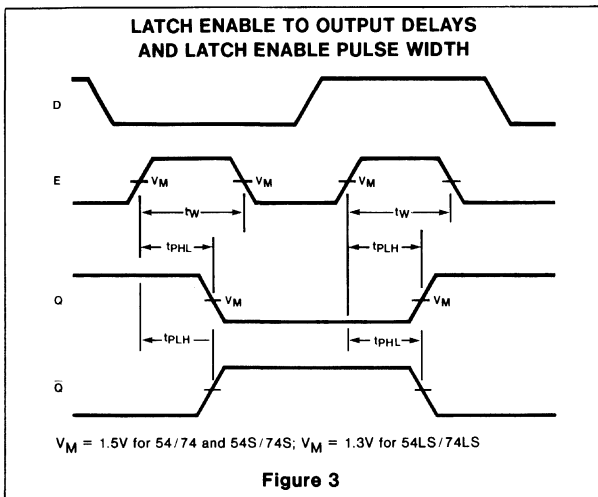
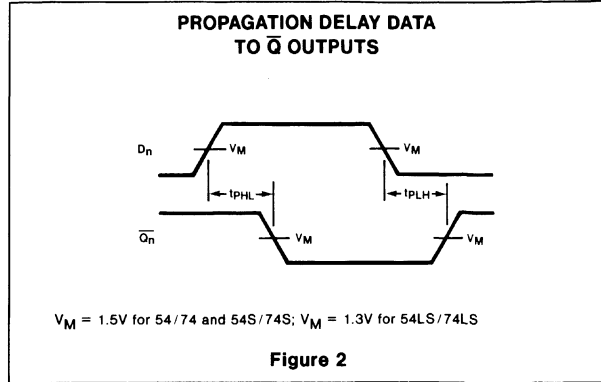
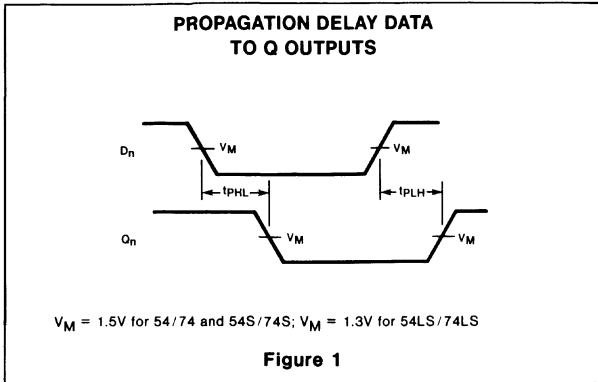
NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W Enable pulse width	Figure 3					20		ns
t_s Setup time Data to Enable	Figure 4					20		ns
t_h Hold time Data to Enable	Figure 4					0		ns

AC WAVEFORMS



54LS/74LS377

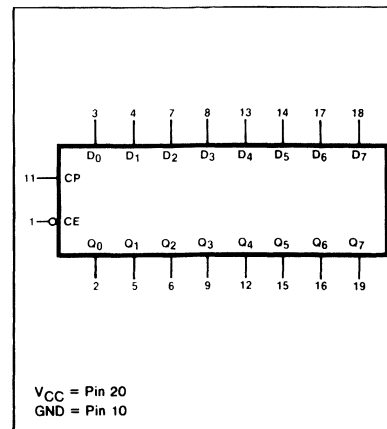
DESCRIPTION

The "377" is an Octal D Flip-Flop used primarily as an 8-bit positive-edge-triggered storage register. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the clock pulse. The device features an edge-triggered Clock Enable (CE) control for address on data synchronization applications.

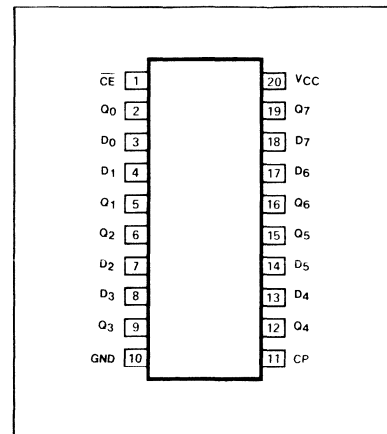
FEATURES

- Ideal for addressable register applications
- Clock Enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Slim 20-Pin plastic and ceramic DIP packages
- See "273" for Master Reset version
- See "373" for transparent latch version
- See "374" for 3-state version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS377N	
Ceramic DIP	N74LS377F	S54LS377F
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
D ₀ -D ₇	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{CE}	Clock Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
Q ₀ -Q ₇	Outputs	I _{OH} (μA) I _{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "377" has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

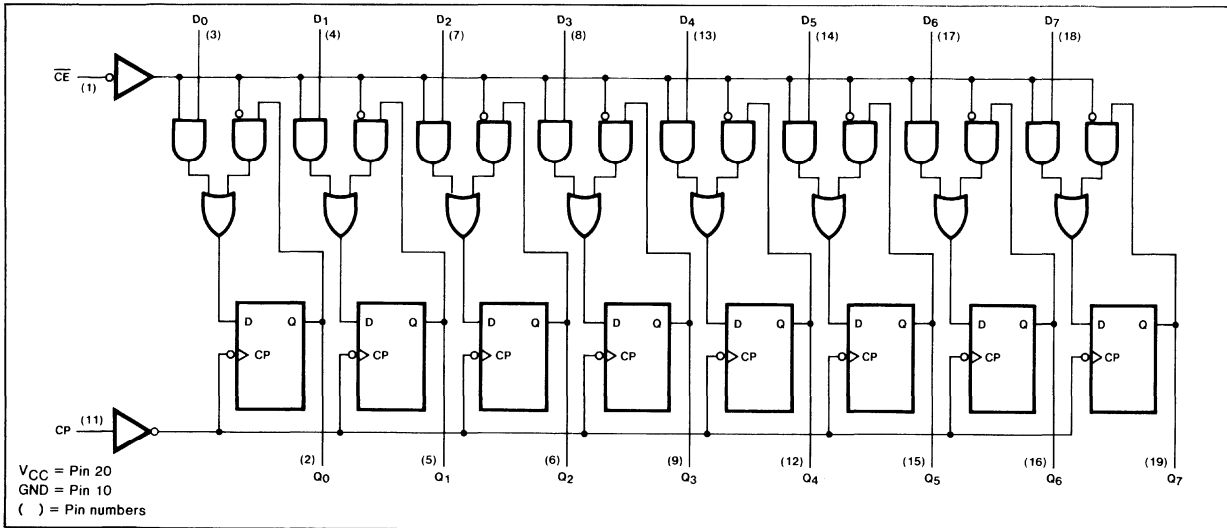
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input is also edge-triggered, and must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	\overline{CE}	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$						28	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

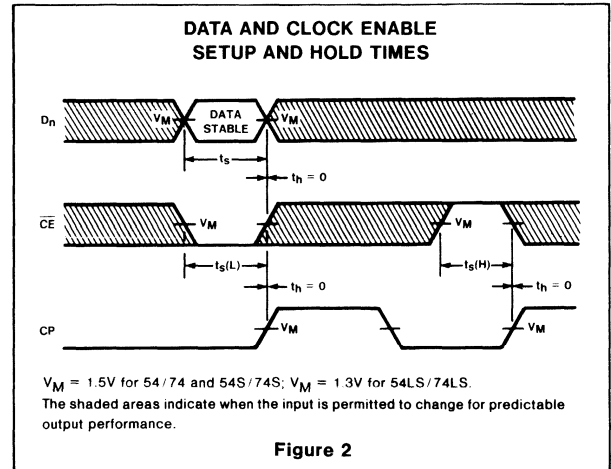
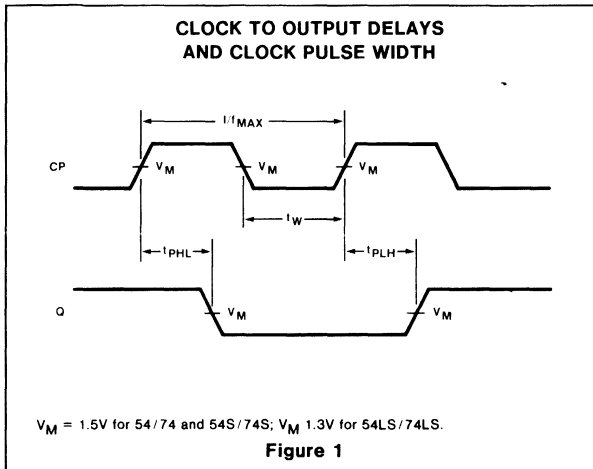
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Figure 1					30		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Figure 1					21 23		ns ns

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Figure 1					20		ns
t_s Setup time Data to CP	Figure 2					20		ns
t_h Hold time Data to CP	Figure 2					0		ns
t_s Setup time \overline{CE} to CP	Figure 2					20		ns
t_h Hold time \overline{CE} to CP	Figure 2					0		ns

AC WAVEFORMS



54LS/74LS378

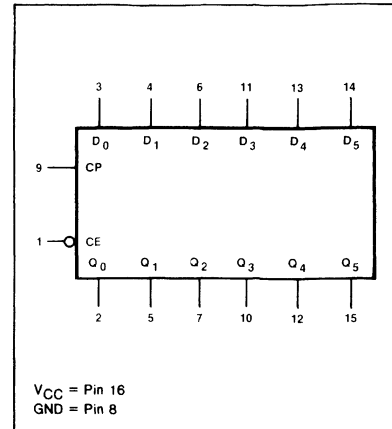
DESCRIPTION

The "378" is a Hex D Flip-Flop used primarily as a 6-bit positive-edge-triggered storage register. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the clock pulse. The device features on edge-triggered Clock Enable (CE) control for address or data synchronization applications.

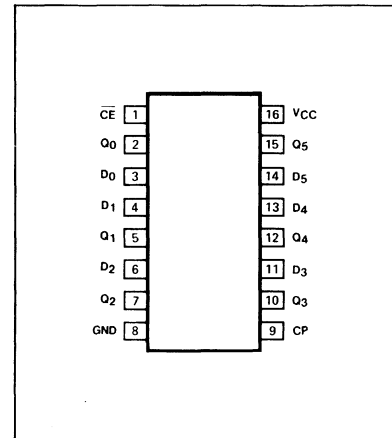
FEATURES

- Ideal for addressable register applications
- Six edge-triggered D flip-flops
- Buffered common clock
- Clock Enable for address and data synchronization applications
- See "174" for Master Reset version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +70°C	MILITARY RANGES V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS378N	
Ceramic DIP	N74LS378F	S54LS378F
Flatpak		S54LS378W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _H (μA) I _L (mA)			20 -0.4
D ₀ -D ₅	Parallel Data inputs	I _H (μA) I _L (mA)			20 -0.4
CE	Clock Enable (active LOW) input	I _H (μA) I _L (mA)			20 -0.4
Q ₀ -Q ₅	Outputs	I _{OH} (μA) I _{OL} (mA)			-400 4/8(a)

NOTE
a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "378" has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

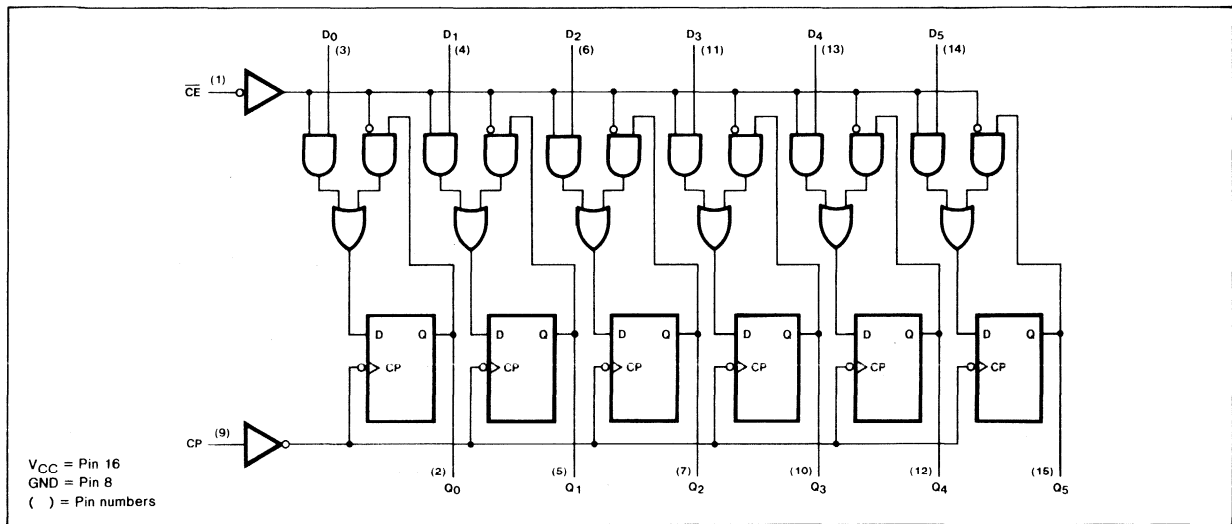
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input is also edge-triggered, and must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	\overline{CE}	D _n	Q _n
Load "1"	↑	L	h	H
Load "0"	↑	L	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						24	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

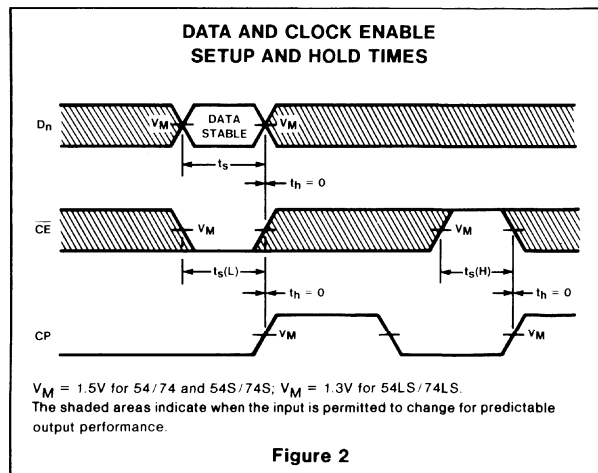
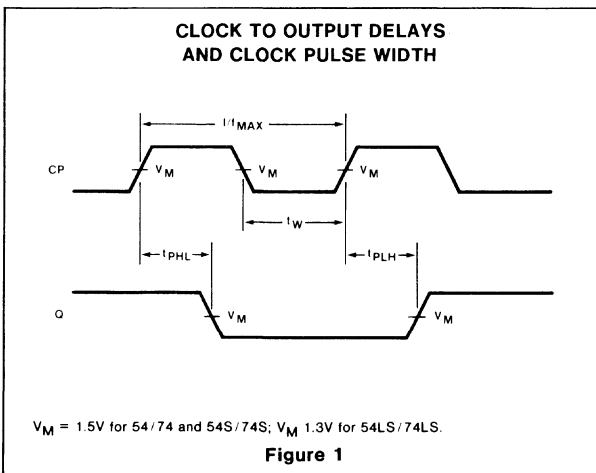
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1					30		MHz
t _{PLH} Propagation delay	Figure 1					21		ns
t _{PHL} Clock to output						23		ns

NOTE
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Figure 1					20		ns
t_s Setup time Data to CP	Figure 2					20		ns
t_h Hold time Data to CP	Figure 2					0		ns
t_s Setup time \overline{CE} to CP	Figure 2					20		ns
t_h Hold time \overline{CE} to CP	Figure 2					0		ns

AC WAVEFORMS



54LS/74LS379 (Preliminary data)

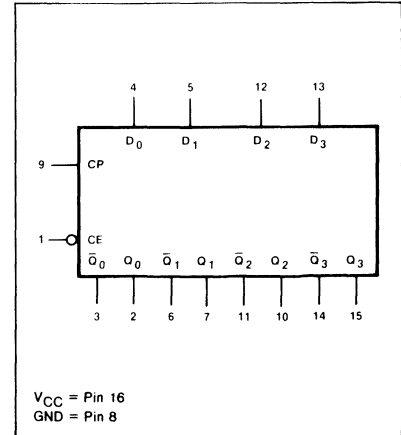
DESCRIPTION

The "379" is a Quad edge-triggered D Flip-Flop with a common buffered clock and an edge-triggered Clock Enable input. Data on the D inputs is transferred to storage during the LOW-to-HIGH transition of the clock pulse. Each flip-flop has both true (Q) and complement (\bar{Q}) outputs useful for general purpose flip-flop applications and simple latch/decoding schemes.

FEATURES

- Four edge-triggered D flip-flops
- Both true and complement outputs
- Clock Enable for address and data synchronization applications
- Buffered common clock
- See "175" for Master Reset version

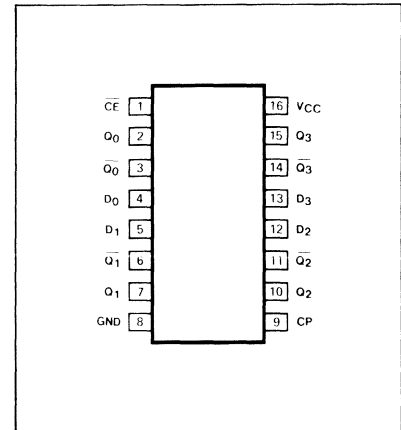
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS379N	
Ceramic DIP	N74LS379F	S54LS379F
Flatpak		S54LS379W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
D ₀ -D ₃	Parallel Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\bar{CE}	Clock Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q ₀ -Q ₃	True outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)
\bar{Q}_0 - \bar{Q}_3	Complement outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE
a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "379" is a quad edge-triggered D-type flip-flop with individual D inputs and both Q and \bar{Q} outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\bar{CE}) is LOW.

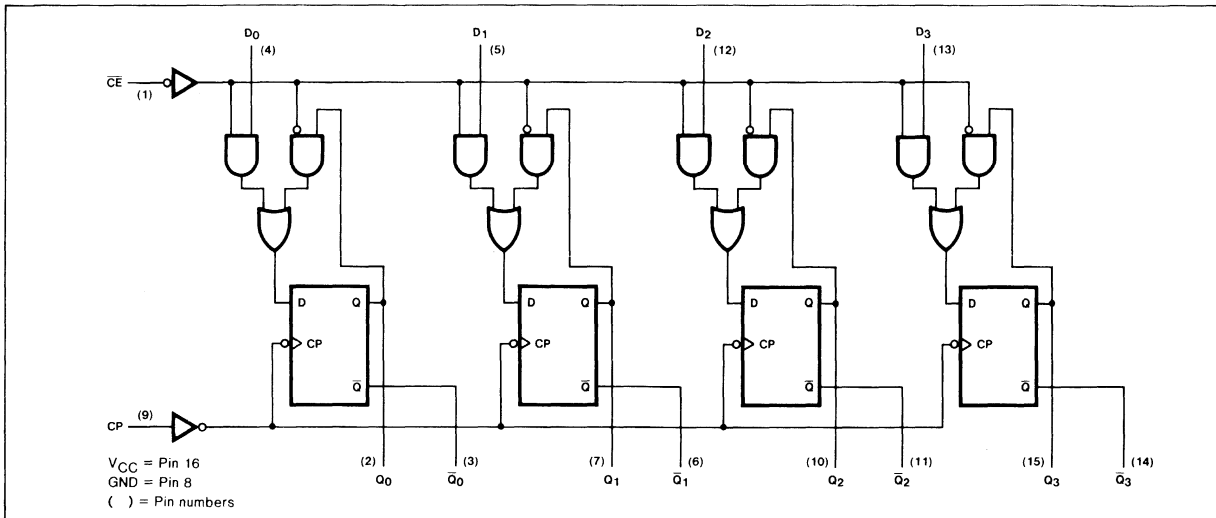
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \bar{CE} input is also edge-triggered, and must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	CP	\bar{CE}	D _n	Q _n	\bar{Q}_n
Load "1"	↑	L	h	H	L
Load "0"	↑	L	L	L	H
Hold (do nothing)	↑	h	X	no change	
	X	H	X	no change	

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						15	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

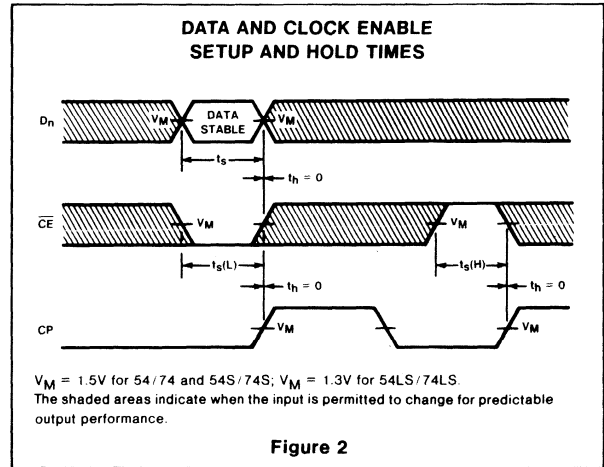
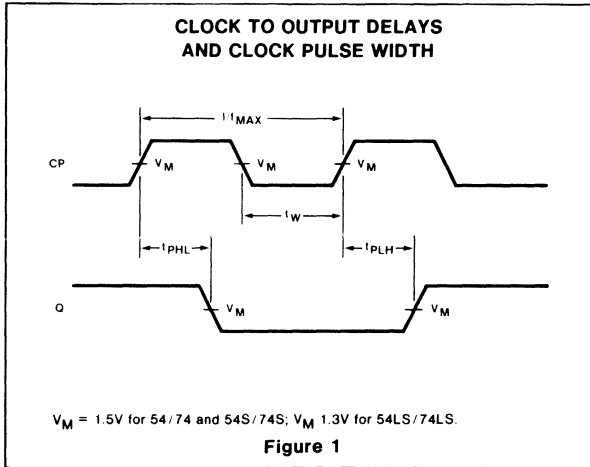
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1					30		MHz
t _{PLH} Propagation delay	Figure 1						27	ns
t _{PHL} Clock to output							27	ns

NOTE
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Figure 1					20		ns
t_s Setup time Data to CP	Figure 2					20		ns
t_h Hold time Data to CP	Figure 2					0		ns
t_s Setup time \overline{CE} to CP	Figure 2					20		ns
t_h Hold time \overline{CE} to CP	Figure 2					0		ns

AC WAVEFORMS



54LS/74LS386

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N74LS386N	
Ceramic DIP	Fig. A	N74LS386F	S54LS386F
Flatpak	Fig. A		S54LS386W

PIN CONFIGURATION

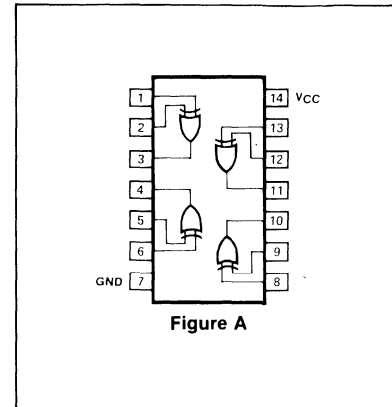


Figure A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA)				40
	I_{IL} (mA)				-0.6
Outputs	I_{OH} (μA)				-400
	I_{OL} (mA)				$4/8^{(a)}$

TRUTH TABLE (Each gate)

INPUTS		OUTPUT
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$								10	mA

AC CHARACTERISTICS $T_A = 25^\circ C$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 2 Other input LOW								23 17	ns ns
t_{PLH} t_{PHL} Propagation delay	Waveform 1 Other input HIGH								30 22	ns ns

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.

54LS/74LS390

DESCRIPTION

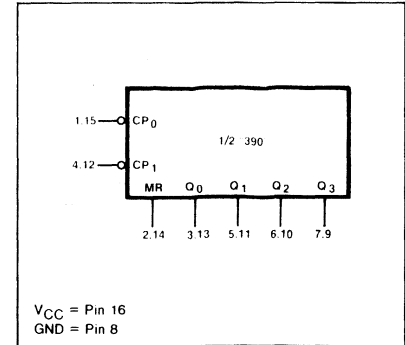
The "390" is a Dual Decade Ripple Counter divided into four sections. The counter has two divide-by-two sections and two divide-by-five sections. The normal configuration for the device is two BCD decade, or two bi-quinary counters, but the four sections can be configured in any combination as long as the Master Resets can also be combined. Each section is triggered by the HIGH-to-LOW transition of the clock inputs.

The Master Resets (MR_a & MR_b) are active HIGH asynchronous inputs which clear the two decade counters defined by the "a" and "b" suffixes in the Pin Configuration.

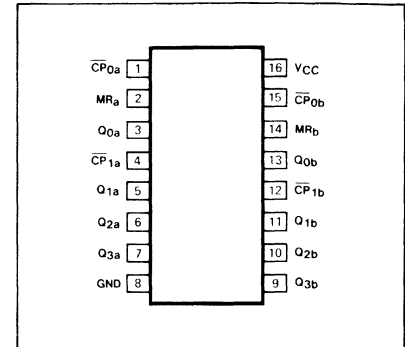
FEATURES

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2,4,,5, 10,20,25,50 or 100
- Two Master Resets to clear each decade counter individually

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N74LS390N	
Ceramic DIP	N74LS390F	S54LS390F
Flatpak		S54LS390W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54 / 74	54S / 74S	54LS / 74LS
\overline{CP}_0	Clock (active LOW going edge) inputs to $\div 2$ sections	I_{IH} (μA) I_{IL} (mA)			100 -1.6
\overline{CP}_1	Clock (active LOW going edge) inputs to $\div 5$ sections	I_{IH} (μA) I_{IL} (mA)			200 -2.4
MR	Master Reset (active HIGH) inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q_0 - Q_3	Counter outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "390" is Dual 4-Bit Decade Ripple Counter divided into four separately clocked sections. The counter has two divide-by-two sections and two divide-by-five sections. These sections are normally used in a BCD decade or a bi-quinary configuration, since they share a common Master Reset input. If the two Master Resets can be used to simultaneously clear all 8-bits of the counter, a number of counting configurations are possible within one package. The separate clocks of each section allow ripple counter or frequency division applications of divide by 2, 4, 5, 10, 20, 25, 50 or 100.

Each section is triggered by the HIGH-to-LOW transition of the Clock (\overline{CP}) inputs. For BCD decade operation, the Q_0 output is connected to the \overline{CP}_1 input of the divide-by-five section. For bi-quinary decade operation (50% duty cycle output), the Q_3 output is connected to the \overline{CP}_0 input, and Q_0 becomes the decade output.

The Master Resets (MR_a & MR_b) are active HIGH asynchronous inputs to each decade counter which operate on the portion of the counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clocks and sets the four outputs LOW.

BCD COUNT SEQUENCE

For 1/2 the "390"

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE

Output Q_0 is connected to Input \overline{CP}_1 with counter input on \overline{CP}_0 .

BI-QUINARY COUNT SEQUENCE

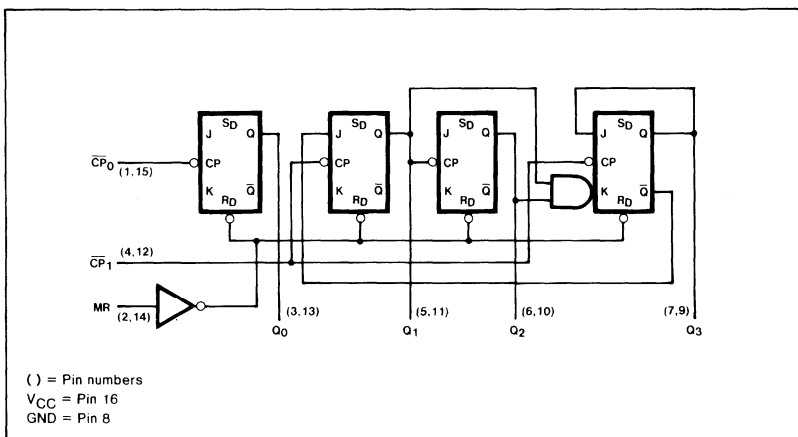
For 1/2 the "390"

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

NOTE

Output Q_3 is connected to input \overline{CP}_0 with counter input on \overline{CP}_1 .

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$						26	mA

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} $\overline{\text{CP}}_0$ input count frequency	Figure 1					35		MHz
f_{MAX} $\overline{\text{CP}}_1$ input count frequency	Figure 1					20		MHz
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_0$ to Q_0	Figure 1					20	20	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_0$ to Q_2	Figure 1					60	60	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_1$ to Q_1 or Q_3	Figure 1					21	21	ns
t_{PLH} t_{PHL} Propagation delay $\overline{\text{CP}}_1$ to Q_2	Figure 1					39	39	ns
t_{PHL} Propagation delay MR to Q	Figure 2						35	ns

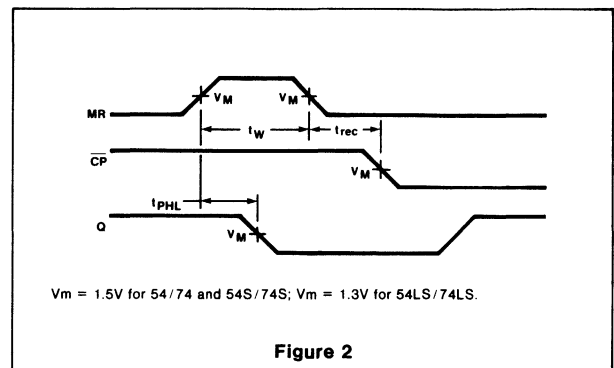
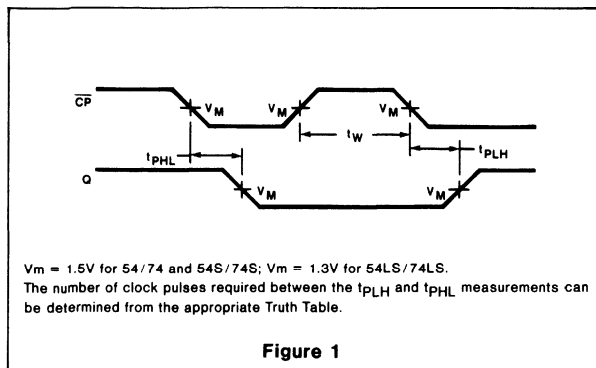
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W $\overline{\text{CP}}_0$ pulse width	Figure 1					15		ns
t_W $\overline{\text{CP}}_1$ pulse width	Figure 1					25		ns
t_W MR pulse width	Figure 2					35		ns
t_{rec} Recovery time MR to $\overline{\text{CP}}$	Figure 2					20		ns

Note

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



54LS/74LS393

DESCRIPTION

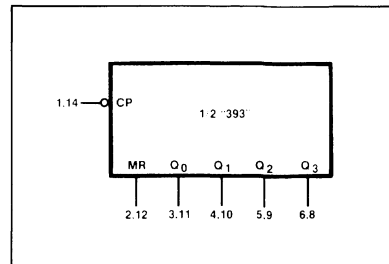
The "393" is a Dual 4-Bit Binary Ripple Counter. Each 4-bit counter is triggered by the HIGH-to-LOW transition of the clock inputs. The ripple type construction means that the output from each stage is internally connected as the clock input for the succeeding stage.

The Master Resets (MR_a & MR_b) are active HIGH asynchronous inputs which clear the two 4-bit counters defined by the "a" and "b" suffixes in the Pin Configuration.

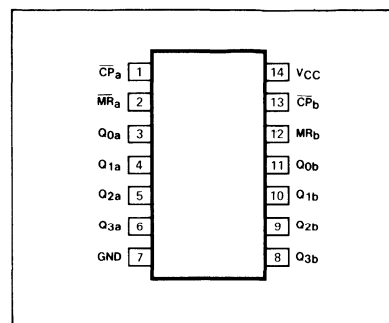
FEATURES

- Two 4-bit binary counters
- Divide-by any binary module up to 28 in one package
- Two Master Resets to clear each 4-bit counter individually

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N74LS393N	
Ceramic DIP	N74LS393F	S54LS393F
Flatpak		S54LS393W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}	Clock (active LOW going edge) inputs to each 4-Bit binary counter	I_{IH} (μA) I_{IL} (mA)			100 -1.6
MR	Master Reset (active HIGH) inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q_0-Q_3	Counter outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

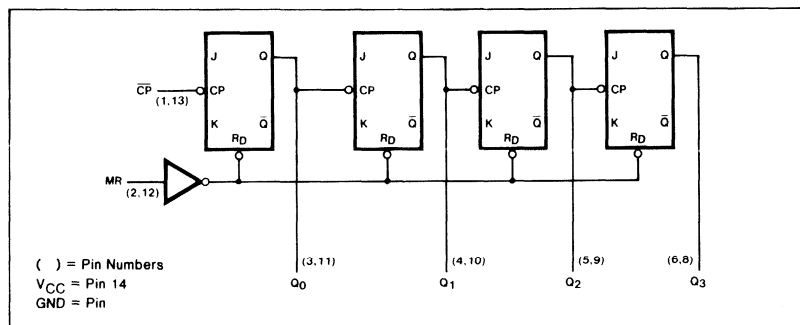
The "393" is a Dual 4-Bit Binary Ripple Counter with separate Clock and Master Reset inputs to each counter. The operation of each half of the "393" is the same as the "93" except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the Clock (CP_a & \overline{CP}_b) inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs are designed to drive the internal flip-flops plus the rated fan-out of the device. The outputs of the ripple counter do not change synchronously, and should not be used for high speed address decoding.

The Master Resets (MR_a & MR_b) are active HIGH asynchronous inputs to each 4-bit counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clock and sets the outputs LOW.

COUNT SEQUENCE FOR 1/2 THE "393"

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						26	ma

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

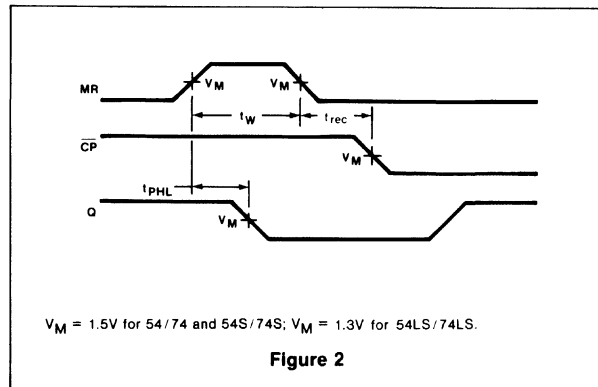
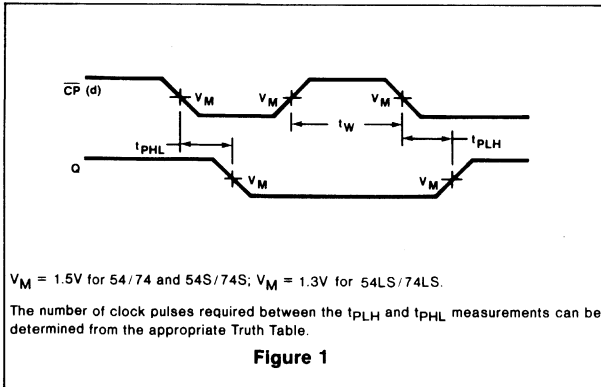
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						$C_L = 15\text{pf}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} $\overline{\text{CP}}$ input count frequency	Figure 1					35		MHz
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CP}}$ to Q_0	Figure 1					20	20	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CP}}$ to Q_3	Figure 1					60	60	ns
t_{PHL} Propagation delay MR to Q	Figure 2					39		ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W $\overline{\text{CP}}$ pulse width	Figure 1					15		ns
t_W MR pulse width	Figure 2					20		ns
t_{rec} Recovery time MR to $\overline{\text{CP}}$	Figure 2					20		ns

AC WAVEFORMS



54LS/74LS395A

DESCRIPTION

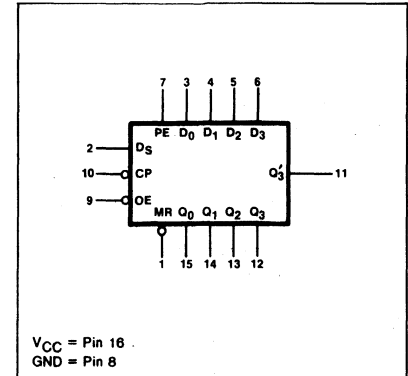
The "395" is a 4-Bit Shift Register with serial and parallel synchronous operating modes, and independent 3-state output buffers. The active HIGH Parallel Enable (PE) input determines the parallel load or shift right operating modes. The PE and data inputs are edge-triggered, responding only to the HIGH-to-LOW transition of the Clock (CP) input. The Master Reset (MR) is an asynchronous active LOW input. When LOW, the MR input overrides the clock and clears the register.

The 3-state output buffers are controlled by an active LOW Output Enable (OE) input. A HIGH on the OE input forces all four outputs to the high impedance "off" state. When OE is LOW, the data in the register appears at the outputs. The output from the last state (Q3) is available for serial expansion with-out interfering with the 3-state buffer operation.

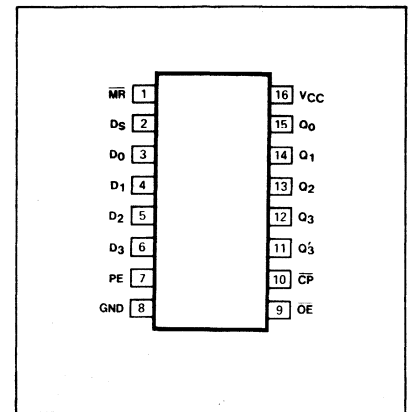
FEATURES

- 4-Bit parallel load shift register
- Independent 3-state buffer outputs
- Separate Q3 output for serial expansion
- Asynchronous Master Reset

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	VCC=5V ± 5%; TA=0°C to +70°C	VCC=5V ± 10%; TA=-55°C to +125°C
Plastic DIP	N74LS395AN	
Ceramic DIP	N74LS395AF	S54LS395AF
Flatpak		S54LS395AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active LOW going edge) input	I _{IH} (μA) I _{IH} (mA)			20 -0.4
D ₀ -D ₃	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)			20 -0.4
D _S	Serial Data input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
PE	Parallel Enable input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
OE	Output Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
MR	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
Q ₀ -Q ₃	3-State outputs	I _{OH} (mA) I _{OL} (mA)			-1/-2.6(a) 12/24(a)
Q ₃	Serial output from last stage	I _{OH} (μA) I _{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "395" is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs (D₀-D₃) into the register synchronous with the HIGH-to-LOW transition of the Clock input (\overline{CP}). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q₀ flip-flop, and the data in the register is shifted one bit to the right in the direction (Q₀ → Q₁ → Q₂ → Q₃) synchronous with the negative clock transition. The PE and data inputs are fully edge triggered and must be stable only one set-up prior to the HIGH-to-LOW transition of the Clock.

The Master Reset (\overline{MR}) is an asynchronous active LOW input. When LOW, the \overline{MR} overrides the clock and all other inputs and clears the register.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads. The active LOW Output Enable (\overline{OE}) controls all four 3-state buffers independent of the register operation. The data in the register appears at the outputs when \overline{OE} is LOW. The outputs are in the high impedance "off" state, which means they will neither drive nor load the bus when \overline{OE} is HIGH. The output from the last stage is brought out separately. This output (Q₃) is tied to the Serial Data input (D_S) of the next register for serial expansion applications. The Q₃ output is not affected by the 3-state buffer operation.

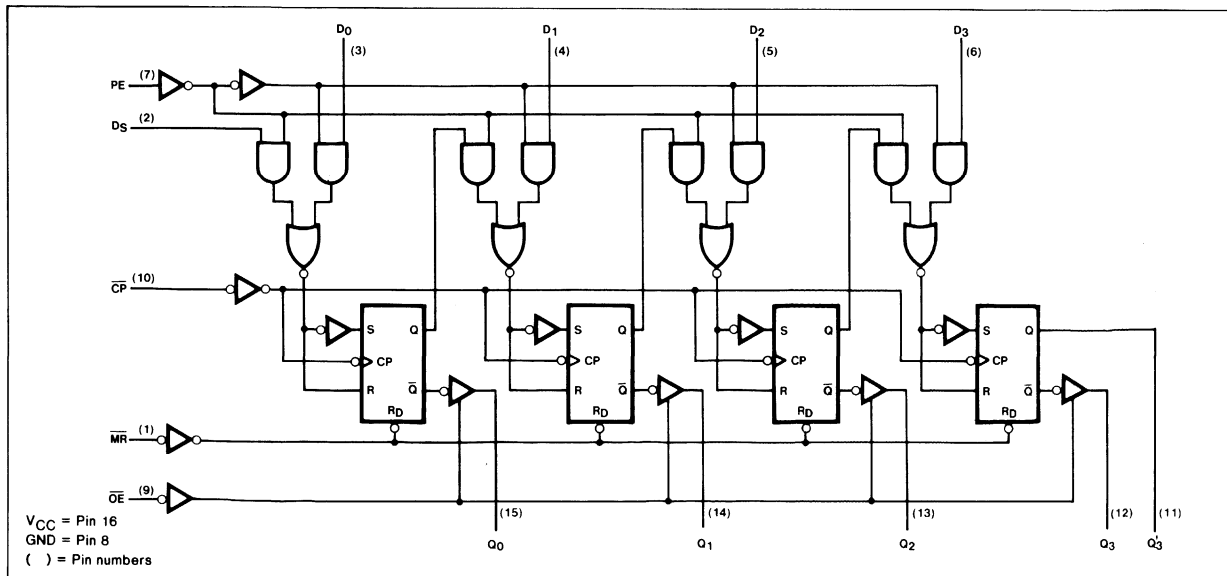
MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODE	INPUTS					OUTPUTS			
	\overline{MR}	\overline{CP}	PE	D _S	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	↓	l	l	X	L	q ₀	q ₁	q ₂
	H	↓	l	h	X	H	q ₀	q ₁	q ₂
Parallel load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	\overline{OE}	Q _n (register)	Q ₀ , Q ₁ , Q ₂ , Q ₃	Q ₃
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	(Z)	L
	H	H	(Z)	H

- H = HIGH voltage level
- h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
- L = LOW voltage level
- l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition
- q_n = Lower letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition
- X = Don't care
- (Z) = High impedance "off" state
- ↓ = HIGH-to-LOW transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH voltage, buffer outputs V _{CC} = Min, V _{OE} = V _{IL} I _{OH} = See Fan Out Table					2.4		V
V _{OL}	Output LOW voltage, buffer outputs V _{CC} = Min, V _{OE} = V _{IL}		I _{OL} = 12mA				0.4	V
			I _{OL} = 24mA				0.5 (c)	V
I _{OS}	Output short circuit current, buffer outputs V _{CC} = Max, V _{OUT} = 0V					-30	-100	mA
I _{CC}	Supply current V _{CC} = Max						34	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 45pF R _L = 667Ω						
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum clock frequency Figure 1					30		MHz
t _{PLH} t _{PHL}	Propagation delay Clock to buffer outputs Figure 1					30 30		ns ns
t _{PLH} t _{PHL}	Propagation delay Clock to Q ₃ output Figure 1 R _L = 2kΩ, C _L = 15pF					30 30		ns ns
t _{PHL}	Propagation delay \overline{MR} to output Figure 2						35	ns
t _{PZH}	Enable time to HIGH level Figure 3						25	ns
t _{PZL}	Enable time to LOW level Figure 4						25	ns
t _{PHZ}	Disable time from HIGH level Figure 3						35	ns
	Figure 3, C _L = 5pF (d)						17	ns
t _{PLZ}	Disable time from LOW level Figure 4						25	ns
	Figure 4, C _L = 5pF (d)						20	ns

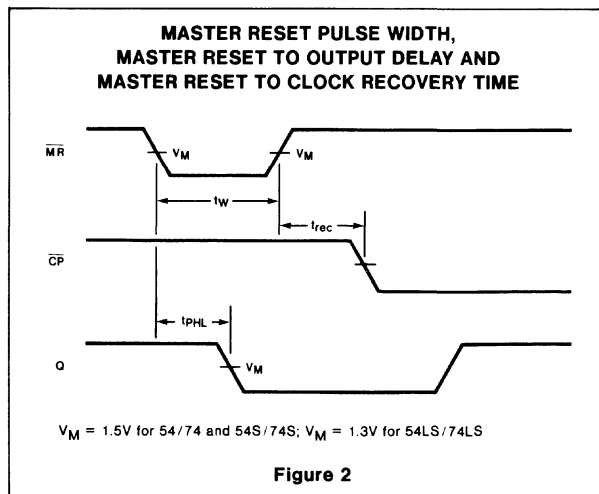
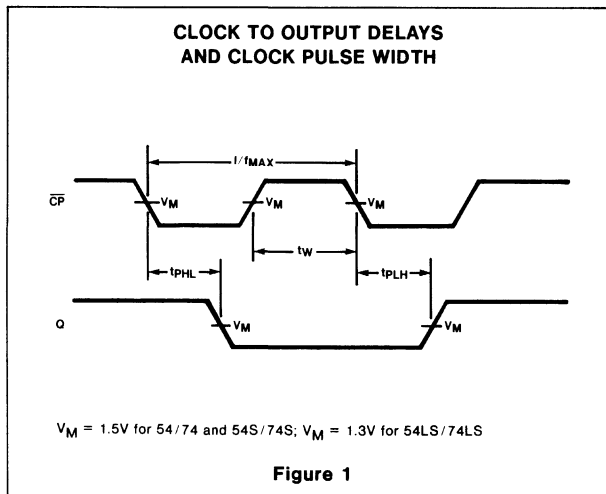
NOTES

- b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- c. This parameter for Commercial range only
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

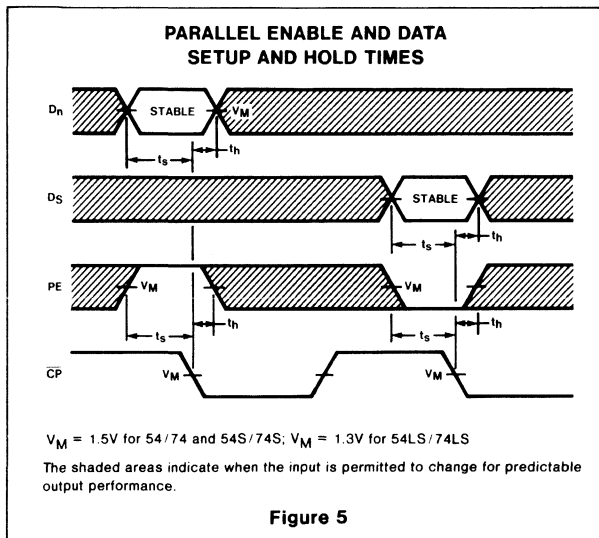
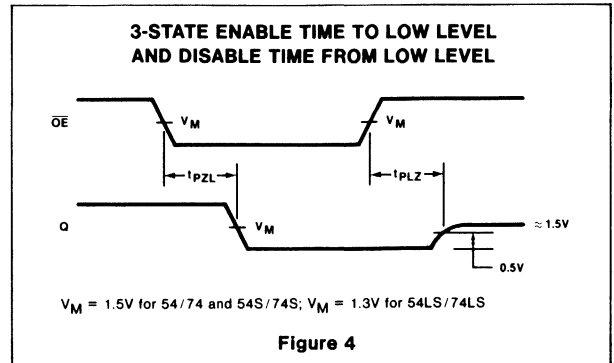
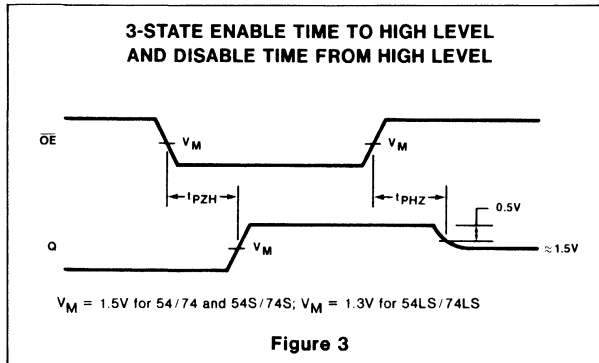
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W Clock pulse width	Figure 1					25		ns
t_W Master Reset pulse width	Figure 2					25		ns
t_s Setup time Data to clock	Figure 5					20		ns
t_h Hold time Data to clock	Figure 5					5.0		ns
t_s Setup time PE to clock	Figure 5					20		ns
t_h Hold time PE to clock	Figure 5					5.0		ns
t_{rec} Recovery time \overline{MR} to clock	Figure 2					30		ns

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



54LS/74LS398 (Preliminary data)

DESCRIPTION

The "398" is a Quad 2-Port Register with true and complement outputs. It combines the functions of a quad 2-input multiplexer and four positive edge triggered flip-flops. The state of the common Select input (S) determines the source of data loaded into the four flip-flops synchronous with the LOW-to-HIGH transition of the common buffered Clock (CP).

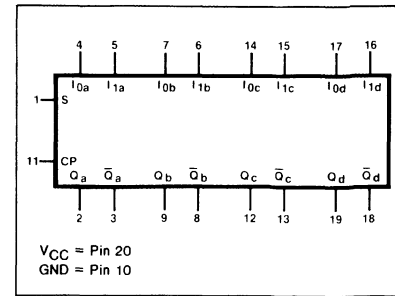
FEATURES

- Fully synchronous operation
- Select from two data sources
- True and complement outputs available
- See "298" for negative edge triggered version
- Available in 20-Pin space saving package

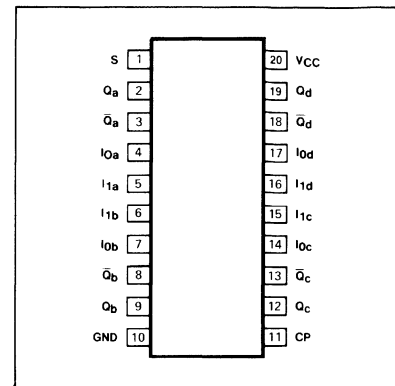
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS398N	
Ceramic DIP	N74LS398F	S54LS398F
Flatpak		

LOGIC SYMBOL



PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
S	Common Select input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
I _{0a} -I _{0d}	Data inputs from Source "0"	I _{IH} (μA) I _{IL} (mA)			20 -0.4
I _{1a} -I _{1d}	Data inputs from Source "1"	I _{IH} (μA) I _{IL} (mA)			20 -0.4
Q _a -Q _d	Register outputs	I _{OH} (μA) I _{OL} (mA)			-400 4/8(a)
Q _a -Q _d	Complementary Register outputs	I _{OH} (μA) I _{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "398" is a high speed Quad 2-Port Register. It selects four bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is loaded into four edge triggered flip-flops synchronous with the LOW-to-HIGH transition of the common buffered Clock input (CP). The four flip-flops are combined to form a synchronous 4-bit register with both true and complement outputs available.

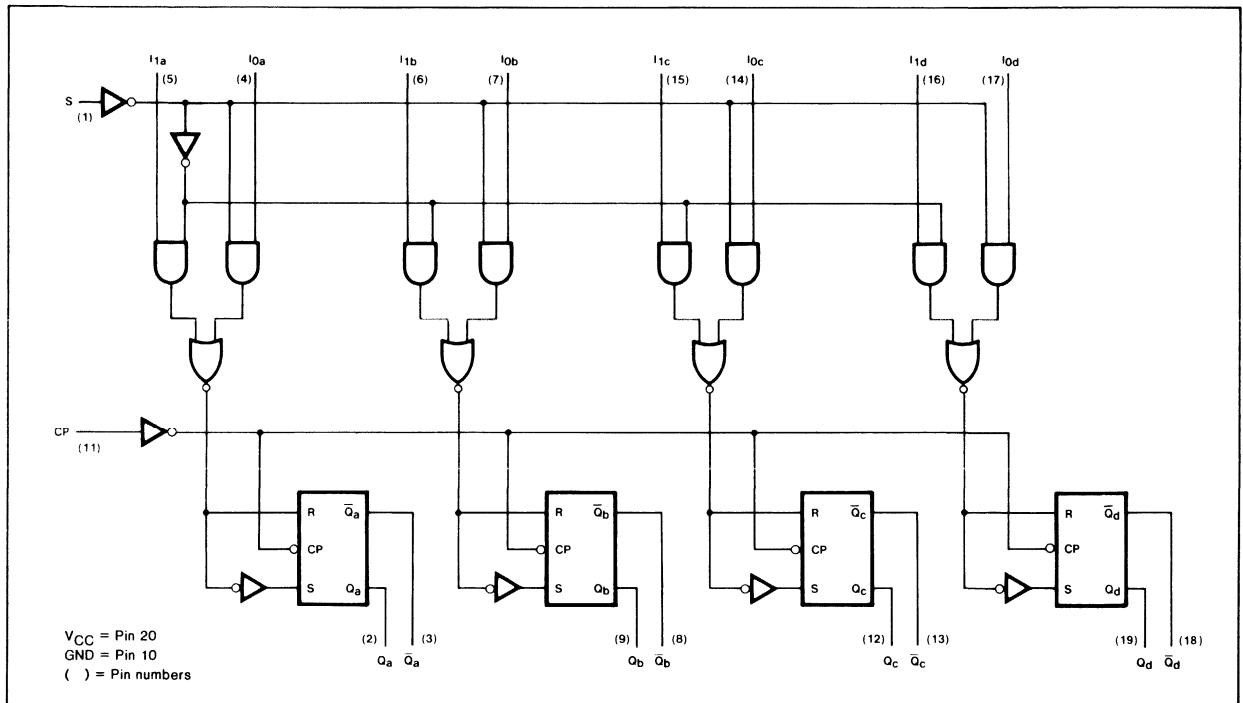
The operation of the device is fully synchronous. The Data inputs (I_0 & I_1) and the Select input (S) must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	CP	S	I_0	I_1	Q_n	\bar{Q}_n
Load Source "0"	↑	l	l	X	L	H
	↑	l	h	X	H	L
Load Source "1"	↑	h	X	l	L	H
	↑	h	X	h	H	L

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$						13	mA

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

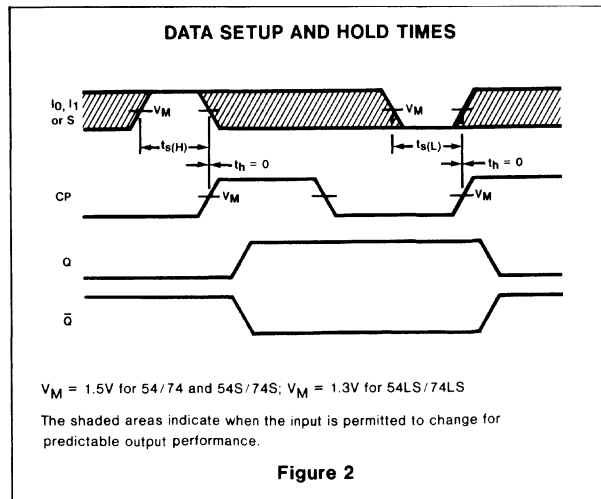
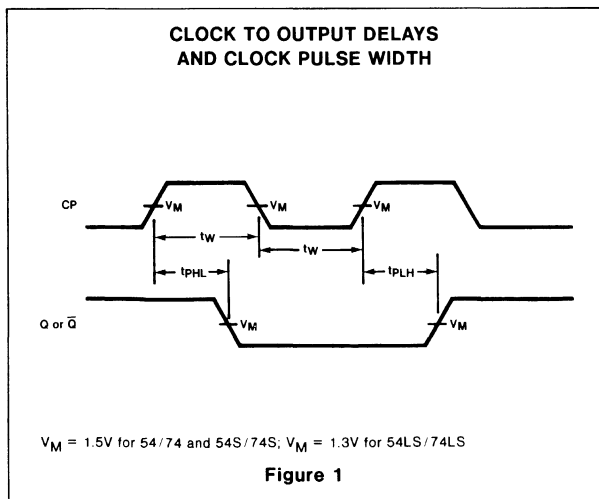
AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$						
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Figure 1						27	ns
t_{PHL} Clock to output							32	ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W Clock pulse width	Figure 1					20		ns
t_S Setup time Data to Clock	Figure 2					20		ns
t_H Hold time Data to Clock	Figure 2					0		ns
t_S Setup time Select to Clock	Figure 2					25		ns
t_H Hold time Select to Clock	Figure 2					0		ns

AC WAVEFORMS



54LS/74LS399 (Preliminary data)

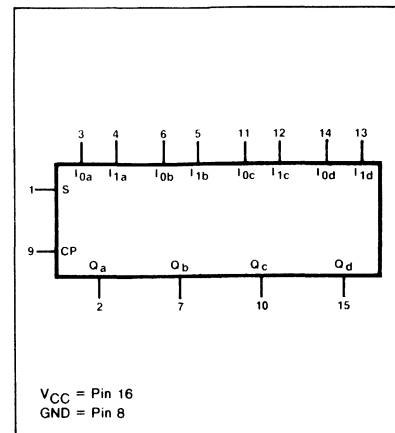
DESCRIPTION

The "399" is a Quad 2-Port Register which combines the functions of a quad 2-input multiplexer and a 4-bit positive edge triggered register. The state of the common Select input (S) determines the source of the data loaded into the register synchronous with the LOW-to-HIGH Clock (CP) transition.

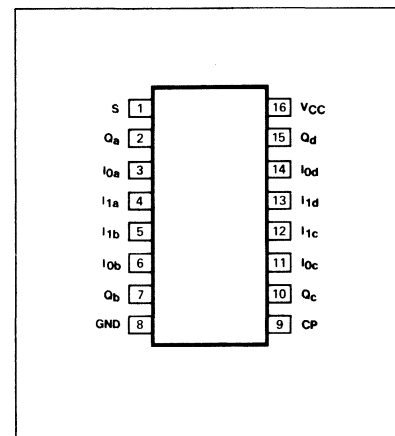
FEATURES

- Fully synchronous operation
- Select from two data sources
- Buffered, positive edge triggered clock
- See "398" for true and complement output version
- See "298" for negative edge triggered version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS399N	
Ceramic DIP	N74LS399F	S54LS399F
Flatpak		S54LS399W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
S	Common Select input	I_{IH} (μA) I_{IL} (mA)			20 -0.4
I_{0a} - I_{0d}	Data inputs from Source "0"	I_{IH} (μA) I_{IL} (mA)			20 -0.4
I_{1a} - I_{1d}	Data inputs from Source "1"	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q_a - Q_d	Register outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "399" is a high speed Quad 2-Port Register. It selects four bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is loaded into the 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP).

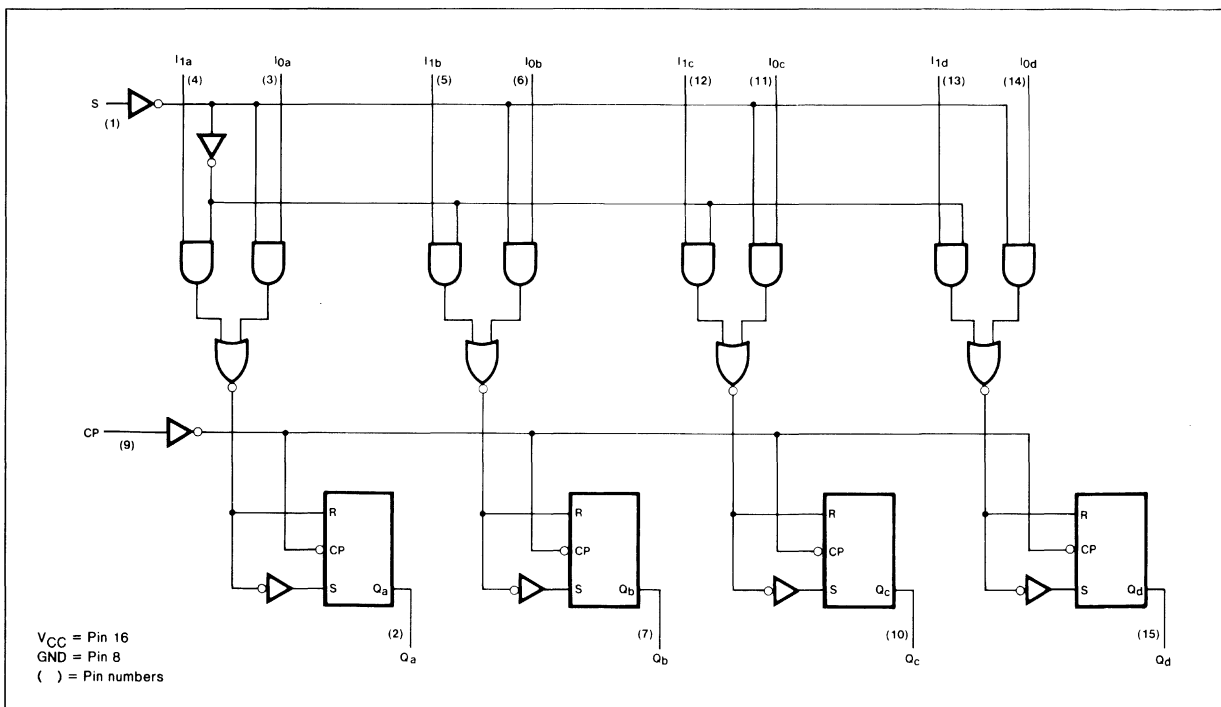
The operation of the device is fully synchronous. The Data inputs (I_0 & I_1) and the Select input (S) must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	CP	S	I_0	I_1	Q_n
Load Source "0"	↑	l	l	X	L
	↑	l	h	X	H
Load Source "1"	↑	h	X	l	L
	↑	h	X	h	H

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I _{CC} Supply current	V _{CC} = Max						13	mA

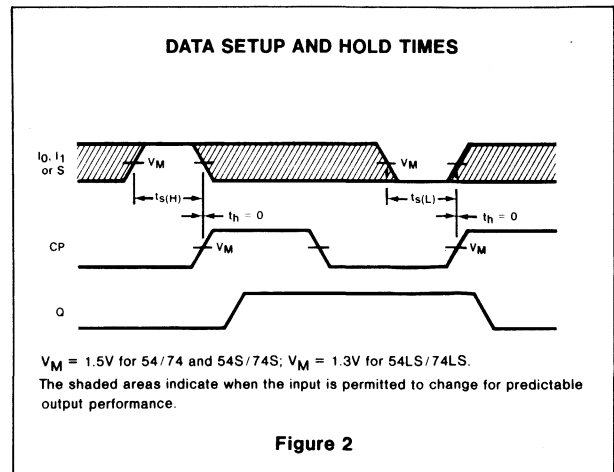
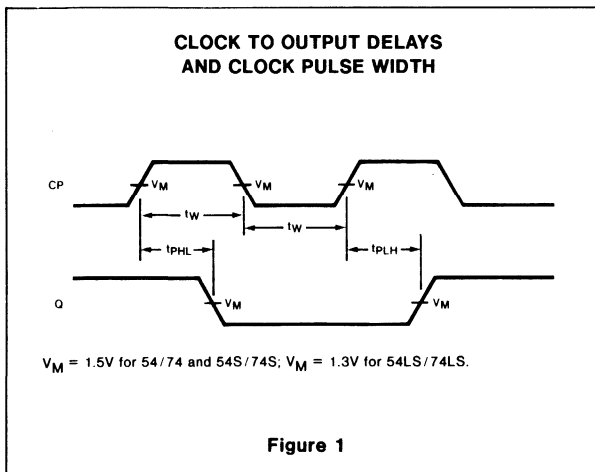
AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Clock to output	Figure 1						27 32	ns ns

AC SETUP REQUIREMENTS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t _w Clock pulse width	Figure 1					20		ns
t _s Setup time Data to Clock	Figure 2					20		ns
t _h Hold time Data to Clock	Figure 2					0		ns
t _s Setup time Select to Clock	Figure 2					25		ns
t _h Hold time Select to Clock	Figure 2					0		ns

AC WAVEFORMS



NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

54/74145
54LS/74LS145 (Preliminary data)

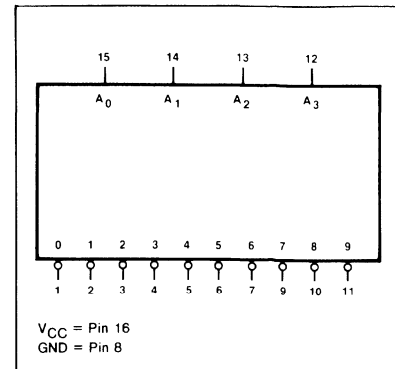
DESCRIPTION

The "445" is a TTL MSI array. It features standard TTL inputs and high voltage, high current (80mA) outputs. The "445" minimum output breakdown is 7 volts.

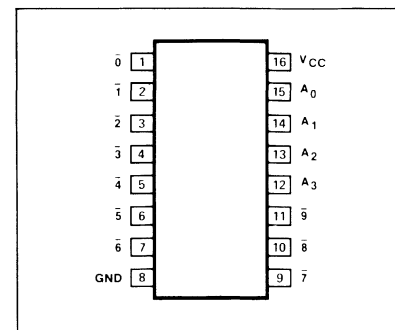
FEATURES

- 80mA output drive capability
- 7V output breakdown voltage
- See "45" for 30V output voltage
- See "42" for standard TTL outputs

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS445N	
Ceramic DIP	N74LS445F	S54LS445F
Flatpak		S54LS445W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION	54/74	54S/74S	54LS/74LS
A ₀ -A ₃	Address inputs I _{IH} (μA) I _{IL} (mA)			20 -0.4
0-9	Active LOW outputs I _{OH} (μA) I _{OL} (mA)			+250 12/80(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OL} Output LOW voltage	V _{CC} = Min I _{OL} = 12mA						0.4	V
							0.5(c)	V
							1.7(c)	V
I _{OH} Output HIGH current	V _{CC} = Min, V _{OUT} = 7V						250	μA
I _{CC} Supply current	V _{CC} = Max						13	mA
							13	mA

NOTES

- The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.
- This parameter for Commercial range only.

FUNCTIONAL DESCRIPTION

The "445" is a 1-of-10 decoder with open collector outputs. This decoder accepts BCD inputs on the A₀ to A₃ address lines and generates ten mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A₃ used as an active LOW enable.

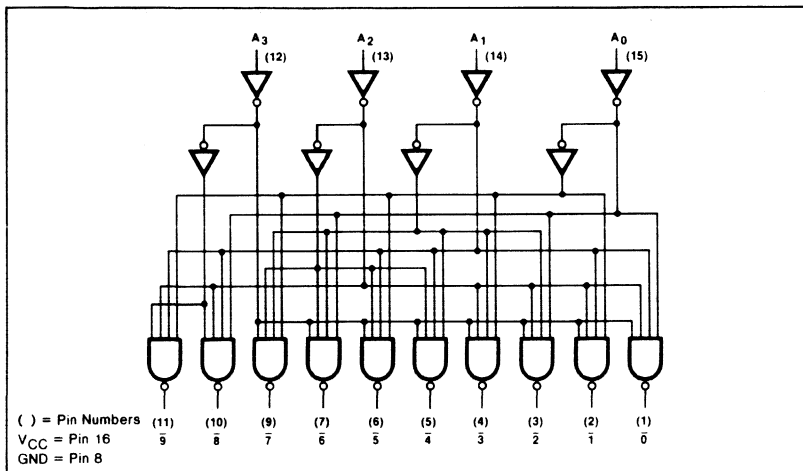
The "445" features an output breakdown voltage of 7V. This device is ideal as a lamp or solenoid driver.

TRUTH TABLE

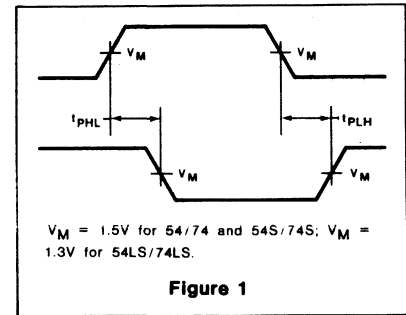
A ₃	A ₂	A ₁	A ₀	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

LOGIC DIAGRAM



AC WAVEFORM



AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 45pF R _L = 667Ω						
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation delay						50	ns
t _{PHL}	Address to output						50	ns

54LS/74LS490

DESCRIPTION

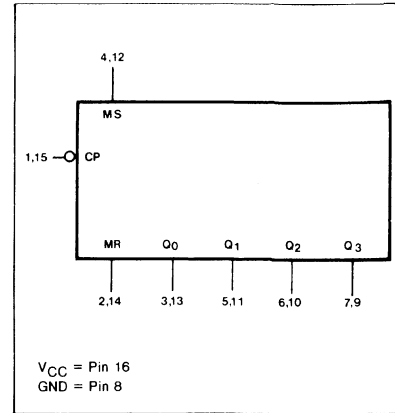
The "490" is a Dual BCD Decade Ripple Counter. Each decade counter is triggered by the HIGH-to-LOW transition of the clock inputs. The counter outputs are used as decoded inputs or clock inputs for succeeding stages.

Each decade counter has a Master Set (set-to-nine) input and a Master Reset (clear) input. These inputs are asynchronous and override the clock operation. The Master Set overrides the Master Reset if both are HIGH simultaneously.

FEATURES

- Two BCD decade counters
- Asynchronous Master Set (set-to-9)
- Asynchronous Master Reset (clear)

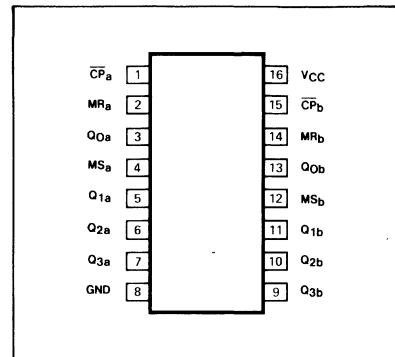
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS490N	
Ceramic DIP	N74LS490F	S54LS490F
Flatpak		S54LS490W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
\overline{CP}	Clock (active LOW going edge) inputs to each decade counter	I_{IH} (μA) I_{IL} (mA)			100 -1.6
MR	Master Reset (clear) inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
MS	Master Set (set to 9) inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
Q_0 - Q_3	Counter outputs	I_{OH} (μA) I_{OL} (mA)			-400 4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$						26	mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

FUNCTIONAL DESCRIPTION

The "490" is a Dual BCD Decade Ripple Counter with separate Clock, Master Set, and Master Reset inputs to each counter. The operation of each half of the "490" is the same as the "90" used in the BCD decade mode.

The counters are triggered by the HIGH-to-LOW transition of the Clock (\overline{CP}) inputs. No external connections are required to get the full BCD (8421) decade counting scheme from the counters. The counter outputs are internally connected as clocks or decoded inputs to succeeding stages. The outputs are designed to drive the internal gates plus the rated fan-out of the device. Since this is a ripple type counter, the outputs do not change synchronously and should not be used for high speed address decoding.

The Master Set (MS) and Master Reset (MR) are asynchronous active HIGH inputs. The HIGH MR input overrides the clock and clears the associated 4-bits of the counter. The HIGH MS input overrides the clock and MR inputs and sets the associated 4-bits to nine (HLLH).

MODE SELECTION—TRUTH TABLE FOR 1/2 THE "490"

RESET/SET INPUTS		OUTPUTS			
MR	MS	Q ₀	Q ₁	Q ₂	Q ₃
H	X	L	L	L	L
X	H	H	L	L	H
L	L	Count			

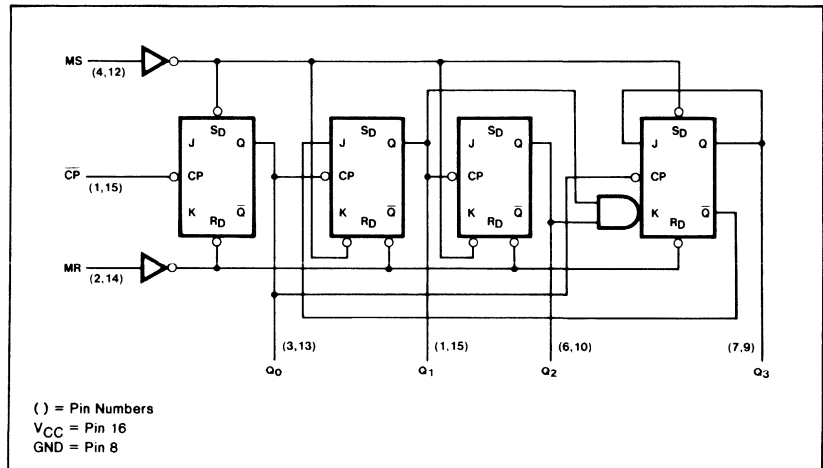
H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE—FOR 1/2 THE "490"

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
Output Q₀ connected to input \overline{CP}_1 .

LOGIC DIAGRAM



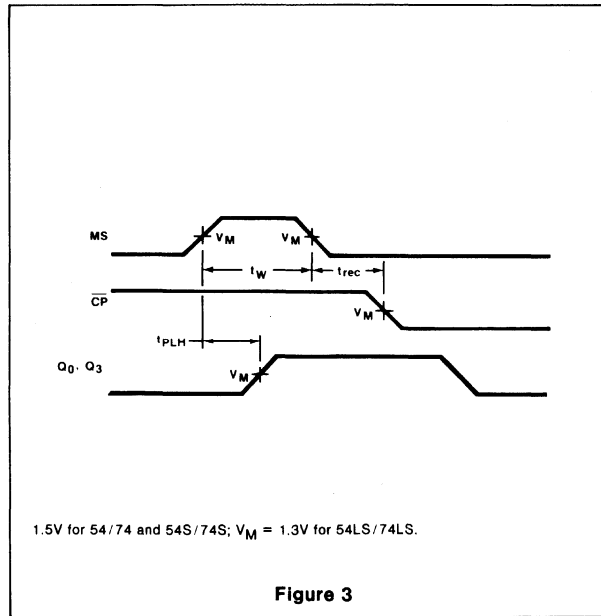
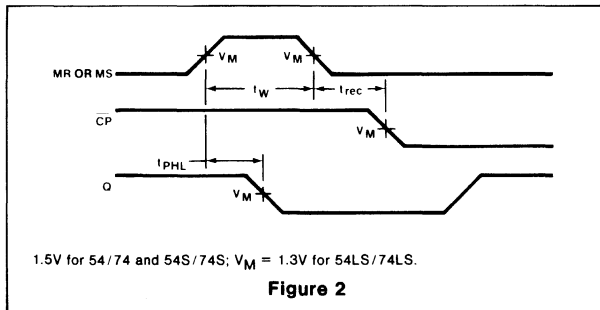
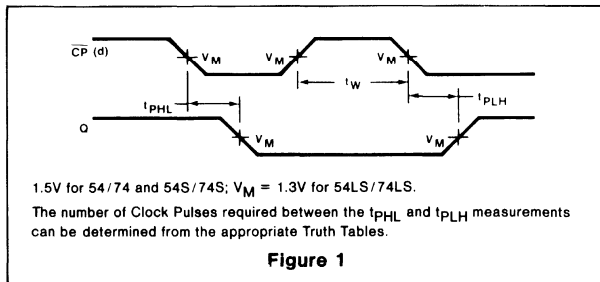
AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		C _L = 15pF R _L = 2kΩ						
		Min	Max	Min	Max	Min	Max	
f _{MAX}	\overline{CP} input count frequency					35		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Q ₀						20 20	ns ns
t _{PLH} t _{PHL}	Propagation delay \overline{CP} to Q ₁ or Q ₃						39 39	ns ns
t _{PLH} t _{PHL}	Propagation delay CP to Q ₂						54 54	ns ns
t _{PHL}	Propagation delay MR to Q						39	ns
t _{PLH} t _{PHL}	Propagation delay MS to Q						35 35	ns ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W $\overline{\text{CP}}$ pulse width	Figure 1					15		ns
t_W MR pulse width	Figure 2					35		ns
t_W MS pulse width	Figures 2 & 3					35		ns
t_{rec} Recovery time MR to $\overline{\text{CP}}$	Figure 2					20		ns
t_{rec} Recovery time MS to $\overline{\text{CP}}$	Figures 2 & 3					20		ns

AC WAVEFORMS



54LS/74LS568 (Preliminary data)

DESCRIPTION

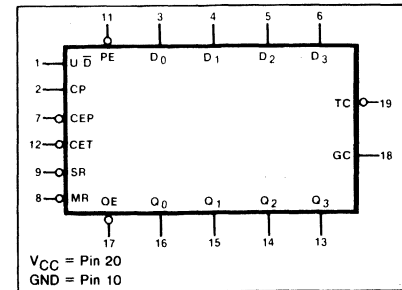
The "568" is a synchronous 4-stage BCD decade (8, 4, 2, 1) UP/DOWN counter featuring preset capability for programmable operation, carry look ahead for easy cascading and U/D input to control the direction of counting. All state changes while counting or loading are initiated by the LOW-to-HIGH transition of the clock.

3-State drivers are provided on the counter outputs for direct interface to bus organized systems. In addition to the Synchronous Reset an asynchronous Master Reset has been provided which overrides all other inputs to set all stages LOW.

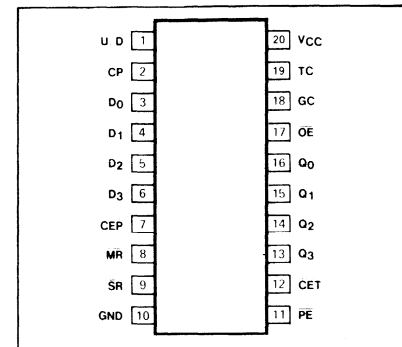
FEATURES

- Synchronous counting and loading
- UP/DOWN counting
- BCD Decade counter
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous master reset
- 3-State counter outputs
- Gated carry output

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 8 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS568N	
Ceramic DIP	N74LS568F	S54LS568F
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{PE}	Parallel Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{CEP}	Count Enable Parallel (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{CET}	Count Enable Trickle (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
U/D	UP/DOWN Control input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
D ₀ -D ₃	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{MR}	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{SR}	Synchronous Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{OE}	Output Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
Q ₀ -Q ₃	3-State counter outputs	I _{OH} (mA) I _{OL} (mA)			-1/-2.6(a) 12/24(a)
\overline{TC}	Terminal Count (active LOW) output	I _{OH} (μA) I _{OL} (mA)			-400 4/8(a)
GC	Gated Clock, Terminal Count output	I _{OH} (μA) I _{OL} (mA)			-400 4/8(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "568" is a synchronous presettable BCD decade UP/DOWN counter featuring an internal carry look-ahead for applications in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The Synchronous Reset (\overline{SR}), when LOW one set-up time before the LOW-to-HIGH transition of the clock, overrides the \overline{CEP} , \overline{CET} and \overline{PE} inputs, and causes the flip-flops to go LOW coincident with the positive clock transition.

The Master Reset (\overline{MR}) is an asynchronous overriding clear function which forces all stages to a LOW state while the \overline{MR} input is LOW without regard to the clock.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs ($\overline{CET} \bullet \overline{CEP}$) and a Terminal Count (\overline{TC}) output. Both count enable inputs must be LOW to count. The \overline{CET} input is fed forward to enable the \overline{TC} output. The \overline{TC} output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level \overline{TC} pulse is used to enable successive cascaded stages. See Figure A in "168" data sheet for the fast synchronous multistage counting connections.

The Gated Clock output (GC) is a Terminal Count output which provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW

time of the clock pulse when \overline{TC} is LOW. The GC output can be used as a clock input for the next stage in a simple ripple expansion scheme.

The direction of counting is controlled by the UP/DOWN (U/\overline{D}) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The active LOW Output Enable (\overline{OE}) input controls the 3-state buffer outputs independent of the counter operation. When \overline{OE} is LOW, the count appears at the buffer outputs. When \overline{OE} is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

COUNTER OPERATING MODES	INPUTS								COUNTER STATES			
	MR	CP	SR	U/ \overline{D}	PE	CEP	CET	D_n	Q ₀	Q ₁	Q ₂	Q ₃
Asynchronous Reset	L	X	X	X	X	X	X	X	L	L	L	L
Synchronous Reset	H	†	l	X	X	L	L	X	L	L	L	L
Parallel load	H	†	h	X	l	X	X	l	L	L	L	L
	H	†	h	X	l	X	X	h	H	H	H	H
Count up	H	†	h	h	h	l	l	X	count up			
Count down	H	†	h	l	h	l	l	X	count down			
Hold (do nothing)	H	†	h	X	h	h	X	X	no change			
	H	†	h	X	h	X	h	X	no change			

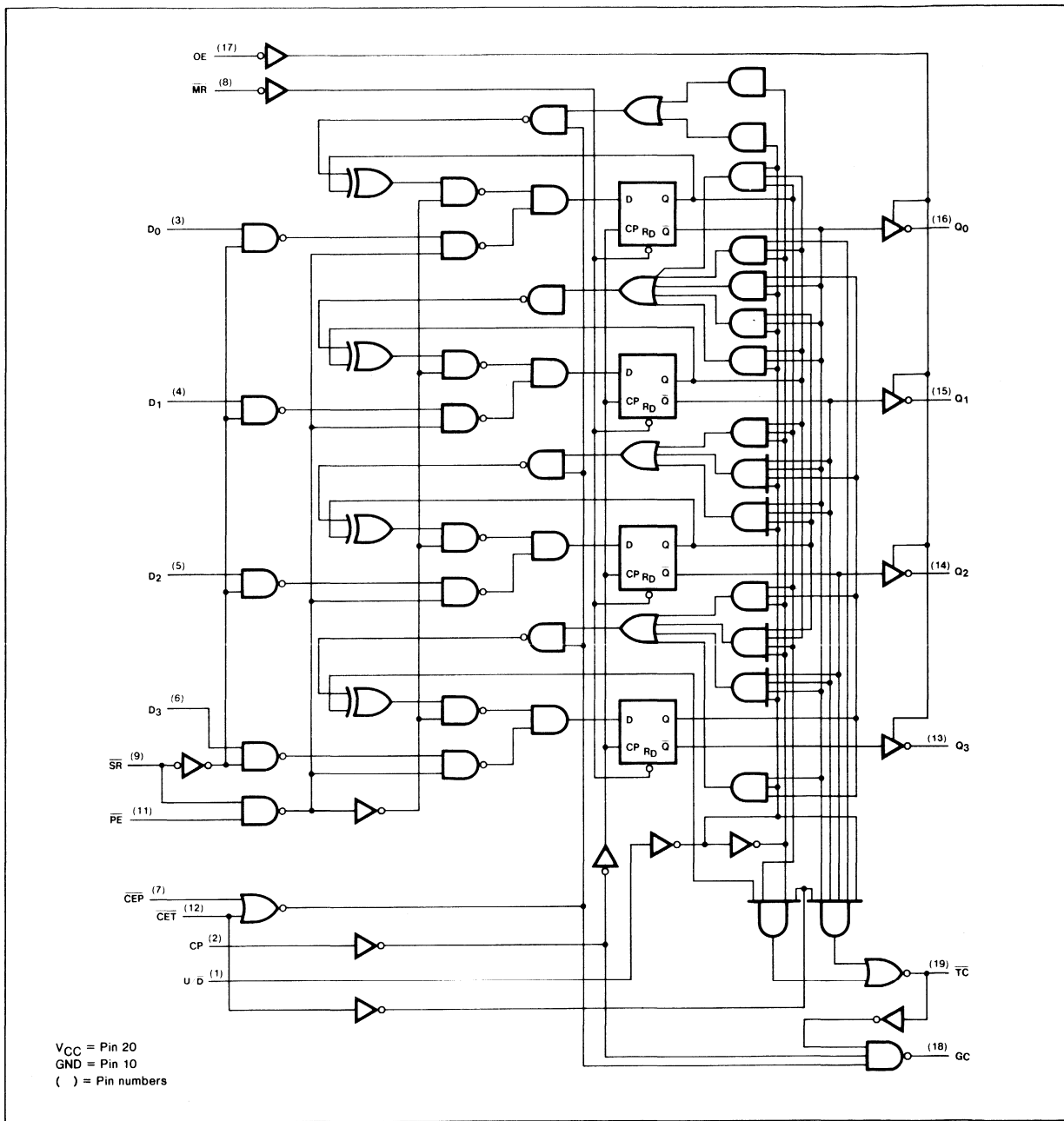
3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	\overline{OE}	Q _n - Counter	Q ₀ , Q ₁ , Q ₂ , Q ₃
Read counter	L	L	L
	L	H	H
Disable outputs	H	L	(Z)
	H	H	(Z)

TERMINAL COUNT TRUTH TABLE

INPUTS				COUNTER STATES				OUTPUTS	
CP	U/ \overline{D}	\overline{CEP}	\overline{CET}	Q ₀	Q ₁	Q ₂	Q ₃	\overline{TC}	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	X	X	H	L	H
L	H	L	L	H	X	X	H	L	L
X	H	H	L	H	X	X	H	L	H
X	H	X	H	H	X	X	H	H	H

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
(Z) = High impedance "off" state
† = LOW-to-HIGH clock transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = Min I _{OH} = See Fan Out Table					2.4		V
V _{OL} Output LOW voltage Q ₀ , Q ₁ , Q ₂ , Q ₃	V _{CC} = Min I _{OL} = 12mA						0.4	V
							0.5 (c)	V
V _{OL} Output LOW voltage \overline{TC} and GC	V _{CC} = Min I _{OL} = 4mA						0.4	V
							0.5 (c)	V
I _{OS} Output short circuit current	V _{CC} = Max Q ₀ , Q ₁ , Q ₂ , Q ₃ \overline{TC} and GC					-30	-100	mA
						-15	-100	mA
I _{CC} Supply current	V _{CC} = Max, V _{OE} = 4.5 V						43	mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						C _L = 45pF R _L = 667Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1					25		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Figure 1					20 23		ns ns
t _{PLH} Propagation delay t _{PHL} Clock to \overline{TC}	Figure 2					35 35		ns ns
t _{PLH} Propagation delay t _{PHL} \overline{CET} to \overline{TC}	Figure 3					14 14		ns ns
t _{PLH} Propagation delay t _{PHL} U/ \overline{D} control to \overline{TC}	Figure 4					25 29		ns ns
t _{PLH} Propagation delay t _{PHL} Clock to GC	Figure 2					20 20		ns ns
t _{PHL} Propagation delay \overline{MR} to output	Figure 5					35		ns
t _{PZH} Output enable to HIGH level	Figure 6							ns
t _{PZL} Output enable to LOW level	Figure 7							ns
t _{PHZ} Output disable from HIGH level	Figure 6							ns
	Figure 6, C _L = 5pF(d)							ns
t _{PLZ} Output disable from LOW level	Figure 7							ns
	Figure 7, C _L = 5pF(d)							ns

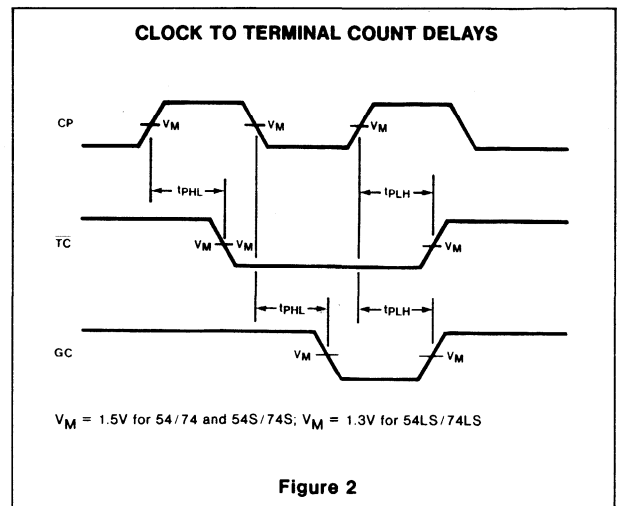
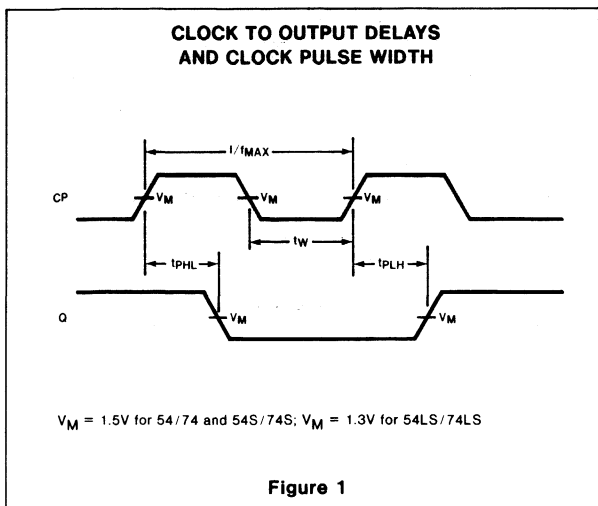
NOTES

- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. This parameter for Commercial Range only.
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

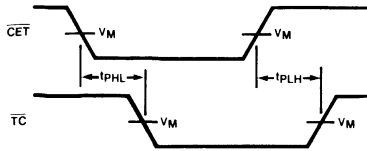
PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_w Clock pulse width	Figure 1					20		ns
t_s Set-up time data to clock	Figure 8					20		ns
t_h Hold time data to clock	Figure 8					0		ns
t_s Set-up time \overline{PE} to clock	Figure 8					25		ns
t_h Hold time \overline{PE} to clock	Figure 8					0		ns
t_s Set-up time \overline{CEP} & \overline{CET} to clock	Figure 9					20		ns
t_h Hold time \overline{CEP} & \overline{CET} to clock	Figure 9					0		ns
t_s Set-up time U/\overline{D} to clock	Figure 10					30		ns
t_h Hold time U/\overline{D} to clock	Figure 10					0		ns
t_s Set-up time \overline{SR} to clock	Figure 11					30		ns
t_h Hold time \overline{SR} to clock	Figure 11					0		ns
t_{rec} Recovery time \overline{MR} to clock	Figure 5					20		ns

AC WAVEFORMS



AC WAVEFORMS (cont'd)

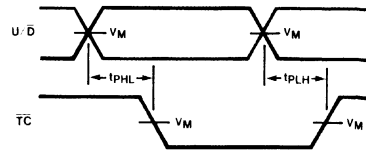
PROPAGATION DELAYS \overline{CET} INPUT TO TERMINAL COUNT OUTPUT



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

Figure 3

PROPAGATION DELAYS $\overline{U/D}$ CONTROL TO TERMINAL COUNT OUTPUT



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

Figure 4

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

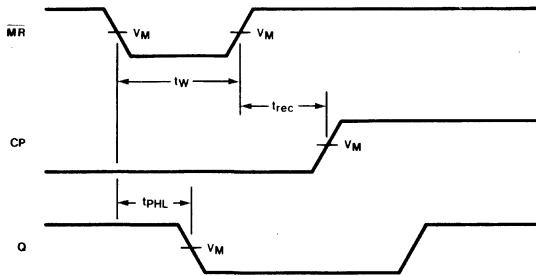
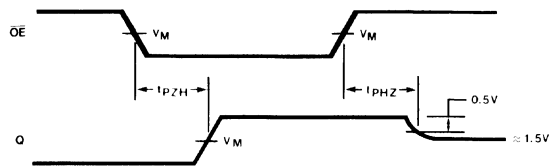


Figure 5

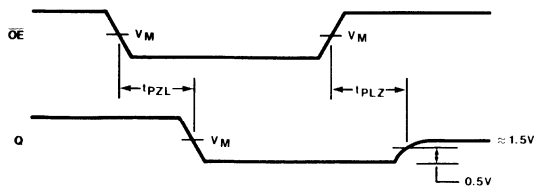
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

Figure 6

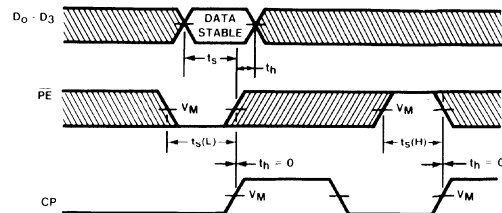
3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

Figure 7

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES

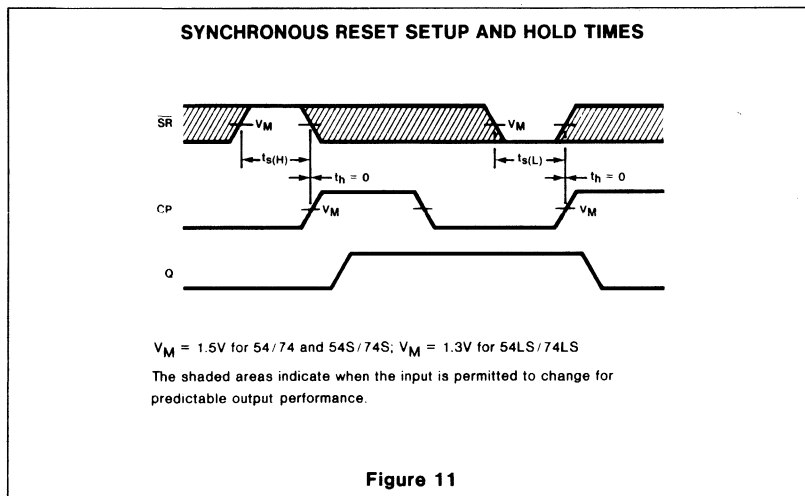
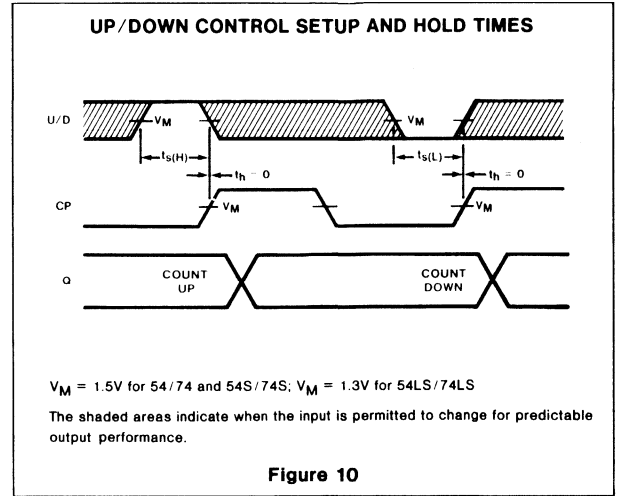
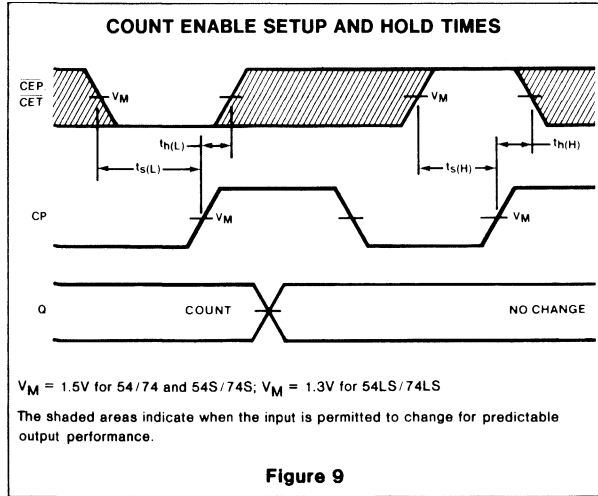


$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 8

AC WAVEFORMS (cont'd)



54LS/74LS569 (Preliminary data)

DESCRIPTION

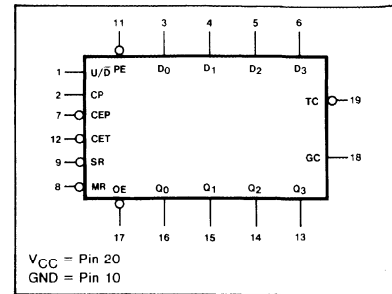
The "569" is a synchronous 4-stage Modulo 16 binary UP/DOWN counter featuring preset capability for programmable operation, carry look ahead for easy cascading and U/D input to control the direction of counting. All state changes while counting or loading, are initiated by the LOW-to-HIGH transition of the clock.

3-State drivers are provided on the counter outputs for direct interface to bus organized systems. In addition to the Synchronous Reset an asynchronous Master Reset has been provided which overrides all other inputs setting all stages LOW.

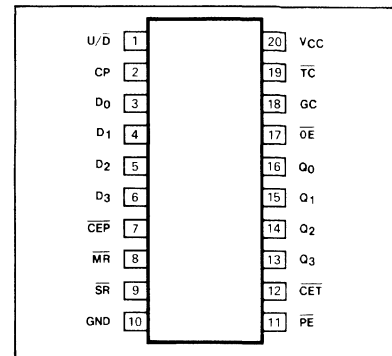
FEATURES

- Synchronous counting and loading
- UP/DOWN counting
- Modulo 16 Binary Counter
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous Master Reset
- 3-State counter outputs
- Gated carry output

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N74LS569N	
Ceramic DIP	N74LS569F	S54LS569F
Flatpak		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{PE}	Parallel Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{CEP}	Count Enable Parallel (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{CET}	Count Enable Trickle (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
U/ \overline{D}	UP/DOWN Control input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
D ₀ -D ₃	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{MR}	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{SR}	Synchronous Reset (active LOW)	I _{IH} (μA) I _{IL} (mA)			20 -0.4
\overline{OE}	Output Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)			20 -0.4
Q ₀ -Q ₃	3-State counter outputs	I _{OH} (mA) I _{OL} (mA)			-1 / -2.6 (a) 12/24 (a)
\overline{TC}	Terminal Count (active LOW) output	I _{OH} (μA) I _{OL} (mA)			-400 4/8 (a)
GC	Gated Clock, terminal count output	I _{OH} (μA) I _{OL} (mA)			-400 4/8 (a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "569" is a synchronous presettable Modulo 16 binary UP/DOWN counter featuring an internal carry look-ahead for applications in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (PE) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The Synchronous Reset (SR), when LOW one setup time before the LOW-to-HIGH transition of the clock, overrides the CEP, CET, and PE inputs, and causes the flip-flops to go LOW coincident with the positive clock transition.

The Master Reset (MR) is an asynchronous overriding clear function which forces all stages to a LOW state while the MR input is LOW without regard to the clock.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs (CET • CEP) and a Terminal Count (TC) output. Both count enable inputs must be LOW to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q₀ output. This LOW level TC pulse is used to enable successive cascaded stages. See Figure A in "169" data sheet for the fast synchronous multistage counting connections.

The Gated Clock output (GC) is a Terminal Count output which provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse when TC is LOW. The GC output can be used as a clock input for the next stage in a simple ripple expansion scheme.

The direction of counting is controlled by the UP/DOWN (U/D) input; a HIGH will cause

MODE SELECT—FUNCTION TABLE

COUNTER OPERATING MODES	INPUTS								COUNTER STATES			
	MR	CP	SR	U/D	PE	CEP	CET	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Asynchronous Reset	L	X	X	X	X	X	X	X	L	L	L	L
Synchronous Reset	H	↑	↓	X	X	L	L	X	L	L	L	L
Parallel load	H	↑	h	X	↓	X	X	↓	L	L	L	L
	H	↑	h	X	↓	X	X	h	H	H	H	H
Count up	H	↑	h	h	h	↓	↓	X	count up			
Count down	H	↑	h	↓	h	↓	↓	X	count down			
Hold (do nothing)	H	↑	h	X	h	h	X	X	no change			
	H	↑	h	X	h	X	h	X	no change			

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	OE	Q _n - Counter	Q ₀ , Q ₁ , Q ₂ , Q ₃
Read counter	L	L	L
	L	H	H
Disable outputs	H	L	(Z)
	H	H	(Z)

TERMINAL COUNT TRUTH TABLE

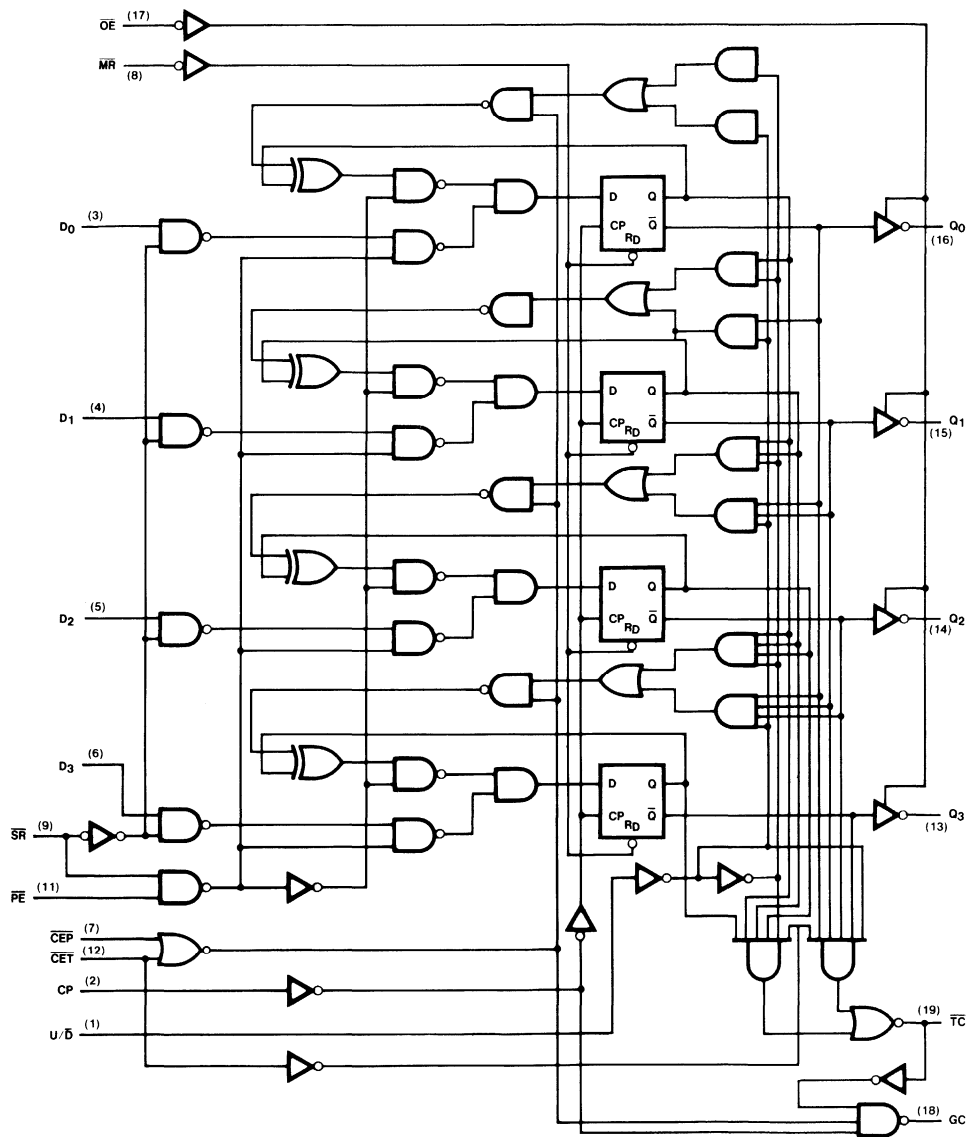
INPUTS				COUNTER STATES				OUTPUTS	
CP	U/D	CEP	CET	Q ₀	Q ₁	Q ₂	Q ₃	TC	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	L	H
H	H	L	L	H	H	H	H	L	H
L	H	L	L	H	H	H	H	L	L
X	H	H	L	H	H	H	H	L	H
X	H	X	H	H	H	H	H	H	H

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care
 (Z) = High impedance "off" state
 ↑ = LOW-to-HIGH clock transition

the count to increase, a LOW will cause the count to decrease.

The active LOW Output Enable (OE) input controls the 3-state buffer outputs independent of the counter operation. When OE is LOW, the count appears at the buffer outputs. When OE is HIGH, the outputs are in the high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM



V_{CC} = Pin 20
 GND = Pin 10
 () = Pin number

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = Min. I _{OH} = See Fan Out Table					2.4		V
V _{OL} Output LOW voltage Q ₀ , Q ₁ , Q ₂ , Q ₃	V _{CC} = Min. I _{OL} = 12mA						0.4	V
							0.5(c)	V
V _{OL} Output LOW voltage \overline{TC} and GC	V _{CC} = Min. I _{OL} = 4mA						0.4	V
							0.5(c)	V
I _{OS} Output short circuit current	V _{CC} = Max Q ₀ , Q ₁ , Q ₂ , Q ₃ \overline{TC} and GC					-30	-100	mA
						-15	-100	mA
I _{CC} Supply current	V _{CC} = Max, V _{OE} = 4.5V						43	mA

AC CHARACTERISTICS: T_A=25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						C _L = 45pF R _L = 667Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Figure 1					25		MHz
t _{PLH} Propagation delay	Figure 1						20	ns
t _{PHL} Clock to output							23	ns
t _{PLH} Propagation delay	Figure 2						35	ns
t _{PHL} Clock to \overline{TC}							35	ns
t _{PLH} Propagation delay	Figure 3						14	ns
t _{PHL} CET to TC							14	ns
t _{PLH} Propagation delay	Figure 4						25	ns
t _{PHL} U/ \overline{D} control to \overline{TC}							29	ns
t _{PLH} Propagation delay	Figure 2						20	ns
t _{PHL} Clock to GC							20	ns
t _{PHL} Propagation delay \overline{MR} to output	Figure 5						35	ns
t _{pZH} Output enable to HIGH level	Figure 6							ns
t _{pZL} Output enable to LOW level	Figure 7							ns
t _{PHZ} Output disable from HIGH level	Figure 6							ns
	Figure 6, C _L = 5pF (d)							ns
t _{PLZ} Output disable from LOW level	Figure 7							ns
	Figure 7, C _L = 5pF (d)							ns

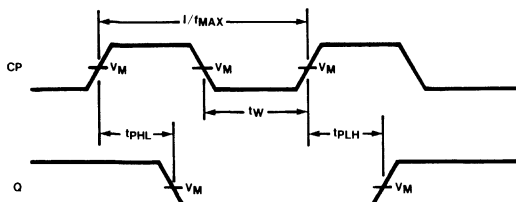
NOTES

- b. For family dc characteristics see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specification.
- c. This parameter for Commercial Range only.
- d. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W Clock pulse width	Figure 1					20		ns
t_S Setup time data to clock	Figure 8					20		ns
t_H Hold time data to clock	Figure 8					0		ns
t_S Setup time \overline{PE} to clock	Figure 8					25		ns
t_H Hold time \overline{PE} to clock	Figure 8					0		ns
t_S Setup time \overline{CEP} & \overline{CET} to clock	Figure 9					20		ns
t_H Hold time \overline{CEP} & \overline{CET} to clock	Figure 9					0		ns
t_S Setup time U/\overline{D} to clock	Figure 10					30		ns
t_H Hold time U/\overline{D} to clock	Figure 10					0		ns
t_S Setup time \overline{SR} to clock	Figure 11					30		ns
t_H Hold time \overline{SR} to clock	Figure 11					0		ns
t_{rec} Recovery time \overline{MR} to clock	Figure 5					20		ns

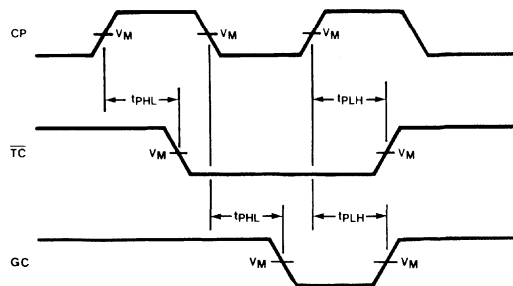
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

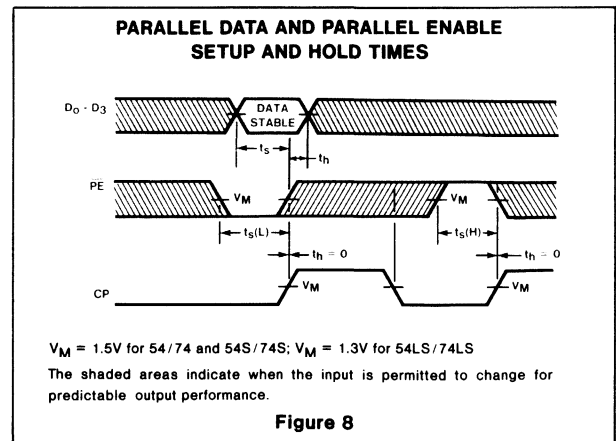
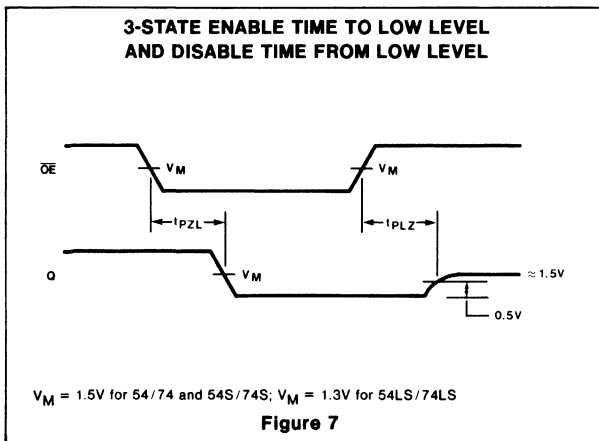
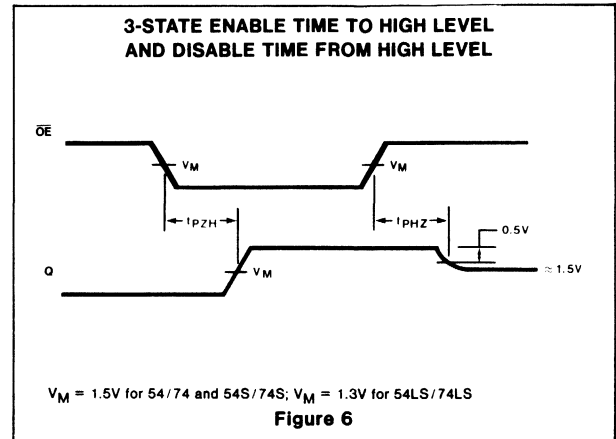
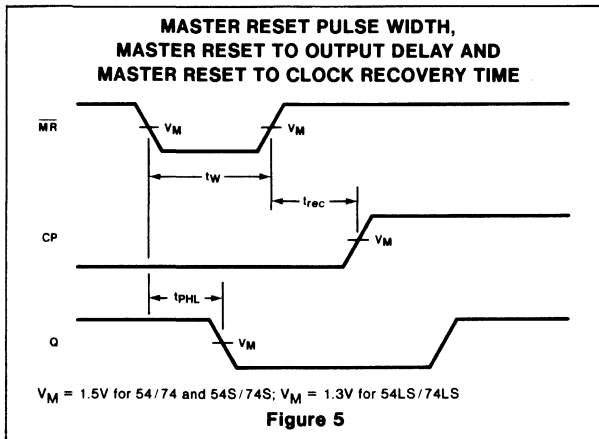
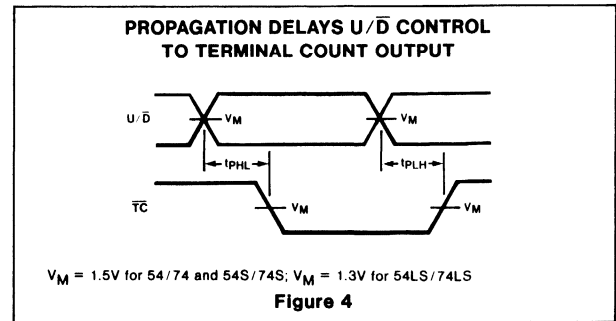
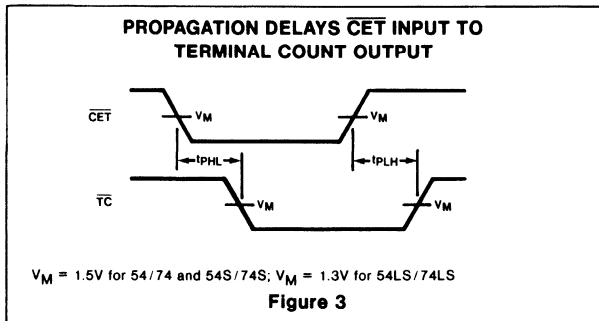
Figure 1

CLOCK TO TERMINAL COUNT DELAYS

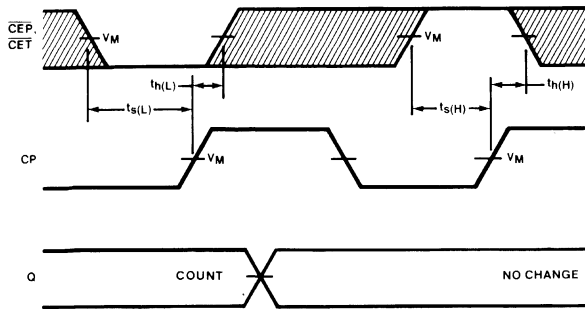


$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

Figure 2



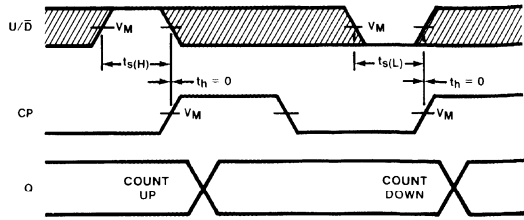
COUNT ENABLE SETUP AND HOLD TIMES



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS
 The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 9

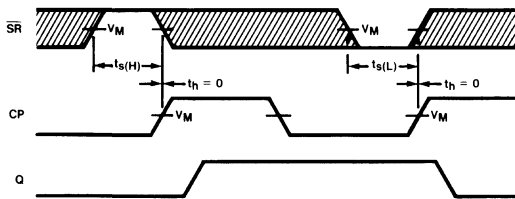
UP/DOWN CONTROL SETUP AND HOLD TIMES



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS
 The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 10

SYNCHRONOUS RESET SETUP AND HOLD TIMES



$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS
 The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 11

54LS/74LS670

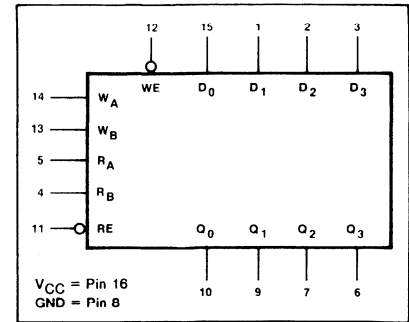
DESCRIPTION

The "670" is a 4-by-4 Register File with 3-State outputs organized as 4-words of 4-bits. Simultaneous read and write operation is allowed by separate read and write inputs, both address and enable. An almost unlimited number of devices can be stacked to increase the word capacity by tying the 3-state outputs together. Any number of these devices can be operated in parallel to generate an n-bit word.

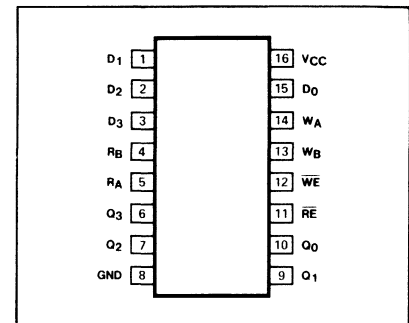
FEATURES

- Simultaneous and independent Read and Write operations
- Expandable to almost any word size and bit length
- 3-State outputs
- See "170" for open collector version

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS670N	
Ceramic DIP	N74LS670F	S54LS670F
Flatpak		S54LS670W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
D ₀ -D ₃	Data inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
W _A , W _B	Write address inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{WE}	Write Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			40 -0.8
R _A , R _B	Read address inputs	I_{IH} (μA) I_{IL} (mA)			20 -0.4
\overline{RE}	Read Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)			40 -0.8
Q ₀ -Q ₃	Outputs	I_{OH} (mA) I_{OL} (mA)			-1 / -2.6 ^(a) 4/8 ^(a)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(d)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = Min	$I_{OH} = -1.0mA$				2.4		V
		$I_{OH} = -2.6mA$				2.4 ^(e)		V
I _{CC} Supply current	V _{CC} = Max					50		mA

NOTES

- a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively. e. This parameter for Commercial range only.
- d. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

FUNCTIONAL DESCRIPTION

The "670" is a 16-bit 3-State Register File organized as 4-words of 4-bits each. Separate read and write address and enable inputs are available permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write Address inputs (W_A & W_B) determine the location of the stored word. When the Write Enable (\overline{WE}) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the \overline{WE} is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs. Data and Write Address inputs are inhibited when \overline{WE} is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A & R_B). The addressed word appears at the four outputs when the Read Enable (\overline{RE}) is LOW. Data outputs are in the high impedance "off" state when the Read Enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-state outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull up resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES ^(b)
	\overline{WE}	D_n	
Write Data	L L	L H	L H
Data Latched	H	X	no change

NOTE
b. The Write Address (W_A & W_B) to the "internal latches" must be stable while \overline{WE} is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS Q_n
	\overline{RE}	INTERNAL LATCHES ^(c)	
Read	L L	L H	L H
Disabled	H	X	(Z)

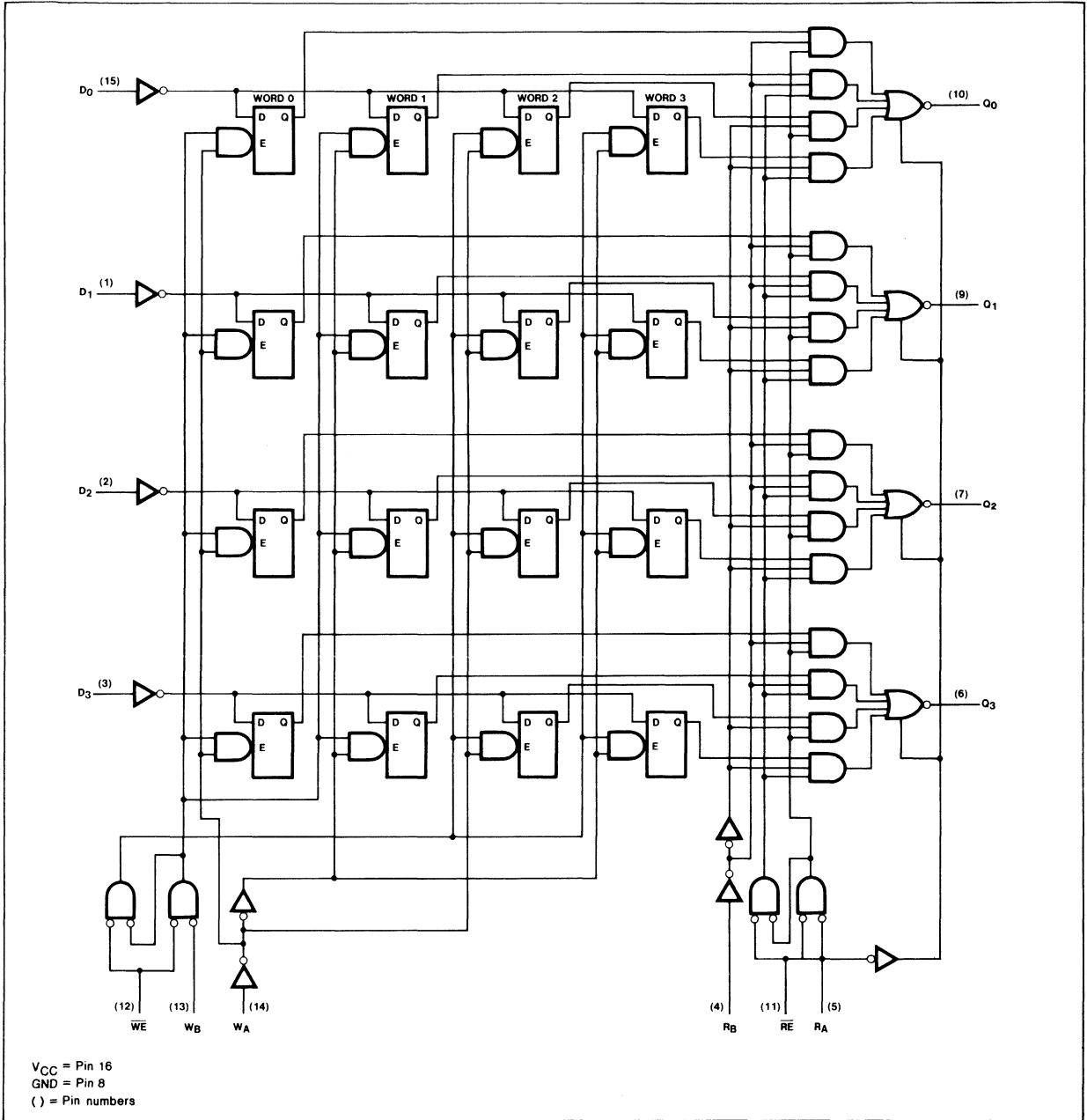
NOTE
c. The Read Address (R_A & R_B) changes to select the "internal latches" are not constrained by \overline{WE} or \overline{RE} operation.

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" state

AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
						$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Read Address to output						40 45	ns ns
t_{PLH} t_{PHL}	Propagation delay Write Enable to output						45 50	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output						45 40	ns ns
t_{PZH}	Read enable time to HIGH level						35	ns
t_{PZL}	Read enable time to LOW level						40	ns
t_{PHZ}	Disable time from HIGH level						50	ns
t_{PLZ}	Disable time from LOW level						35	ns

LOGIC DIAGRAM

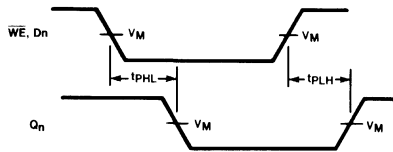


AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	
t_W	Write Enable pulse width					25		ns
t_s	Setup time Data to positive going WE					10		ns
t_h	Hold time Data to positive going WE					15		ns
t_s	Setup time Read Address to negative going WE					15		ns
t_h	Hold time Read Address to positive going WE					5.0		ns

AC WAVEFORMS

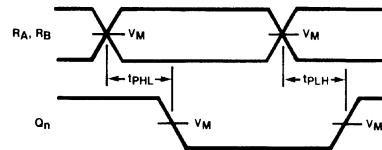
PROPAGATION DELAY, WRITE ENABLE AND DATA TO OUTPUTS



$V_M = 1.5\text{V}$ for 54/74 and 54S/74S; $V_M = 1.3\text{V}$ for 54LS/74LS

Figure 1

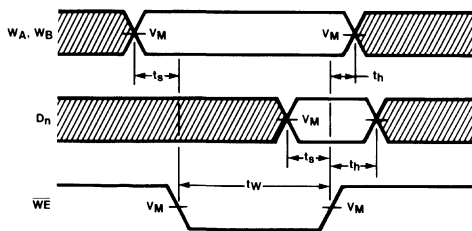
PROPAGATION DELAY READ ADDRESS TO OUTPUTS



$V_M = 1.5\text{V}$ for 54/74 and 54S/74S; $V_M = 1.3\text{V}$ for 54LS/74LS

Figure 2

SETUP AND HOLD TIMES WRITE ADDRESS AND DATA TO WRITE ENABLE

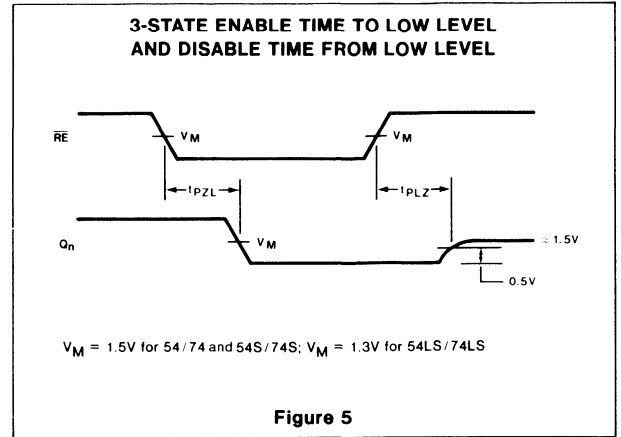
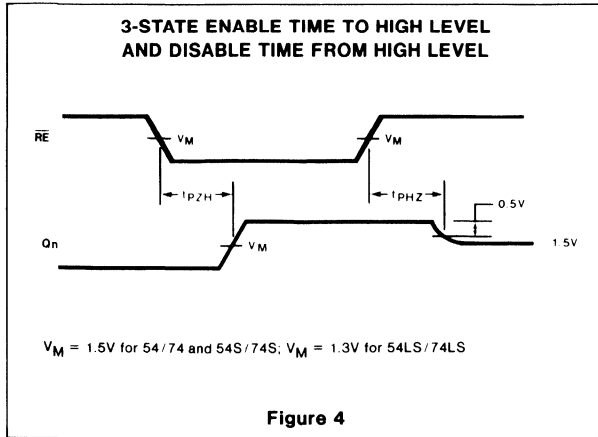


$V_M = 1.5\text{V}$ for 54/74 and 54S/74S; $V_M = 1.3\text{V}$ for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3

AC WAVEFORMS (Cont'd)



SECTION 4

AC Waveforms and Conditions

AC TEST CIRCUITS AND WAVEFORMS

This section contains the parameter measurement information necessary to perform the ac/switching tests for the majority of the devices specified in this book. The individual data sheets specify the appropriate variables data applicable to the TTL devices; i.e. R_L and C_L .

The equivalent test circuits used to measure the ac performance of the devices contained in this book are shown in Figures 1 thru 6. The table below specifies the test circuits applicable to the various output configurations of each TTL family. The table also specifies the input pulse requirements necessary for performing the ac tests. The

specified Repetition Rate (Rep. Rate) and Pulse Width are for the general test case which are neither frequency nor duty cycle sensitive. For measuring specified values of f_{MAX} (frequency) or t_{PW} (pulse width) the minimum values specified in the data sheets should be used in place of the values shown in the table.

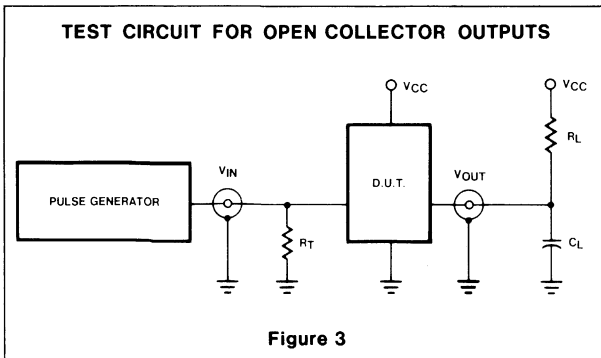
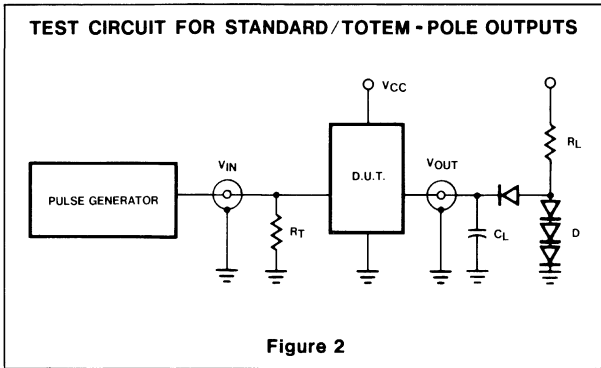
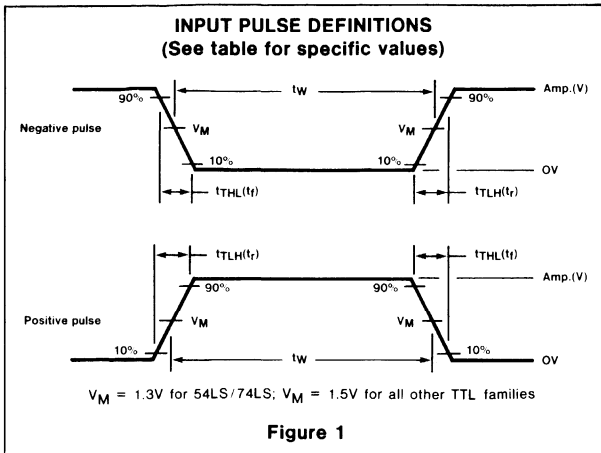
The measurement of ac parameters requires a number of setup and performance precautions to assure accurate, repeatable readings. The ac test fixture must conform to good high frequency design practice such as: pc boards with ground planes, short source and sense leads of equal length, no

switches between the sensing point and the device under test, and properly terminated pulse generator input lines. The power supply must be adequately decoupled with a good high frequency capacitor at the test head or socket. The ac load circuit must be connected as close to the device under test as possible. The probe used to make the output measurements should be a high impedance (10Megohm or FET) type, except for the 8200 series. As shown in Figure 5, the load circuit for the 8200 devices has been designed to accommodate a 5k Ω probe, or a high impedance probe with a 5k Ω terminating resistor.

TEST CIRCUITS AND INPUT PULSE REQUIREMENTS

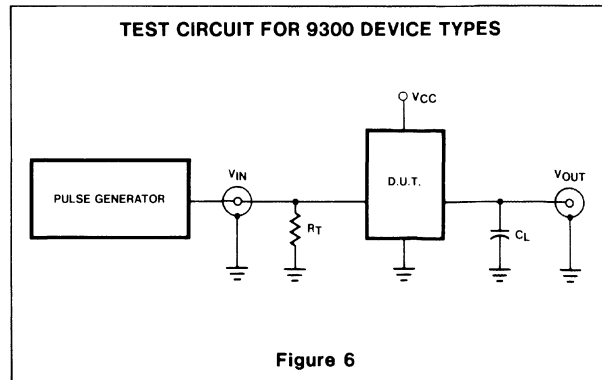
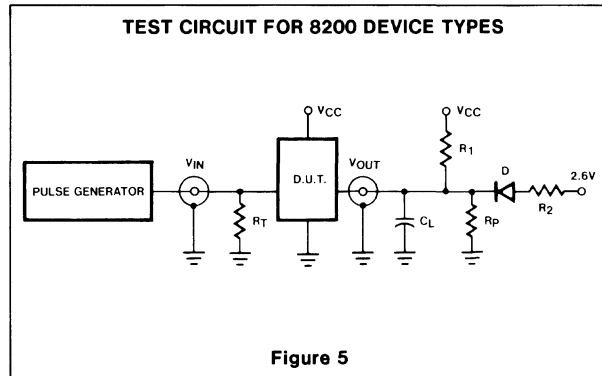
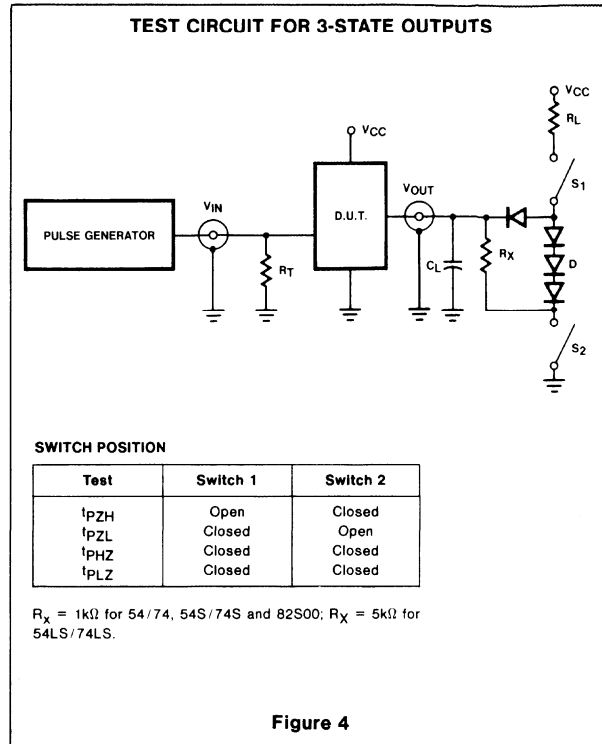
FAMILY (Output)	TEST CIRCUIT	INPUT PULSE REQUIREMENTS (See Figure 1)				
		Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74 (Standard) (O.C.) (3-State)	Figure 2	3.0V	1MHz	500ns	7ns	7ns
	Figure 3	3.0V	1MHz	500ns	7ns	7ns
	Figure 4	3.0V	1MHz	500ns	7ns	7ns
54H/ 74H (Standard) (O.C.)	Figure 2	3.0V	1MHz	500ns	7ns	7ns
	Figure 3	3.0V	1MHz	500ns	7ns	7ns
54S/ 74S (Standard) (O.C.) (3-State)	Figure 2	3.0V	1MHz	500ns	2.5ns	2.5ns
	Figure 3	3.0V	1MHz	500ns	2.5ns	2.5ns
	Figure 4	3.0V	1MHz	500ns	2.5ns	2.5ns
54LS/ 74LS (Standard) (O.C.) (3-State)	Figure 2	3.0V	1MHz	500ns	6ns	6ns
	Figure 3	3.0V	1MHz	500ns	6ns	6ns
	Figure 4	3.0V	1MHz	500ns	6ns	6ns
8200 (Standard) (O.C.)	Figure 5	2.6V	1MHz	500ns	5ns	5ns
	Figure 5	2.6V	1MHz	500ns	5ns	5ns
82S00 (Standard) (O.C.) (3-State)	Figure 2	3.0V	1MHz	500ns	2.5ns	2.5ns
	Figure 3	3.0V	1MHz	500ns	2.5ns	2.5ns
	Figure 4	3.0V	1MHz	500ns	2.5ns	2.5ns
9300 (Standard) (O.C.)	Figure 6	3.0V	1MHz	500ns	7ns	7ns
	Figure 3	3.0V	1MHz	500ns	7ns	7ns

O.C. = Open collector



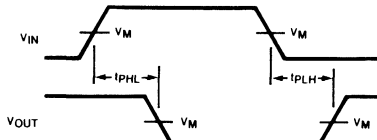
DEFINITIONS

- R_L = Load resistor to V_{CC} ; see data sheet for value.
- C_L = Load capacitance includes jig and probe capacitance; see data for value.
- R_T = Termination resistance should be equal to Z_{out} of Pulse Generators.
- R_1 = Load resistance to V_{CC} ; infinity (∞) means no resistor needed.
- R_2 = Load resistance to 2.6V supply.
- D = Diodes are 1N916, 1N3064, or equivalent.
- R_p = $5k\Omega$ probe impedance, or $5k\Omega$ termination resistor when 10 megohm or FET probe is used.



AC TEST CIRCUITS AND WAVEFORMS

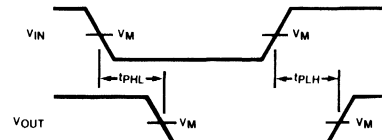
WAVEFORM FOR INVERTING OUTPUTS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families

Waveform 1

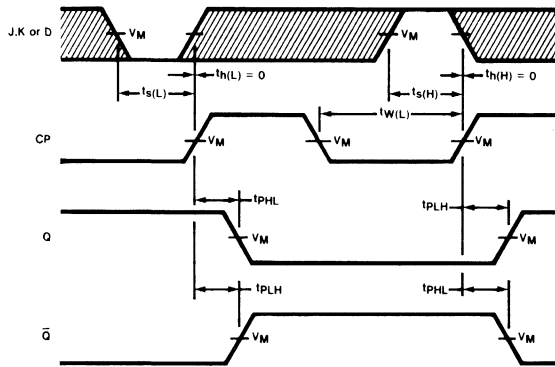
WAVEFORM FOR NON-INVERTING OUTPUTS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families

Waveform 2

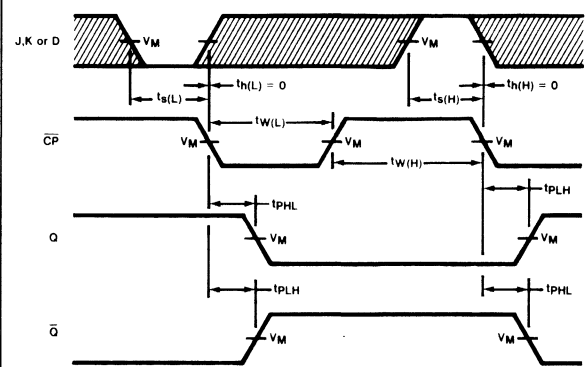
CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3

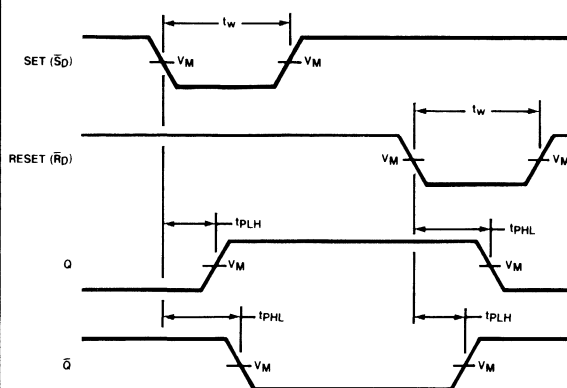
CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4

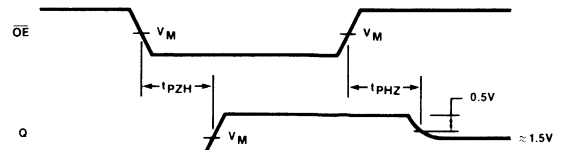
SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families

Waveform 5

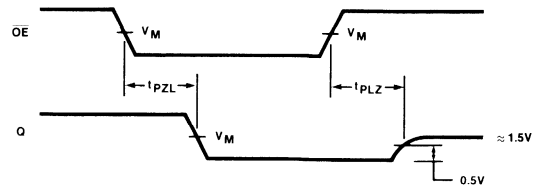
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families

Waveform 6

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families

Waveform 7

SECTION 5

8200 Series

Data Sheets

DESCRIPTION

The 8200/8201/8202/8203 MSI Buffer Registers are arrays of ten clocked "D" flip-flops especially suited for parallel-in parallel-out register applications. They are also suitable for general purpose applications as parallel-in serial-out, serial-in parallel-out registers.

The flip-flops are arranged as dual 5 arrays, (8200 and 8201) and single 10 arrays with reset, (8202 and 8203). The true output of each bit is made available to the user.

The 8200 and 8202 feature true "D" inputs. The logic state presented at these "D" inputs will appear at the Q outputs after a negative transition of the clock.

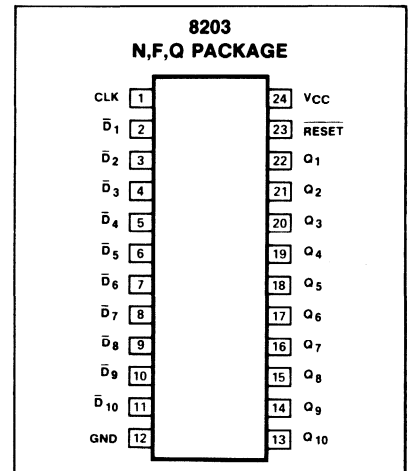
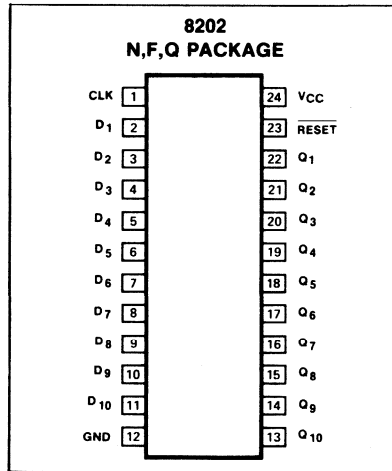
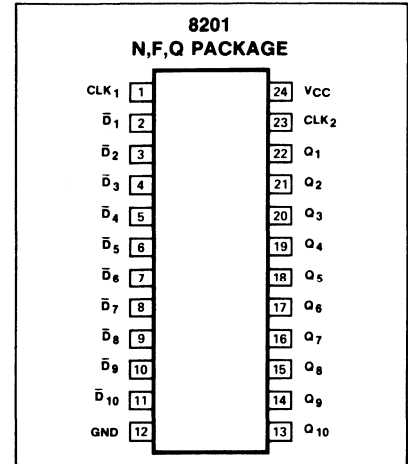
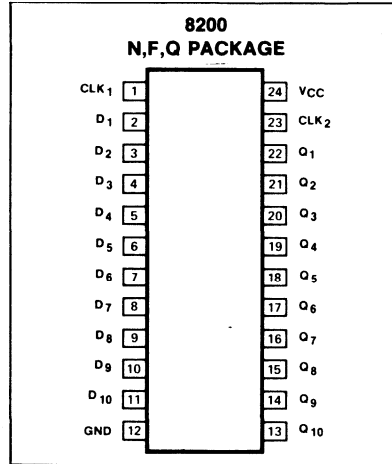
The 8201 and 8203 feature complementing "D" inputs (" \bar{D} "). The logic state presented at these " \bar{D} " inputs will invert and appear at the Q outputs after a negative going transition of the clock. This complementing input feature (" \bar{D} ") permits the use of standard AND-OR-INVERT gates to achieve the AND-OR function without additional gate delays.

TRUTH TABLE

	D_n	\bar{D}_n	RESET	Q_{n+1}
8200	H	—	—	H
	L	—	—	L
8201	—	H	—	L
	—	L	—	H
8202	H	—	H	H
	L	—	H	L
8203	L	—	H	H
	H	—	H	L

H = HIGH voltage level
L = LOW voltage level

PIN CONFIGURATIONS



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+75^\circ C$		MILITARY RANGES $V_{CC} = 5V \pm 5\%$; $T_A = -55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N8200N N8202N	• •	N8201N N8203N
Ceramic DIP	N8200F N8202F	• •	N8201F N8203F	S8200F • S8201F S8202F • S8203F
Flatpak				S8200Q • S8201Q S8202Q • S8203Q

DESCRIPTION

The 8-Input Digital Multiplexer is the logical equivalent of a single-pole, 8 position switch whose position is specified by a 3-bit input address.

The 8230 incorporates an INHIBIT input which, when LOW, allows the one-of-eight inputs selected by the address to appear on the f output and, in complement, on the \bar{f} output. With the INHIBIT input HIGH, the f output is unconditionally LOW and the \bar{f}

output is unconditionally HIGH. The 8230 is a functional and pin-for-pin replacement for the 9312.

The 8231 is a variation of the 8230 that provides open collector output \bar{f} for expansion of input terms. The 8232 is similar to the 8230 except in the effect of the INHIBIT input on the \bar{f} output. With the INHIBIT input LOW, the selected input appears at the f output and, in complement, on the \bar{f} output. With the INHIBIT input HIGH, both the f and the \bar{f} output are unconditionally LOW.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

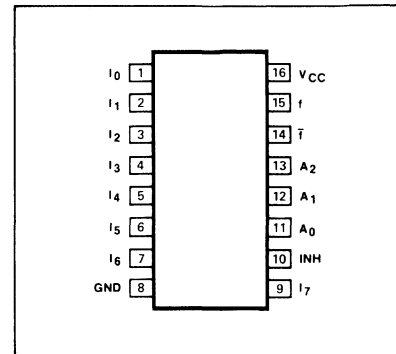
PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $75^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 5\%$; $T_A = -55^\circ C$ to $125^\circ C$
Plastic DIP	N8230N • N8231N • N8232N N82S30N • N82S31N	
Ceramic DIP	N8230F • N8231F • N8232F N82S30F • N82S31F	S8230F • S8231F • S8232F S82S30F • S82S31F
Flatpak		S8230W • S8231W

TRUTH TABLE

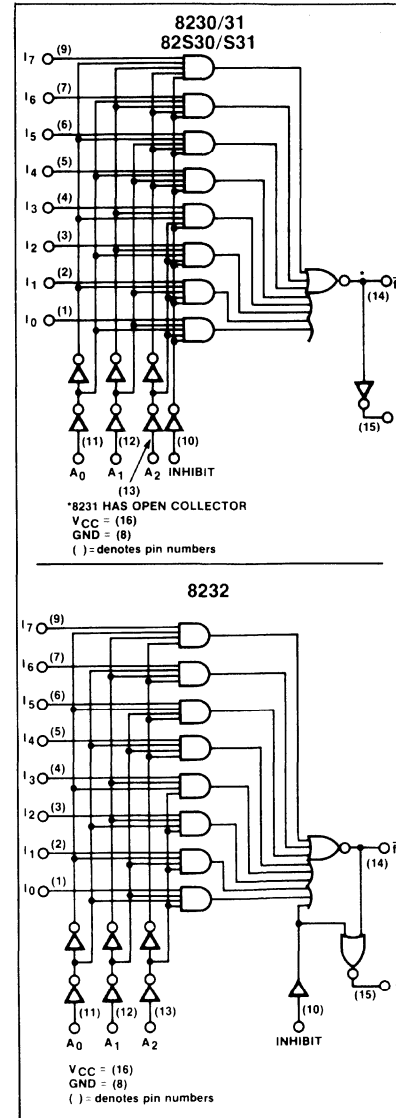
ADDRESS			DATA INPUTS								OUTPUT			
A_2	A_1	A_0	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	INH	f	8230/ 82S30 8231/ 82S31 \bar{f}	8232 \bar{f}
L	L	L	x	x	x	x	x	x	x	H	L	H	L	L
L	L	H	x	x	x	x	x	x	H	x	L	H	L	L
L	H	L	x	x	x	x	x	H	x	x	L	H	L	L
L	H	H	x	x	x	H	x	x	x	x	L	H	L	L
H	L	L	x	x	x	H	x	x	x	x	L	H	L	L
H	L	H	x	x	H	x	x	x	x	x	L	H	L	L
H	H	L	x	H	x	x	x	x	x	x	L	H	L	L
H	H	H	H	x	x	x	x	x	x	x	L	H	L	L
L	L	L	x	x	x	x	x	x	x	L	L	L	H	H
L	L	H	x	x	x	x	x	x	L	x	L	L	H	H
L	H	L	x	x	x	x	L	x	x	x	L	L	H	H
L	H	H	x	x	x	L	x	x	x	x	L	L	H	H
H	L	L	x	x	L	x	x	x	x	x	L	L	H	H
H	L	H	x	L	x	x	x	x	x	x	L	L	H	H
H	H	L	x	L	x	x	x	x	x	x	L	L	H	H
H	H	H	L	x	x	x	x	x	x	x	L	L	H	H
x	x	x	x	x	x	x	x	x	x	x	H	L	H	L

L LOW voltage level
H HIGH voltage level
x Don't care

PIN CONFIGURATION



LOGIC DIAGRAMS



DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8230/31/32			UNIT
		Min	Typ	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -800 μ A	2.6	3.5		V
I _{OH} Output HIGH current f̄ output of 8231 only	V _{CC} = 4.75V, V _{OUT} = 4.5V			150	μ A
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 16mA			0.4	V
I _{IH} Input HIGH current A _n , I _n (all) INH (all)	V _{CC} = 5.25V, V _{IN} = 4.5V			40 80	μ A μ A
I _{IL} Input LOW current A _n , I _n , INH (8230, 8231) INH (8232)	V _{CC} = 5.25V, V _{IN} = 0.4V	-0.1 -0.1		-1.6 -3.2	mA mA
V _{BD} Input voltage rating	V _{CC} = 4.75V, I _{IN} = 10mA	5.5			V
I _{OS} Output short circuit current	V _{CC} = 5V, V _{OUT} = 0V	-20		-70	mA
I _{CC} Supply current 8230, 8231 8232	V _{CC} = 5.25V		35 33	47.7 50	mA mA

DC ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS	82S30/82S31			UNIT
		Min	Typ	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -1.0mA	2.7			V
I _{OH} Output HIGH current f̄ Output of 82S31 only	V _{CC} = 4.75V, V _{OUT} = 4.5V			250	μ A
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 20mA			0.5	V
I _{IH} Input HIGH current	V _{CC} = 5.25V, V _{IN} = 4.5V			10	μ A
I _{IL} Input LOW current	V _{CC} = 5.25V, V _{IN} = 0.5V			-400	μ A
V _{CD} Input clamp voltage	V _{CC} = 4.75V, I _{IN} = -18mA			-1.2	V
I _{OS} Output short circuit current	V _{CC} = 5.25V, V _{OUT} = 0V	-40		-100	mA
I _{CC} Supply current	V _{CC} = 5.25V			62	mA

AC CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8230		8231		8232		UNIT	
		Typ	Max	Typ	Max	Typ	Max		
t _{PLH} t _{PHL}	Propagation delay A _n to \bar{f} output	R _L = 280Ω - Figures 1,2 (See Note a)	19 19	30 30	19 19	30 30	19 19	30 30	ns ns
t _{PLH} t _{PHL}	Propagation delay I _n to \bar{f} output	R _L = 280Ω - Figures 1,2 (See Note a)	13 13	20 20	15 15	24 24	13 13	20 20	ns ns
Δ t _{PLH} Δ t _{PHL}	Prop. delay difference \bar{f} output to f output	R ₁ = 280Ω - Figures 1,2 (See Note a)	10 10	15 15	10 10	15 15	10 10	15 15	ns ns
t _{PLH} t _{PHL}	Propagation delay INH to \bar{f} output	R _L = 280Ω - Figures 1,2 (See Note a)	18 18	30 30	18 18	30 30	13 13	20 20	ns ns
t _{PLH} t _{PHL}	Propagation delay INH to f output	R ₁ = 280Ω - Figures 1,2 (See Note a)					13 13	20 20	ns ns

AC CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS	82S30		82S31		UNIT	
		Typ	Max	Typ	Max		
t _{PLH} t _{PHL}	Propagation delay A _n to \bar{f} output	R _L = 280Ω - Figures 1,2 (See Note a)	14 14	17 17	16 16	19 19	ns ns
t _{PLH} t _{PHL}	Propagation delay I _n to \bar{f} output	R _L = 280Ω - Figures 1,2 (See Note a)	7.0 7.0	10 10	9.0 9.0	12 12	ns ns
Δ t _{PLH} Δ t _{PHL}	Prop. delay difference \bar{f} output to f output	R ₁ = 280Ω - Figures 1,2 (See Note a)	6.0 6.0	9.0 9.0	6.0 6.0	9.0 9.0	ns ns
t _{PLH} t _{PHL}	Propagation delay INH to \bar{f} output	R _L = 280Ω - Figures 1,2 (See Note a)	12 12	16 16	14 14	18 18	ns ns
t _{PLH} t _{PHL}	Propagation delay INH to f output	R ₁ = 280Ω - Figures 1,2 (See Note a)		26 26		28 28	ns ns

NOTE

a. C_L = 30pF for 82; C_L = 15pF for 82S

AC TEST FIGURE

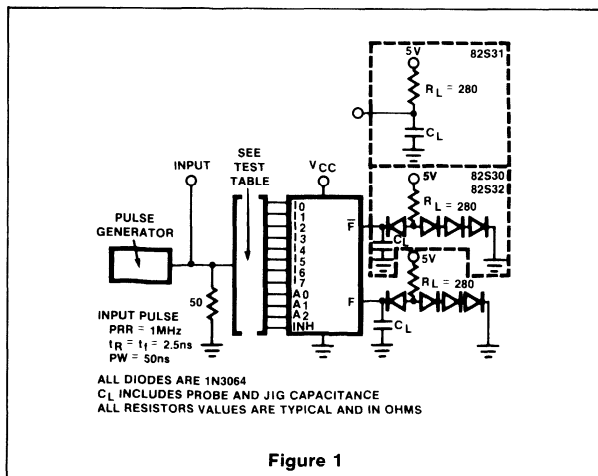


Figure 1

AC WAVEFORMS

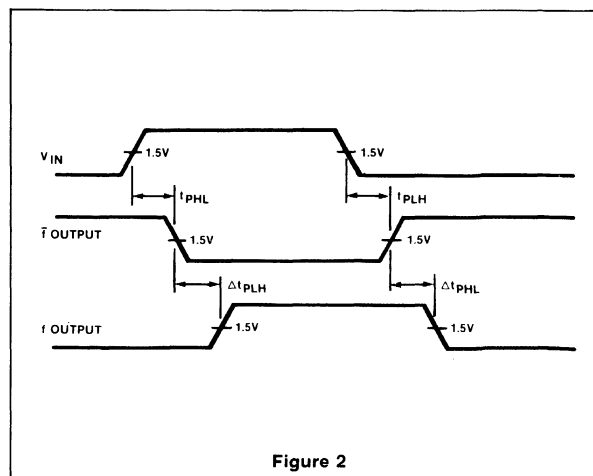


Figure 2

DESCRIPTION

These devices are 2-input 4-bit Digital Multiplexers designed for general purpose data-selection applications.

The 8233 features *non-inverting* data paths; and, the 8234 features *inverting* data paths.

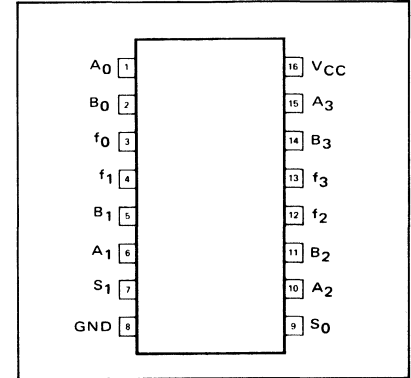
The 8235 is designed for input to adders, registers and general paralleled data handling due to its capability to perform **CONDITIONAL COMPLEMENTING (TRUE / COMPLEMENT)**. When the two inputs for each bit position (A_i, B_i) are connected together, the f output will provide either the *True* or *Complement* of the input data. This capability is especially useful for transferring data into

parallel adders where both true data for adding or multiplying and also complemented data for subtracting or dividing are needed.

The 8234 and 8235 designs have open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty 8234/8235s in the **WIRED-AND** mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

PIN CONFIGURATION



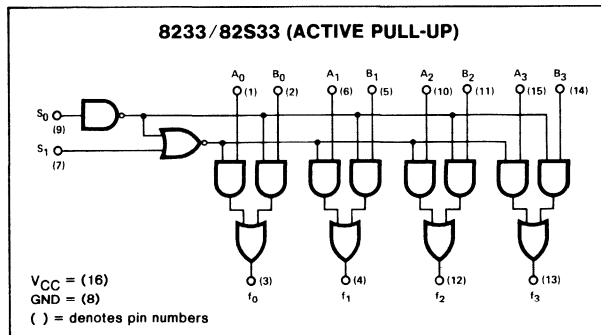
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +75°C	V _{CC} =5V ± 5%; T _A =-55°C to +125°C
Plastic DIP	N8233N • N8234N • N8235N N82S33N • N82S34N	
Ceramic DIP	N8233F • N8234F • N8235F N82S33F • N82S34F	S8233F • S8234F • S8235F
Flatpak		S8233W • S8234W • S8235W

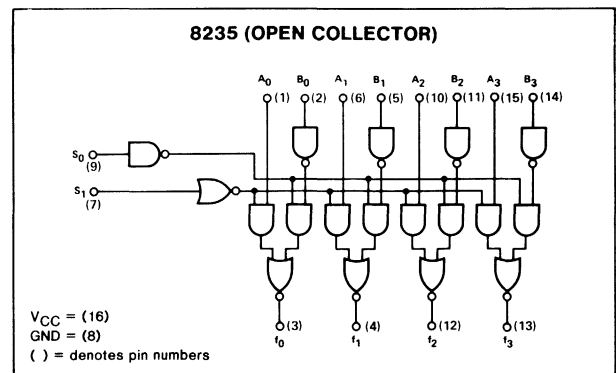
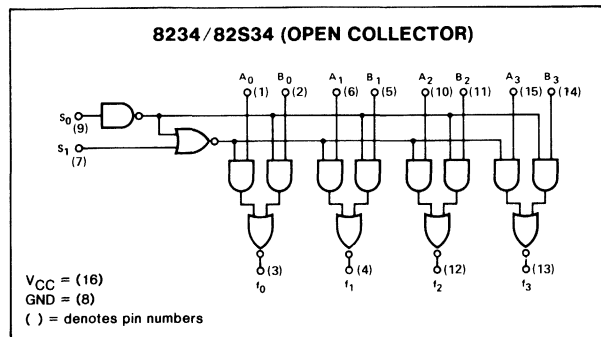
TRUTH TABLE

TYPE	INPUTS		OUTPUT
	S ₀	S ₁	f _n
8233/82S33	L	L	B
	H	L	A
	L	H	B
	H	H	L
8234/82S34	L	L	\overline{B}
	H	L	\overline{A}
	L	H	\overline{B}
	H	H	H
8235	L	L	$\overline{A_n}B_n$
	L	H	B_n
	H	L	$\overline{A_n}$
	H	H	H

LOGIC DIAGRAMS



H = HIGH voltage level
L = LOW voltage level.



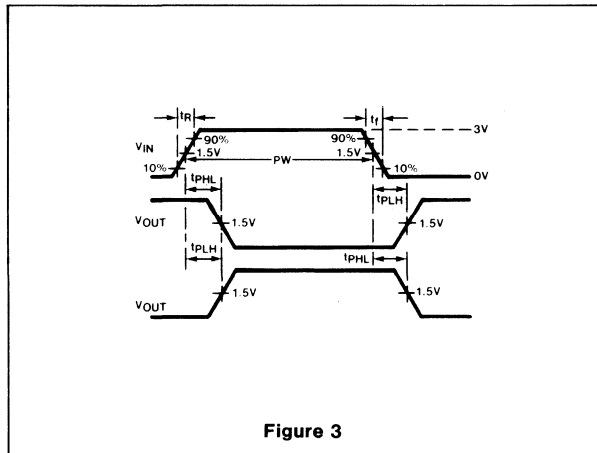
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	8233/34/35		82S33/34		UNIT	
		Min	Max	Min	Max		
V _{OH} Output HIGH voltage	V _{CC} = 4.75V	I _{OH} = -800μA	2.6				V
		I _{OH} = -1.0mA				2.7	V
V _{OL} Output LOW voltage	V _{CC} = 4.75V	I _{OL} = 16mA		0.4			V
		I _{OL} = 20mA				0.5	V
I _{OH} Output HIGH current 8234/35 and 82S34	V _{CC} = 5.25V, V _{OUT} = 5.0V		100			250	μA
I _{IH} Input = LOW current	V _{CC} = 5.25V, V _{IN} = 4.5V		40			10	μA
I _{IL} Input LOW current	V _{CC} = 5.25V, V _{IN} = 0.4V		-1.6			-0.4	mA
V _{BD} Input Breakdown voltage	V _{CC} = 5.25V, I _{IN} = 10mA	5.5					V
V _{CD} Input Clamp current	V _{CC} = 4.75V	I _{IN} = -12mA		-1.5			V
		I _{IN} = -18mA				-1.2	V
I _{OS} Output short circuit current	V _{CC} = 5.25V, V _{OUT} = 0V	-20	-70			-40 -100	mA
I _{CC} Supply current	V _{CC} = 5.0V	8233, 82S33		48		58	mA
		8234, 82S34		40		50	mA
		8235		59			mA

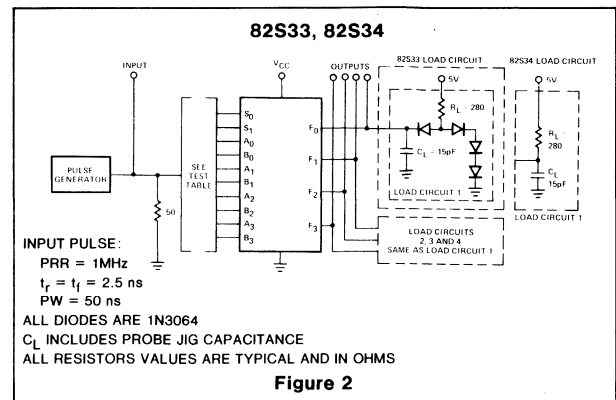
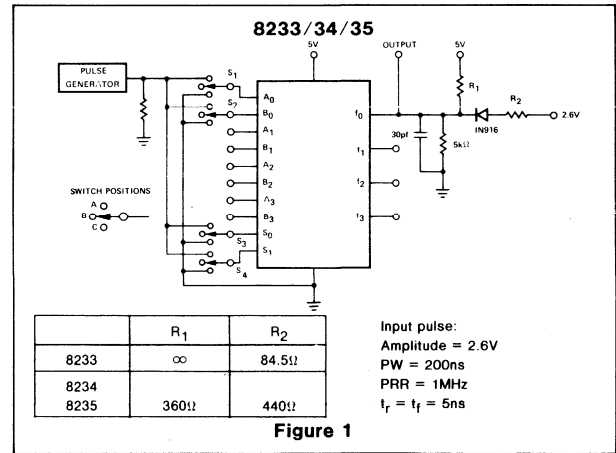
AC CHARACTERISTICS: $T_A=25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8233/34/45		82S33/S34		UNIT
		$C_L = 30\text{pF}$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay A_n to f_n (accept 8235)	Figures 1,2 & 3		25 25		12 12	ns ns
t_{PLH} t_{PHL} Propagation delay B_n to f_n (accept 8235)	Figures 1,2 & 3		25 25		12 12	ns ns
t_{PLH} t_{PHL} Propagation delay A_n to f_n (8235 only)	Figures 1,2 & 3		25 25			ns ns
t_{PLH} t_{PHL} Propagation delay B_n to f_n (8235 only)	Figures 1,2 & 3		35 35			ns ns
t_{PLH} t_{PHL} Propagation delay S_0 to f_n	Figures 1,2 & 3		38 38		18 18	ns ns
t_{PLH} t_{PHL} Propagation delay S_1 to f_n	Figures 1,2 & 3		38 38		16 16	ns ns

AC WAVEFORMS



AC TEST FIGURE



DESCRIPTION

The 8241/82S41 contains four independent gating structures to perform the Exclusive-OR function on two input variables.

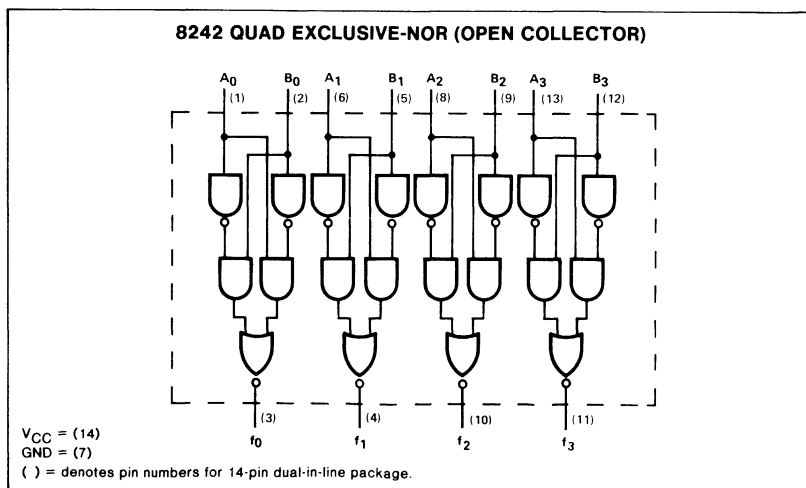
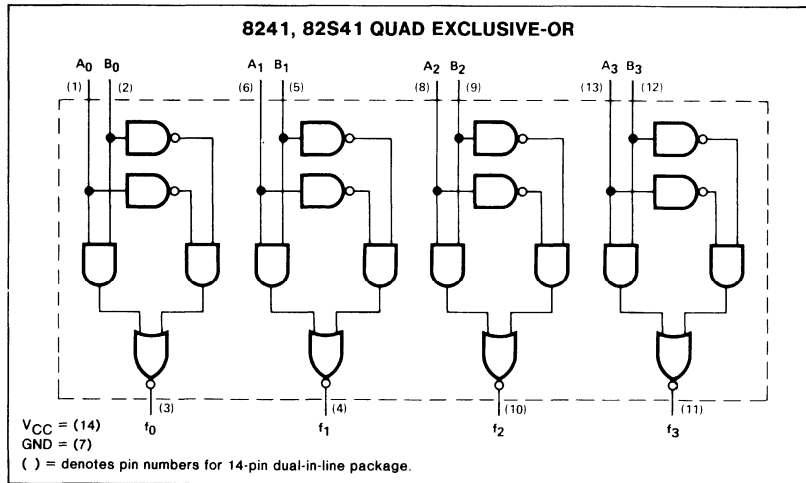
The output of the 8241/82S41 employs the totem-pole structure characteristic of TTL devices.

The 8242/82S42 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The 8242/82S42 outputs are open collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

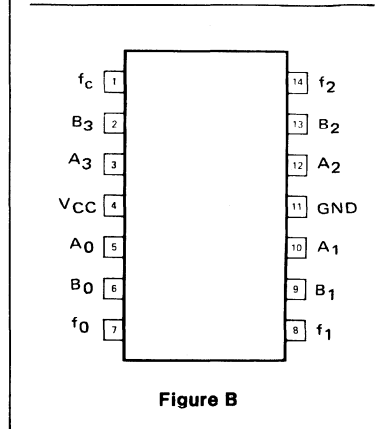
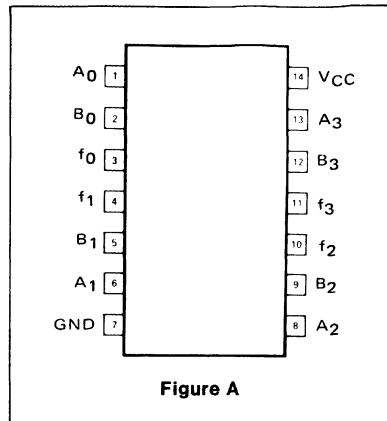
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$		$V_{CC}=5V \pm 5\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N8241N	• N8242N		
	Fig. A	N82S41N	• N82S42N		
Ceramic DIP	Fig. A	N8241F	• N8242F	S8241F	• S8242F
	Fig. A	N82S41F	• N82S42F		
Flatpak	Fig. B			S8241W	• S8242W

LOGIC DIAGRAMS



PIN CONFIGURATION



TRUTH TABLE

TYPE	INPUTS		OUTPUT
	A	B	f
8241/82S41	L	L	L
	H	L	H
	L	H	H
	H	H	L
8242/82S42	L	L	H
	H	L	L
	L	H	L
	H	H	H

NOTE
 H = HIGH voltage level
 L = LOW voltage level

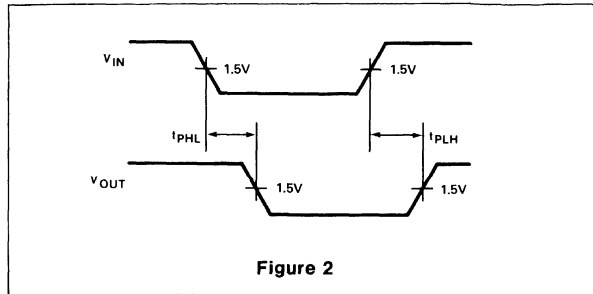
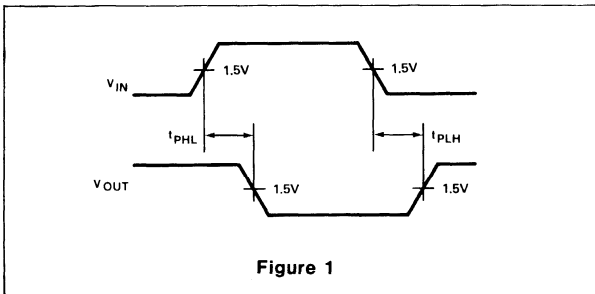
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	8241		8242		82S41		82S42		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} =4.75V	I _{OH} =-800μA	2.6							V
		I _{OH} =-1.0mA					2.7			V
V _{OL} Output LOW voltage	V _{CC} =4.75V	I _{OL} = 16mA		0.4						V
		I _{OL} = 20mA					0.5			V
		I _{OL} = 25mA				0.4			0.5	V
I _{OH} Output HIGH current	V _{CC} = 5.25V V _{OUT} =5.0V					25			250	μA
I _{IH} Input HIGH current	V _{CC} = 5.25V V _{IN} = 4.5V		80		80		10		10	μA
I _{IL} Input LOW current	V _{CC} = 5.25V V _{IN} = 0.4V	-0.1	-3.2	-0.1	-3.2		-0.8		-0.8	mA
V _{BD} Input breakdown voltage	V _{CC} = 5.25V I _{IN} = 10mA	5.5		5.5						V
V _{CD} Input clamp voltage	V _{CC} = 4.75V I _{IN} =-18mA						-1.2		-1.2	V
I _{OS} Output short circuit current	V _{CC} = 5.25V V _{OUT} = 0V	-20	-70			-40	-100			V
I _{CC} Supply current	V _{CC} = 5.25V		57		47.5		55		62	mA

AC CHARACTERISTICS: T_A 25°C $V_{CC} = 5.25V$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8241		8242		82S41		82S42		UNIT
		$C_L = 30pF$		$C_L = 30pF$ $R_1 = \infty$ $R_2 = 84.2\Omega$		$C_L = 15pF$ $R_L = 280\Omega$		$C_L = 15pF$ $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Inverting path	Figures 1, 3 & 4		17 23	23 20	10 10	14 14	14 14	ns ns	
t_{PLH} t_{PHL}	Propagation delay Non-inverting path	Figures 2, 3 & 4		17 23	28 21	10 10	14 14	14 14	ns ns	

AC WAVEFORMS



AC TEST FIGURE

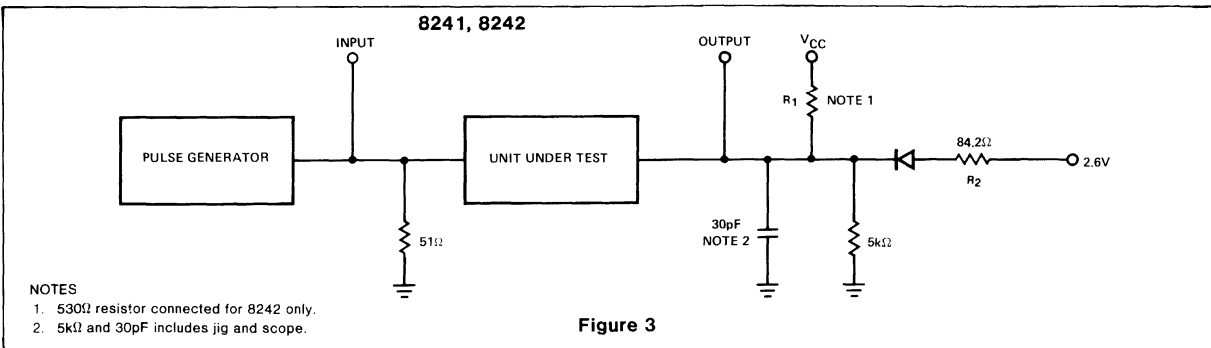


Figure 3

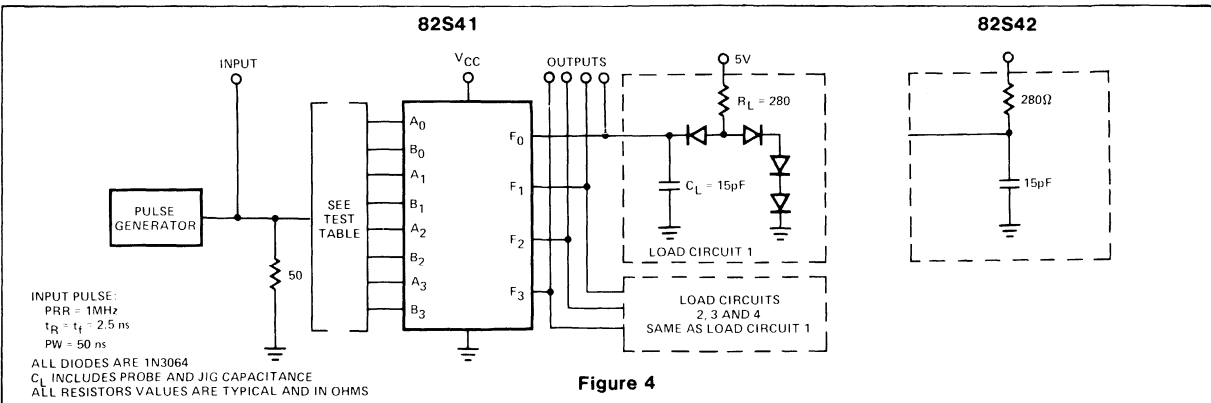


Figure 4

DESCRIPTION

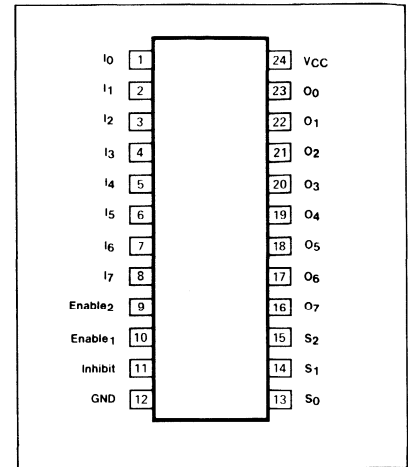
The 8243 8-Bit Position Scaler is an MSI array of approximately 70 gate complexity. The primary function of the 8243 is to scale (or shift) data bit positions by a selection of a 3-bit binary selector code.

The most significant bit input (I_7) may be shifted 8 positions to the least significant bit output (O_0). At zero shift, or scale select, all eight input data bits are transferred and inverted to their respective outputs, (I_0 to O_0 , I_1 to O_1 , I_2 to O_2 , etc.) At a shift, or scale select, of one, each input bit (I_n) will shift to the next lower output bit (O_{n-1}). See truth table for other shift codes.

The 8243's advantages over shift registers are the speed of operation and lower complexity of external logic required to effect a scale function. The speed of the 8243 Scaler is a function of gate propagation delays—the speed equivalent shift registers is the time for clock periods plus the propagation delay to effect a scale function.

The 8243 is provided with open collector outputs to provide expansion to larger scaling functions. Data input logic zero loading is reduced to less than $-100\mu\text{A}$ when the unit is disabled.

PIN CONFIGURATION



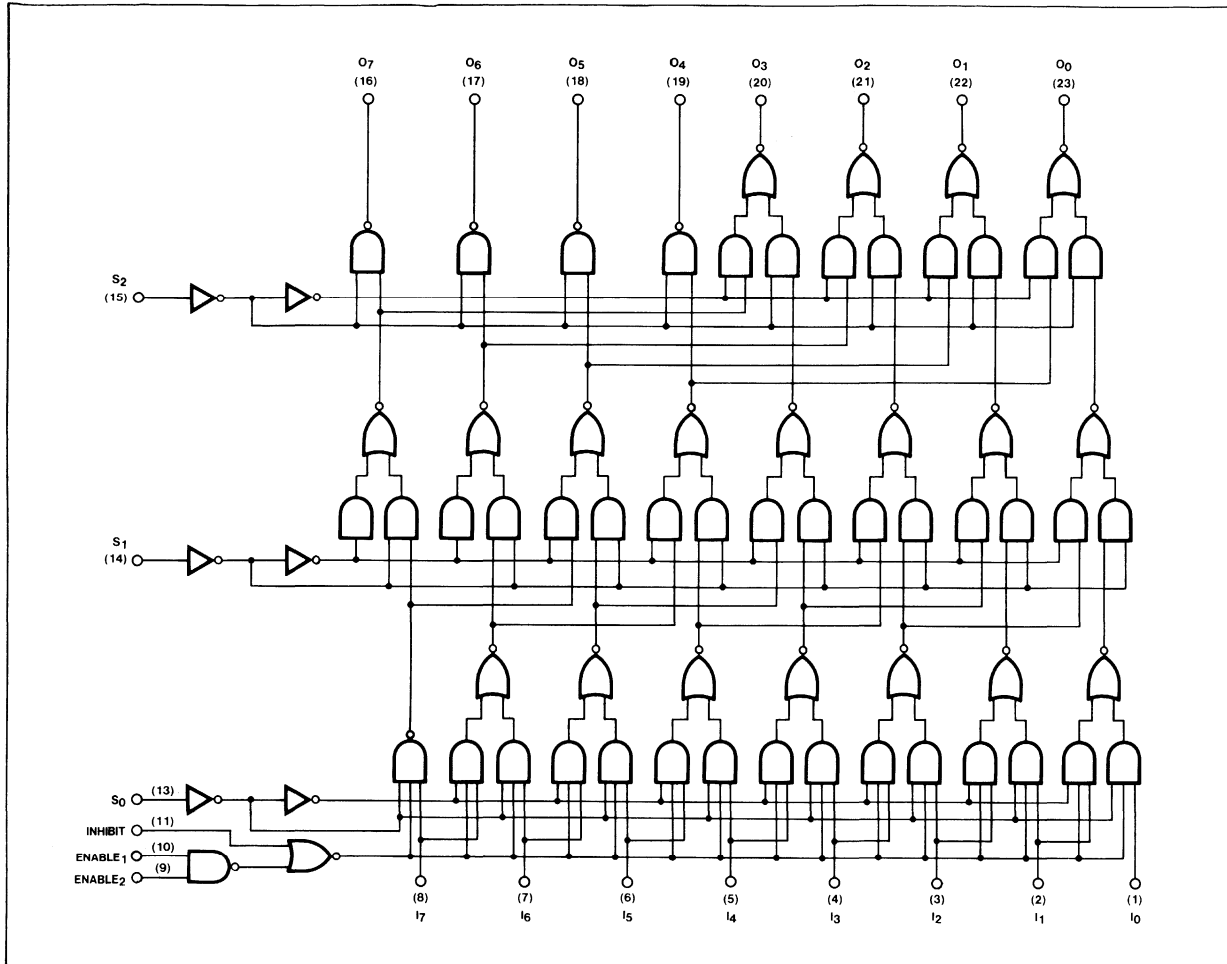
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ\text{C}$ to $+75^\circ\text{C}$	$V_{CC}=5V \pm 5\%$; $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
Plastic DIP	N8243N	
Ceramic DIP	N8243F	S8243F
Flatpak		S8243Q

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	8243		UNIT
		Min	Max	
I_{OH} Output HIGH current	$V_{CC} = 4.75V$, $V_{OUT} = 5.25V$		150	μA
V_{OL} Output LOW voltage	$V_{CC} = 4.75V$, $I_{OL} = 12.8\text{mA}$		0.4	V
I_{IL} Input LOW current Data in (Disabled) Data in (Enabled)	$V_{CC} = 5.25V$, $V_{IN} = 0.4V$ $V_E = 0.8V$		-100 -1.6	μA mA
I_{IH} Input HIGH current Data in Select, Inhibit, Enable 1 & 2	$V_{CC} = 5.25V$, $V_{IN} = 4.5V$		80 40	μA μA
V_{BD} Voltage breakdown	$V_{CC} = 5.0V$, $I_N = 10\text{mA}$	5.5		V
I_{CC} Supply Current	$V_{CC} = 5.25V$,		75.2	mA

LOGIC DIAGRAM



TRUTH TABLE

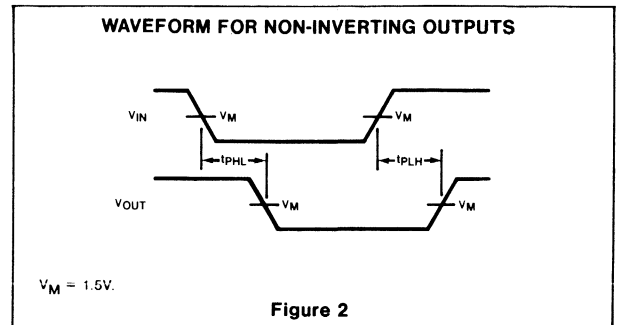
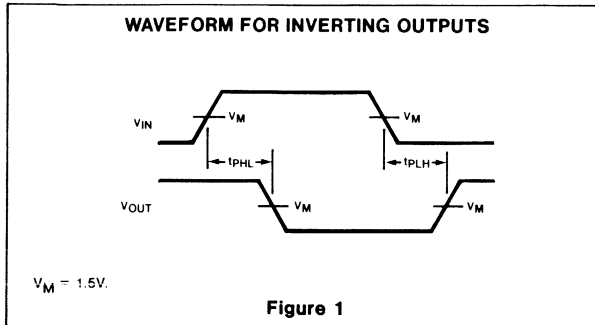
INHIBIT	ENABLE 1 & 2	INPUTS			OUTPUTS							
		S ₀	S ₁	S ₂	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇
L	H	L	L	L	$\bar{1}_0$	$\bar{1}_1$	$\bar{1}_2$	$\bar{1}_3$	$\bar{1}_4$	$\bar{1}_5$	$\bar{1}_6$	$\bar{1}_7$
L	H	H	L	L	$\bar{1}_1$	$\bar{1}_2$	$\bar{1}_3$	$\bar{1}_4$	$\bar{1}_5$	$\bar{1}_6$	$\bar{1}_7$	H
L	H	L	H	L	$\bar{1}_2$	$\bar{1}_3$	$\bar{1}_4$	$\bar{1}_5$	$\bar{1}_6$	$\bar{1}_7$	H	H
L	H	H	H	L	$\bar{1}_3$	$\bar{1}_4$	$\bar{1}_5$	$\bar{1}_6$	$\bar{1}_7$	H	H	H
L	H	L	L	H	$\bar{1}_4$	$\bar{1}_5$	$\bar{1}_6$	$\bar{1}_7$	H	H	H	H
L	H	H	L	H	$\bar{1}_5$	$\bar{1}_6$	$\bar{1}_7$	H	H	H	H	H
L	H	L	H	H	$\bar{1}_6$	$\bar{1}_7$	H	H	H	H	H	H
L	H	H	H	H	$\bar{1}_7$	H	H	H	H	H	H	H
H	X	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	H	H	H	H	H	H	H	H

X indicates either logic H or logic L may be present.
 H = HIGH voltage level
 L = LOW voltage level

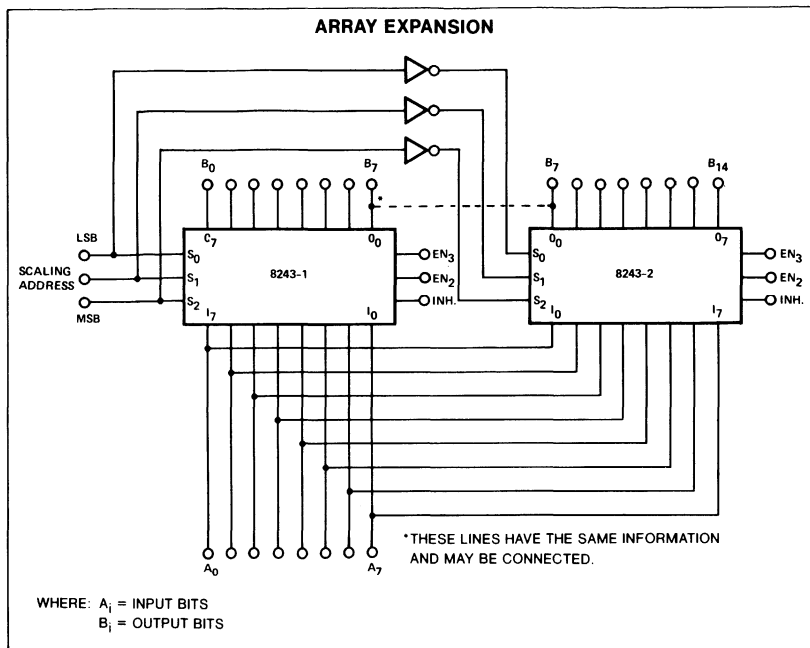
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8243		UNITS
		$C_L = 24\text{pF}$ $R_1 = 480\Omega$ $R_2 = 500\Omega$		
		Min	Max	
t_{PLH} t_{PHL} Propagation delay Data to output	Waveform 1		32 32	ns ns
t_{PLH} t_{PHL} Propagation delay Select to output	Waveforms 1 & 2		40 40	ns ns
t_{PLH} t_{PHL} Propagation delay Inhibit to output	Waveform 2		35 35	ns ns
t_{PLH} t_{PHL} Propagation delay Enable to output	Waveform 1		45 45	ns ns

AC WAVEFORMS



TYPICAL APPLICATIONS



TRUTH TABLE FOR ARRAY EXPANSION

SCALE ADDRESS			8243-1							8243-2								
MSB	LSB		B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}
L	L	L	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7	\bar{A}_7	H	H	H	H	H	H	H
L	L	H	H	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_6	\bar{A}_7	H	H	H	H	H	H
L	H	L	H	H	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_5	\bar{A}_6	\bar{A}_7	H	H	H	H	H
L	H	H	H	H	H	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7	H	H	H	H
H	L	L	H	H	H	H	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7	H	H	H
H	L	H	H	H	H	H	H	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7	H	H
H	H	L	H	H	H	H	H	H	\bar{A}_0	\bar{A}_1	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7	H
H	H	H	H	H	H	H	H	H	H	\bar{A}_0	\bar{A}_0	\bar{A}_1	\bar{A}_2	\bar{A}_3	\bar{A}_4	\bar{A}_5	\bar{A}_6	\bar{A}_7

DESCRIPTION

The 8250, 8251 and 8252 are gate arrays for decoding and logic conversion applications. The 8250 converts 3 lines of input to a one-of-eight output. The fourth input line (D) is utilized as an inhibit to allow use in larger decoding networks.

The 8251 and 8252 convert a 4 line input code (with 1-2-4-8 weighting) to a one-of-ten output as shown in the Truth Table.

The 8252 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs.

The selected output is LOW.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$	$V_{CC}=5V \pm 5\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig. A	N8250N • N82S50N	
	Fig. C	N8251N • N8252N • N82S52N	
Ceramic DIP	Fig. A	N8250F • N82S50F	S8250F
	Fig. C	N8251F • N8252F • N82S52F	S8251F • S8252F
Flatpak	Fig. B		S8250W
	Fig. C		S8251W • S8252W

TRUTH TABLE

INPUT STATE				OUTPUT STATES											
				8250/82S50					8251/8252/82S52						
A	B	C	D	0	1	2	3	4	5	6	7	8	9	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
H	H	L	L	L	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H	H	H	H
H	H	H	L	L	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	L	H	L	H
H	L	L	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	H	L	H	H	H
H	H	L	H	L	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	L	H	H	H
H	L	H	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H

PIN CONFIGURATIONS

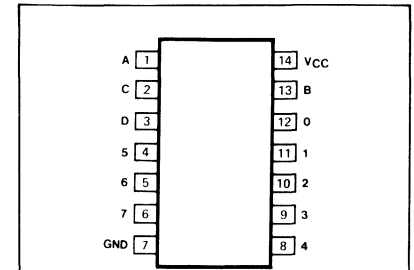


Figure A

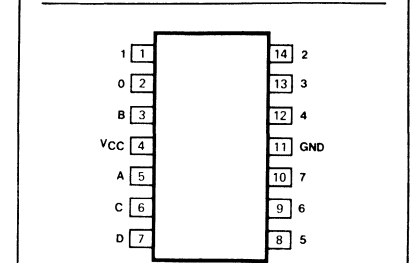


Figure B

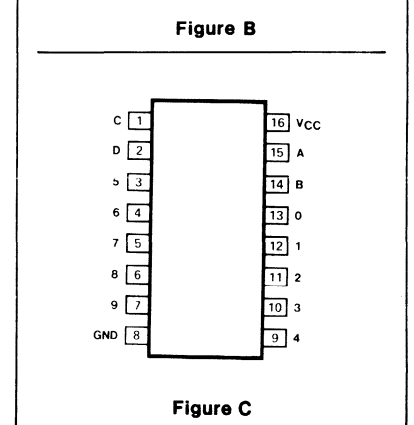
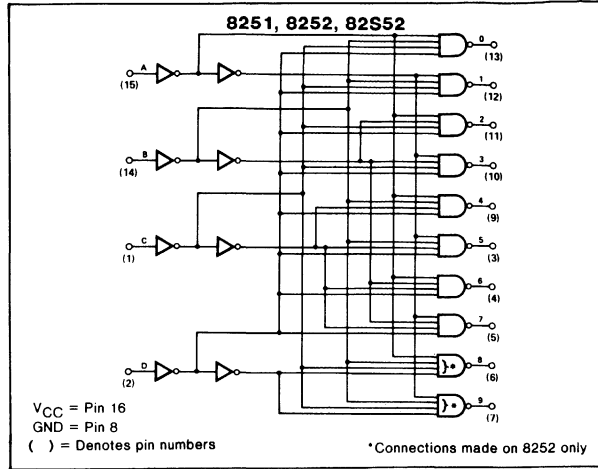
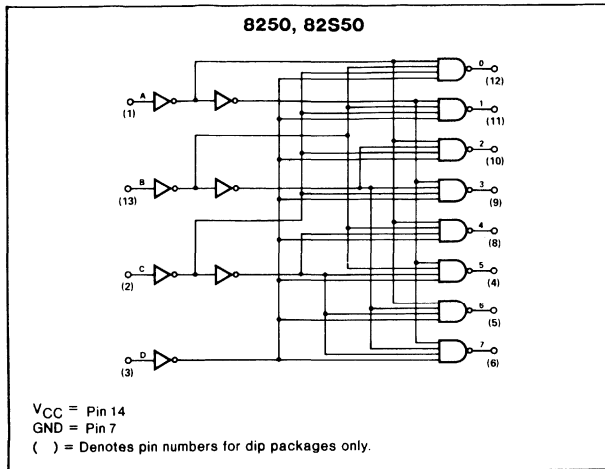


Figure C

LOGIC DIAGRAMS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	8250/51/52		UNIT
		Min	Max	
I_{OH} Output HIGH voltage	$V_{CC} = 4.75V, V_{OUT} = 5.25V$	2.6		V
V_{OL} Output LOW voltage	$V_{CC} = 4.75V, I_{OL} = 16mA$		0.4	V
I_{IH} Input HIGH current	$V_{CC} = 5.25V, V_{IN} = 4.5V$		40	μA
I_{IL} Input LOW current A,B,C, (8250/51) A,B,C,D (8252) D (8251 only) D (8250 only)	$V_{CC} = 5.25V, V_{IN} = 0.4V$		-1.2	mA
			-1.6	mA
			-1.2	mA
			-1.0	mA
V_{BD} Voltage Breakdown	$V_{CC} = 5.0V, I_{IN} = 10mA$	5.5		V
I_{CC} Supply Current (8250 only) (8251 and 8252)	$V_{CC} = 5.0V, V_{OUT} = 0V$		23.8	mA
			25.7	mA

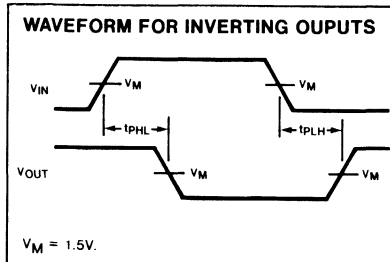
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	82S50/S52		UNIT
		Min	Max	
I_{OH} Output HIGH voltage	$V_{CC} = 4.75V, V_{OUT} = 5.25V$	2.7		V
V_{OL} Output LOW voltage	$V_{CC} = 4.75V, I_{OL} = 20mA$		0.5	V
I_{IH} Input HIGH current	$V_{CC} = 5.25V, V_{IN} = 4.5V$		10	μA
I_{IL} Input LOW current	$V_{CC} = 5.25V, V_{IN} = 0.5V$		-400	μA
V_{CD} Input clamp voltage	$V_{CC} = 5.0V, I_{IN} = -18mA$		-1.2	V
I_{CC} Supply Current (82S50 only) (82S52 only)	$V_{CC} = 5.0V$		72	mA
			85	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8250/51/52		82S50/S52		UNIT
		$C_L = 30\text{pF}$ $R_1 = \infty\Omega$ $R_2 = 84.5\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Input to output	Waveform 1		35		16	ns
			35		16	ns

AC WAVEFORM



DESCRIPTION

The 8262 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 8262. (A logic HIGH on the INHIBIT input forces both outputs to a logic LOW).

When used as a Parity Generator, the 8262 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the 8262 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N8262N	• N82S62N		
Ceramic DIP	Fig. A	N8262F	• N82S62F		S8262F
Flatpak	Fig. B				S8262W

PIN CONFIGURATION

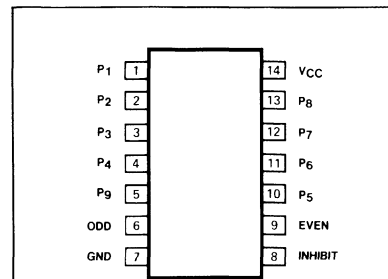


Figure A

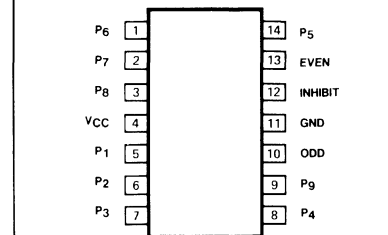
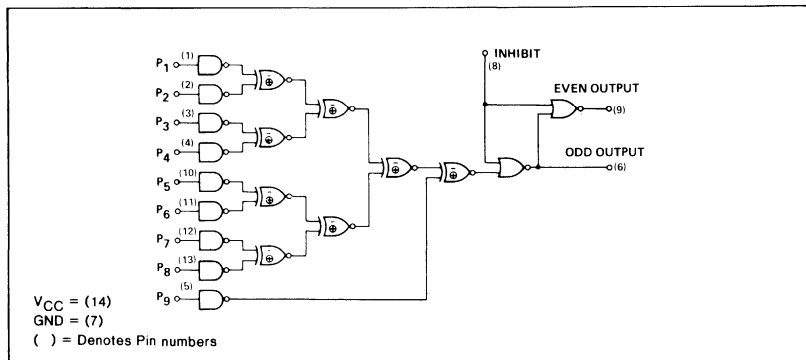


Figure B

LOGIC DIAGRAM



LOGIC EQUATIONS

Odd =
 $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8$
 $\oplus P_9$
 Even =
 $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8$
 $\oplus P_9$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	8262		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = Max, I _{OH} = -800 μ A	2.6		V
V _{OL} Output LOW voltage	V _{CC} = 4.75, I _{OL} = 16mA		0.40	V
I _{IH} Input HIGH current Data inputs Inhibit inputs	V _{CC} = Max, V _{IN} = 4.5V		80 160	μ A μ A
I _{IL} Input LOW current Data inputs Inhibit inputs	V _{CC} = Max, V _{IN} = 0.4V		-1.6 -3.2	mA mA
V _{BD} Voltage breakdown	V _{CC} = Max, I _{IN} = 10mA	5.5		V
I _{OS} Output short circuit-current	V _{CC} = Max, V _{OUT} = 0V	-20	-70	mA
I _{CC} Supply current	V _{CC} = Max		70	mA

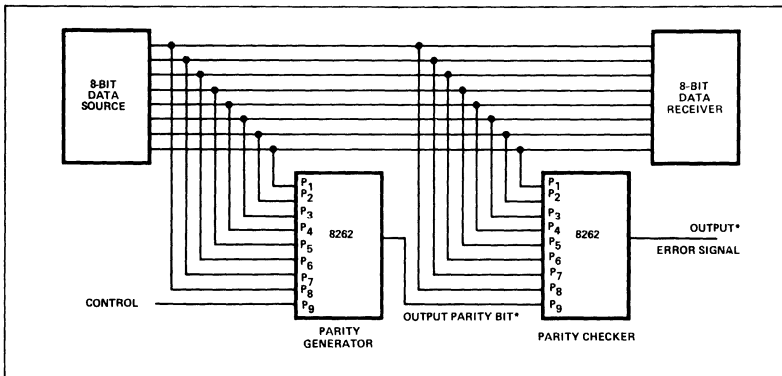
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	82S62		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = - /mA	2.7		V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 20mA		0.5	V
I _{IH} Input HIGH current	V _{CC} = Max, V _{IN} = 4.5V		10	μ A
I _{IL} Input LOW current Data inputs P ₁ -P ₈ Data input P ₉ & Inhibit input	V _{CC} = Max, V _{IN} = 0.5V		-800 -1.2	μ A mA
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-30	-100	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

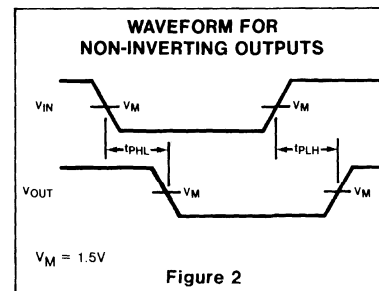
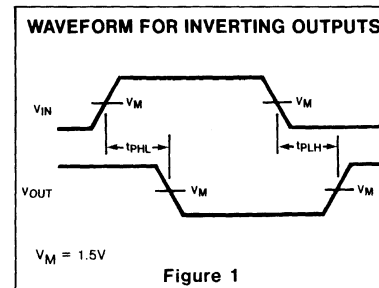
PARAMETER	TEST CONDITIONS	8262		82S62		UNIT
		$C_L = 30\text{pF}$ $R_L = 84.5\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $P_1 - P_8$ to even		50 55		23 23	ns ns
t_{PLH} t_{PHL}	Propagation delay $P_1 - P_8$ to odd		45 45		34 34	ns ns
t_{PLH} t_{PHL}	Propagation delay P_9 to even		35 40		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay P_9 to odd		30 35		18 18	ns ns
t_{PLH} t_{PHL}	Propagation delay Inhibit to even		15 18		9 9	ns ns
t_{PLH} t_{PHL}	Propagation delay Inhibit to odd		15 18		9 9	ns ns

TYPICAL APPLICATION



*Output can be conditioned for odd or even parity.
 An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.
 An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.

AC WAVEFORMS



DESCRIPTION

The 8263/8264 3-Input, 4-Bit Multiplexer is a gating array whose function is analogous to that of a 4-pole, 3-position switch. Four bits of digital data are selected from one of three inputs. A 2-bit channel-selection code determines which input is to be active.

The Data Complement input controls the conditional complement circuit at the Multiplexer output to effect either inverting or non-inverting data flow.

The 8263 employs active output structures to effect minimum delays: the 8264 utilizes bare collector outputs for expansion of input terms.

The 8264 may be expanded by connecting its outputs to the outputs of another 8264. Provision is made for use of a 3-bit code to determine which Multiplexer is selected; thus, eight Multiplexers may be commoned to effect a 4-pole, 24-position switch.

PIN CONFIGURATIONS

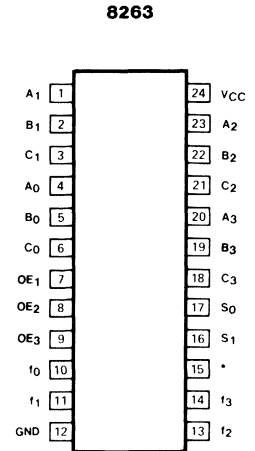


Figure A

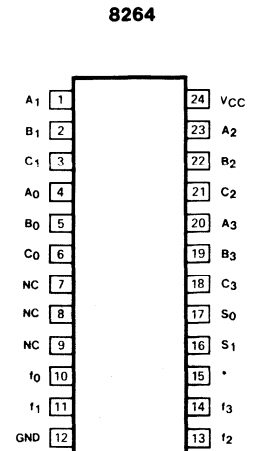


Figure B

*Data complement

ORDERING CODE (See Section 9 for further Package and Ordering Information)

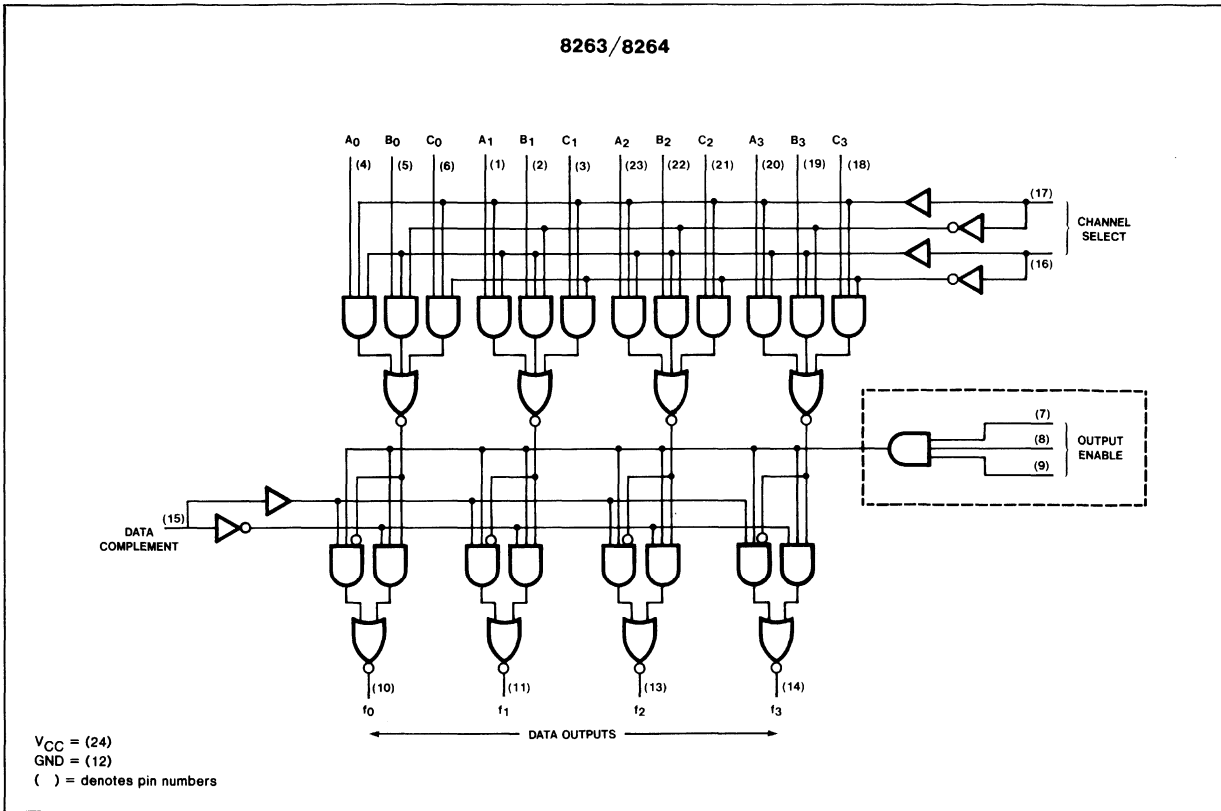
PACKAGES	PIN CONF.	COMMERCIAL RANGES	MILITARY RANGES
		V _{CC} =5V ± 5%; T _A =0°C to +75°C	V _{CC} =5V ± 5%; T _A =-55°C to +125°C
Plastic DIP	Fig.A Fig.B	N8263N N8264N	
Ceramic DIP	Fig.A Fig.B	N8263F N8264F	S8263F S8264F
Flatpak	Fig.A Fig.B		S8263Q S8264Q

TRUTH TABLE

DATA INPUT			CHANNEL SELECT		DATA COMPLEMENT	OUTPUT ENABLE (8264)	DATA OUTPUTS
A _n	B _n	C _n	S ₀	S ₁			
A _n	X	X	H	H	L	H	A _n
X	B _n	X	L	H	L	H	B _n
X	X	C _n	H	L	L	H	C _n
X	X	X	L	L	L	H	0
A _n	X	X	H	H	H	H	\bar{A}_n
X	B _n	X	L	H	H	H	\bar{B}_n
X	X	C _n	H	L	H	H	\bar{C}_n
X	X	X	L	L	H	H	H
X	X	X	X	X	X	L	H

H = HIGH
L = LOW
X = Don't care

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8263		8264		UNIT
		Min	Max	Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -800μA	2.6				V
I _{OH} Output HIGH current	V _{CC} = 4.75V, V _{OUT} = 2.0V				200	μA
V _{OL} Output LOW voltage 8263 8264	V _{CC} = 4.75V, I _{OL} = 9.6mA I _{OL} = 16.mA		0.4		0.4	V
I _{IL} Input LOW current A _n , B _n , C _n , OE, DC S ₀ , S ₁	V _{CC} = 5.25V, V _{IN} = 4.5V		-1.6 -3.2		-1.6 -3.2	mA mA
I _{IH} Input HIGH current A _n , B _n , C _n , OE, DC S ₀ , S ₁	V _{CC} = 5.25V, V _{IN} = 4.5V		40 80		40 80	μA μA
I _{OS} Output short circuit current	V _{CC} = 5V, V _{OUT} = 0V	-20	-70			mA
I _{CC} Supply current	V _{CC} = 5.25V		80		90.4	mA

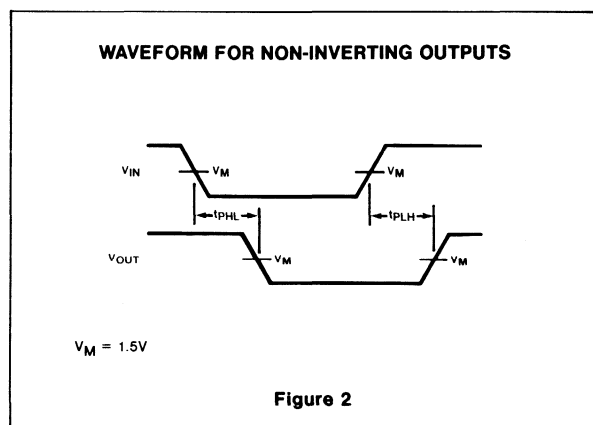
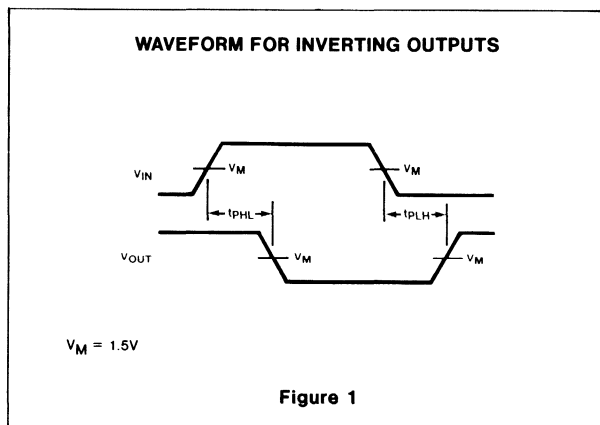
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8263		8264		UNIT
		$C_L = 18\text{pF}$ $R_1 = \infty\Omega$ $R_2 = 150\Omega$		$C_L = 30\text{pF}$ $R_1 = 360\Omega$ $R_2 = 440\Omega$		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay A_n to f_n		26 26		36 36	ns ns
t _{PLH} t _{PHL}	Propagation delay S_0, S_1 to f_n		36 36		36 36	ns ns
t _{PLH} t _{PHL}	Propagation delay DC to f_n		26 26		30 30	ns ns
t _{PLH} t _{PHL}	Propagation delay OE to f_n				30 30	ns ns

NOTE

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC WAVEFORMS



DESCRIPTION

The 8266/8267 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing familiar TTL circuit structures. The 8267 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

The multiplexer is able to choose from two different input sources, each containing 4

bits: $A = (A_0, A_1, A_2, A_3)$, $B = (B_0, B_1, B_2, B_3)$. The selection is controlled by the input S_0 , while the second control input, S_1 , is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform ADDITION/SUBTRACTION. Further, the inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

PIN CONFIGURATION

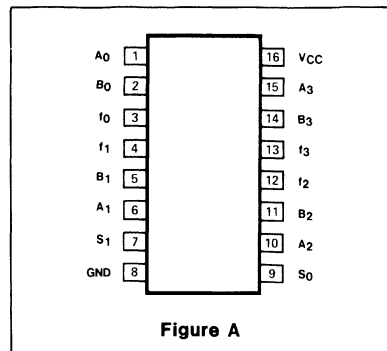


Figure A

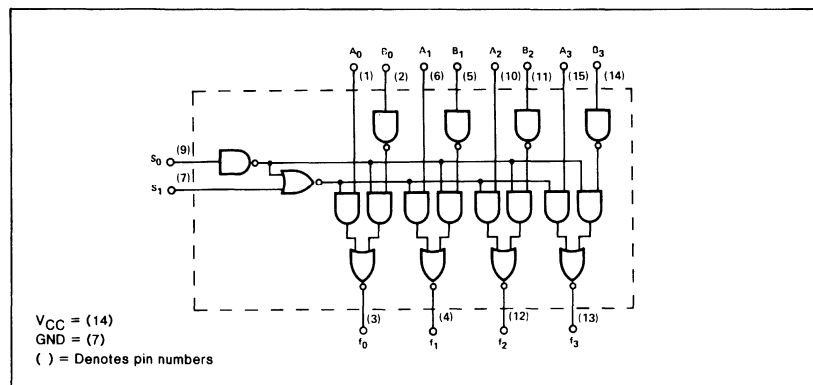
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$		MILITARY RANGES $V_{CC}= 5V \pm 5\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig.A	N8266N N82S66N	• •	N8267N N82S67N	
Ceramic DIP	Fig. A	N8266F N82S66F	• •	N8267F N82S67F	S8266F • S8267F
Flatpak	Fig. A				S8266W • S8267W

TRUTH TABLE

SELECT LINES		OUTPUTS
S_0	S_1	$f_n(0, 1, 2, 3)$
L	L	B_n
L	H	$\overline{B_n}$
H	L	A_n
H	H	H

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	82S66		82S67		UNIT
		Min	Max	Min	Max	
V _{OH}	Output HIGH voltage V _{CC} = 4.75V, I _{OH} = -800 μ A (8266)	2.6				V
V _{OL}	Output LOW voltage V _{CC} = 4.75V, I _{OL} = 16mA		0.4		0.4	V
I _{OH}	Output HIGH current V _{CC} = 5.25V, V _{OUT} = 5.25V				250	μ A
I _{IH}	Input HIGH current V _{CC} = MAX, V _{IN} = 4.5V		40		40	μ A
I _{IL}	Input LOW current V _{CC} = MAX, V _{IN} = 0.4V		-1.6		-1.6	mA
V _{BD}	Voltage breakdown V _{CC} = 4.75V, I _{IN} = 10mA		5.5		5.5	V
I _{OS}	Output short circuit current V _{CC} = 5.25V, V _{OUT} = 0V	-20	-70			mA
I _{CC}	Supply current V _{CC} = 5.0V		52.4		52.4	mA

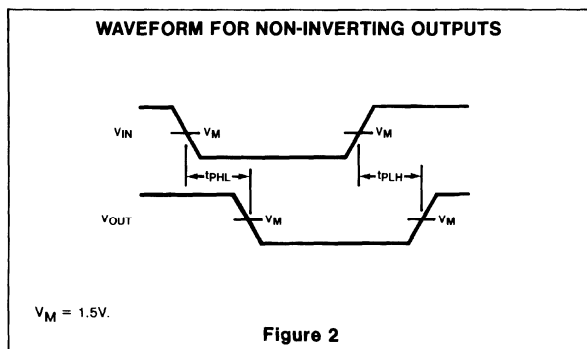
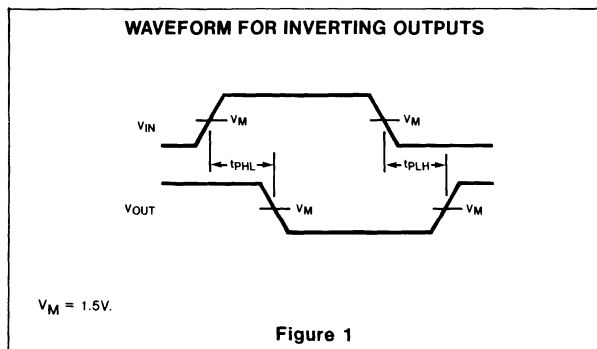
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	8266		8267		UNIT
		Min	Max	Min	Max	
V _{OH}	Output HIGH voltage V _{CC} = 4.75V, I _{OH} = -1mA (82S66)	2.7				V
V _{OL}	Output LOW voltage V _{CC} = 4.75V, I _{OL} = 20mA		0.5		0.5	V
I _{OH}	Output HIGH current V _{CC} = 5.25V, V _{OUT} = 5.25V				25	μ A
I _{IH}	Input HIGH current V _{CC} = MAX, V _{IN} = 4.5V		10		10	μ A
I _{IL}	Input LOW current V _{CC} = MAX, V _{IN} = 0.4V		-400		-400	μ A
I _{OS}	Output short circuit current V _{CC} = 5V, V _{OUT} = 0V	-40	-100			mA
I _{CC}	Supply current V _{CC} = 5.25V		69		69	mA

AC CHARACTERISTICS: T_A 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8266		8267		82S66		82S67		UNITS
		C _L = 30pF R ₁ = ∞Ω R ₂ = 84.5Ω		C _L = 30pF R ₁ = 330Ω R ₂ = 470Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay S ₀ to f _n (short path)	Figure 2		28 28	28 28	18 18	18 18	20 20	20 20	ns ns
t _{PLH} t _{PHL}	Propagation delay S ₀ to f _n (long path)	Figure 1		30 30	36 36	18 18	18 18	20 20	20 20	ns ns
t _{PLH} t _{PHL}	Propagation delay A _n to f _n	Figure 1		20 20	20 20	10 10	10 10	12 12	12 12	ns ns
t _{PLH} t _{PHL}	Propagation delay S ₁ to f _n	Figure 2		25 25	28 28	15 15	15 15	18 18	18 18	ns ns
t _{PLH} t _{PHL}	Propagation delay B _n to f _n	Figure 2		25 25	28 28	12 12	12 12	15 15	15 15	ns ns

AC WAVEFORMS



DESCRIPTION

The 8270 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

The internal design uses level sensitive binaries which respond to the negative-going clock transition. A buffer clock driver has been included to minimize input clock loading.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control. The truth table for the control modes is shown below.

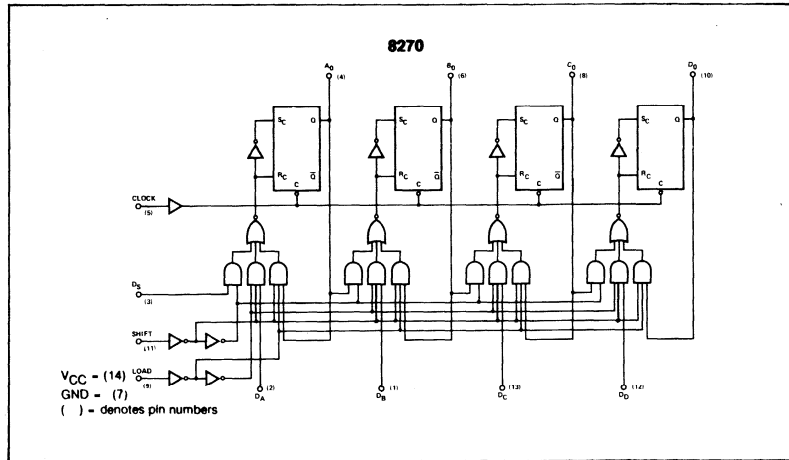
For applications not requiring the hold mode, the load input may be tied high and the shift input used as the mode control.

The 8271 provides a direct reset (R_D), and a \bar{D}_{out} line in addition to the available outputs of the 8270 element. The fan-out specification for this output is the same as the true outputs of the 8270 element.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$		$V_{CC}=5V \pm 5\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig.A	N8270N	•	N82S70N	
	Fig.C	N8271N	•	N82S71N	
Ceramic DIP	Fig.A	N8270F	•	N82S70F	S8270F
	Fig.C	N8271F	•	N82S71F	S8271F
Flatpak	Fig.B				S8270W
	Fig.A				S8271W

LOGIC DIAGRAM



PIN CONFIGURATIONS

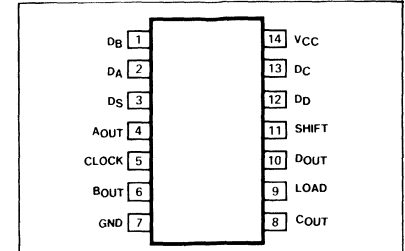


Figure A

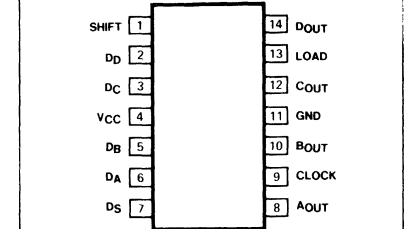


Figure B

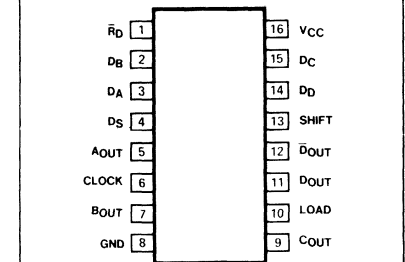


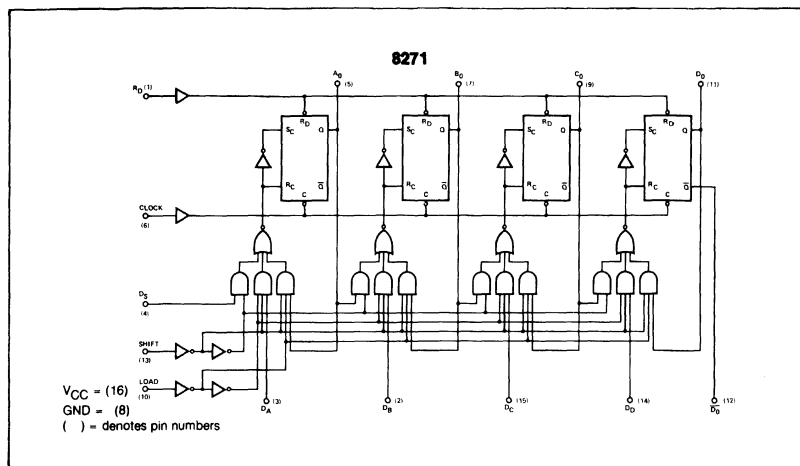
Figure C

MODE SELECT—
FUNCTION TABLE

CONTROL STATE	LOAD	SHIFT
Hold	L	L
Parallel Entry	H	L
Shift Right	L	H
Shift Right	H	H

H = HIGH voltage level
L = LOW voltage level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	8270		8271		UNIT
		Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -800μA		2.6		V
V _{OL}	Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 11.2mA			0.4	V
I _{IH}	Input HIGH current Reset 8271 only	V _{CC} = 5.25V, V _{IN} = 4.5V			40 40	μA μA
I _{IL}	Input LOW current	V _{CC} = 5.25V, V _{IN} = 0.4V			-1.2	mA
V _{BD}	Voltage breakdown	V _{CC} = 5.25V, I _{IN} = 10mA		5.5		V
I _{CC}	Supply current	V _{CC} = 5.25V			47	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	82S70		82S71		UNIT
		Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = 1.0mA		2.7		V
V _{OL}	Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 20mA			0.5	V
I _{IH}	Input HIGH current Reset 82S71 only	V _{CC} = 5.25V			10 10	μA μA
I _{IL}	Input LOW current Load, Data, Clock inputs Shift, Reset (82S71 only)	V _{CC} = 5.25V, V _{IN} = 0.5V			-400 -800	μA μA
V _{BD}	Voltage breakdown	V _{CC} = 4.75V, I _{IN} = 1mA		5.5		V
V _{CD}	Input clamp voltage	V _{CC} = 4.75, I _{IN} = -18mA			-1.2	V
I _{CC}	Supply current	V _{CC} = 5.25V			90	mA

Note

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

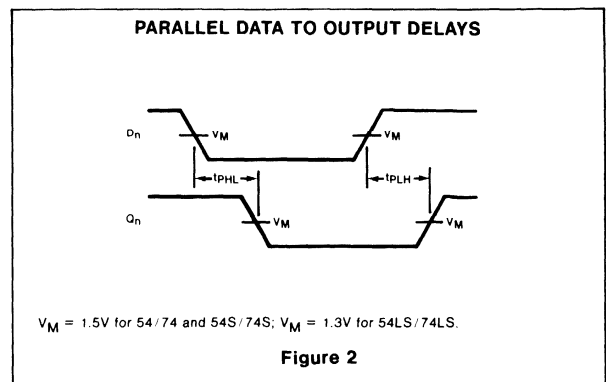
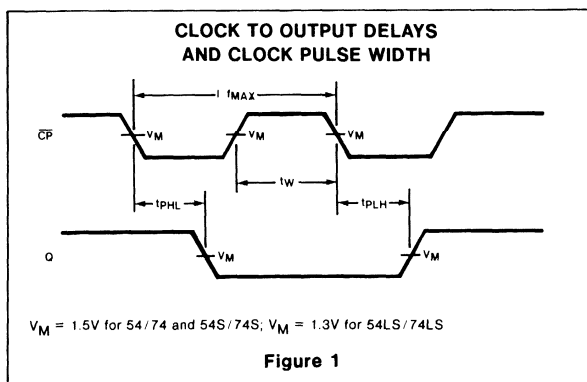
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8270/71		82S70/S71		UNIT
		$C_L = 21\text{pF}$ $R_1 = \infty\Omega$ $R_2 = 127\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Figure 1	15		40		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Figure 1		40 40		20 20	ns ns
t_{PLH} Propagation delay t_{PHL} Reset to output	Figure 2		40 40		16 16	ns ns

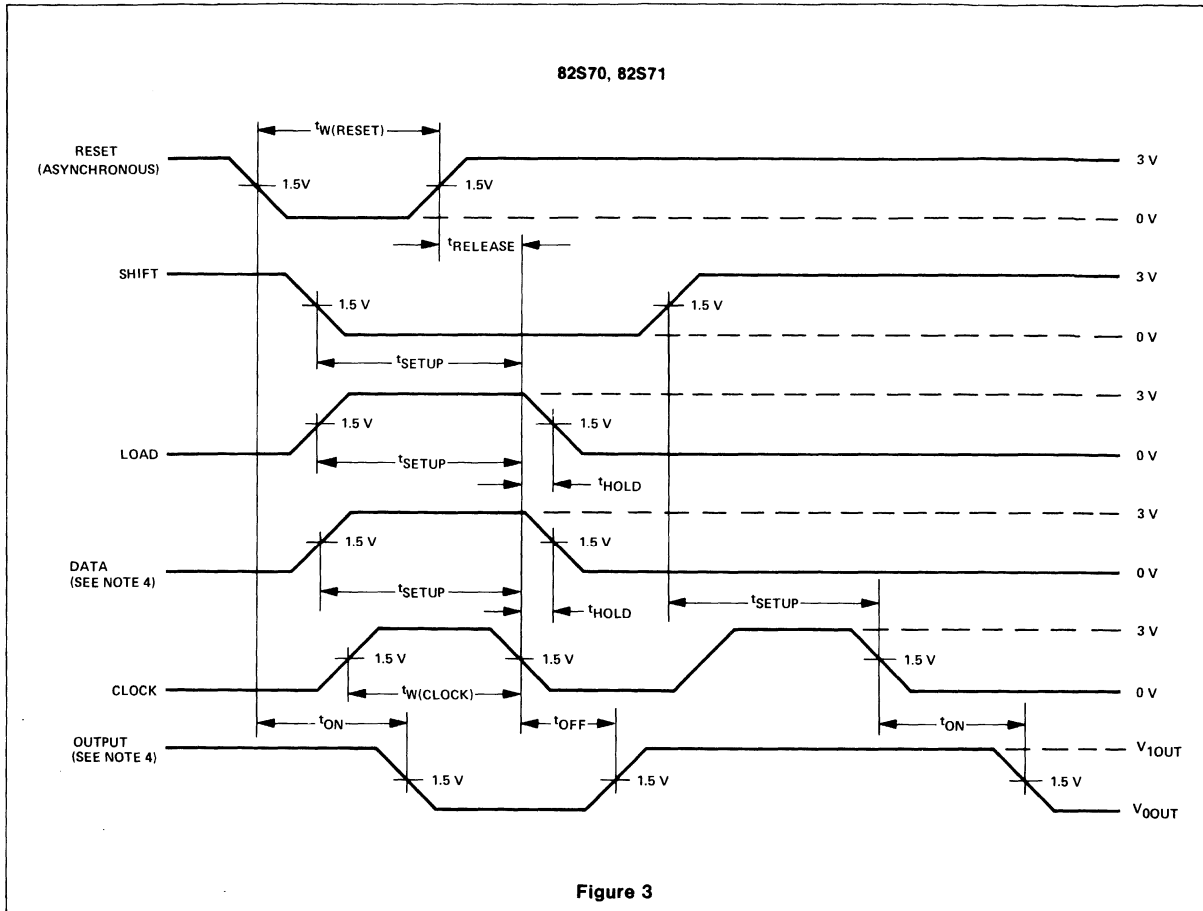
AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8270/71		82S70/S71		UNIT
		Min	Max	Min	Max	
t_w Clock pulse width	Figure 1	20		8.0		ns
t_w Reset pulse width	Figure 2	30		9.0		ns
t_s Set-up time Data to clock	Figure 3	30		3.0		ns
t_h Hold time Data to clock	Figure 3	0		2.0		ns
t_s Set-up time Load or Shift to clock	Figure 3	15		6.0		ns
t_h Hold time Load or Shift to clock	Figure 3	0		0		ns
t_{rec} Recovery time MR to clock	Figure 3	30		10		ns

AC WAVEFORMS



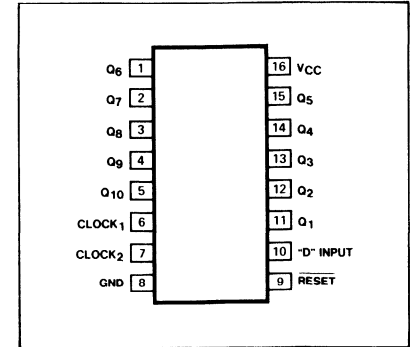
AC TEST FIGURE AND WAVEFORMS



DESCRIPTION

The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and Clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +75°C	MILITARY RANGES V _{CC} =5V ± 5%; T _A =-55°C to +125°C
Plastic DIP	N8273N	
Ceramic DIP	N8273F	S8273F
Flatpak		S8273W

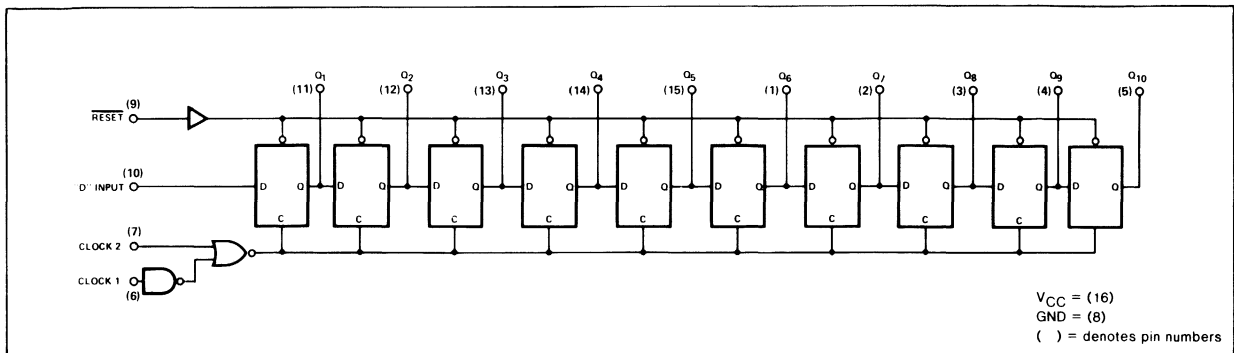
MODE SELECT—FUNCTION TABLE

INPUT	RESET	CLOCK 1	CLOCK 2	OUTPUTS Q _n
H	H	↓	L	H
L	H	↓	L	L
H	H	H	↑	H
L	H	H	↑	L
H	H	↓	H	Q _{n-1}
L	H	↓	H	Q _{n-1}
H	H	L	↑	Q _{n-1}
L	H	L	↑	Q _{n-1}
X	L	X	X	L

NOTE

The unused clock input performs the INHIBIT function.
RESET = 0 Q = 0

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	8273		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -500 μ A	2.6		V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 9.6mA		0.4	V
I _{IH} Input HIGH current	V _{CC} = 5.25V, V _{IN} = 4.5V		40	μ A
I _{IL} Input LOW current	V _{CC} = 5.25V, V _{IN} = 0.4V		-1.6	mA
V _{BD} Input breakdown voltage	V _{CC} = 5.25V, I _N = 10mA	5.5		V
I _{OS} Output short circuit current	V _{CC} = 5.25V, V _{OUT} = 0V	-20	-70	mA
I _{CC} Supply current	V _{CC} = 5.25V		103	mA

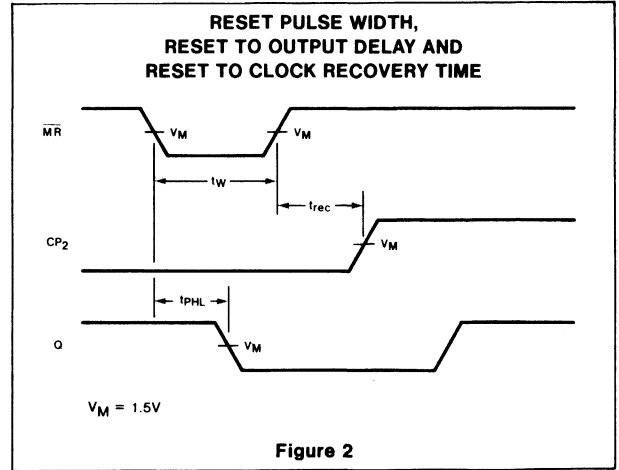
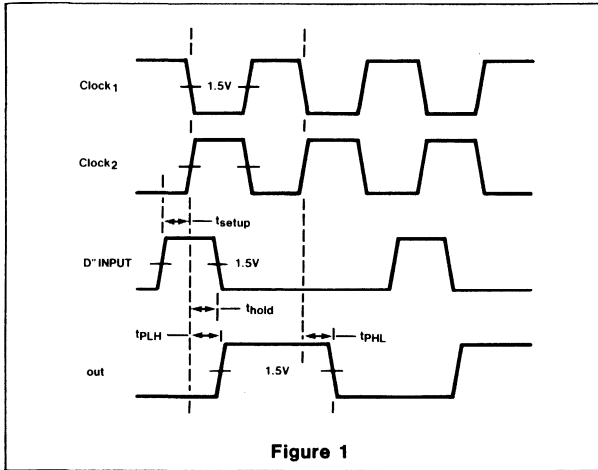
AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8273		UNIT
		C _L = 18pF R ₁ = $\infty\Omega$ R ₂ = 150 Ω		
		Min	Max	
f _{MAX} Maximum Clock Frequency	Figure 1	25		MHz
t _{PLH} Propagation delay t _{PHL} CP ₁ to output	CP ₂ = 0V, Figure 1		40 40	ns ns
t _{PLH} Propagation delay t _{PHL} CP ₂ to output	CP ₁ = 4.5V, Figure 1		40 40	ns ns
t _{PHL} Propagation delay Reset to output	Figure 2		50	ns

AC SET-UP REQUIREMENTS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8273		UNIT
		Min	Max	
t _W CP ₁ pulse width	Figure 1	25		ns
t _s Setup time Data to CP ₁	Figure 1	15		ns
t _h Hold time Data to CP ₁	Figure 1	15		ns
t _W CP ₂ pulse width	Figure 1	20		ns
t _s Setup time Data to CP ₂	Figure 1	10		ns
t _h Hold time Data to CP ₂	Figure 1	10		ns

AC WAVEFORMS

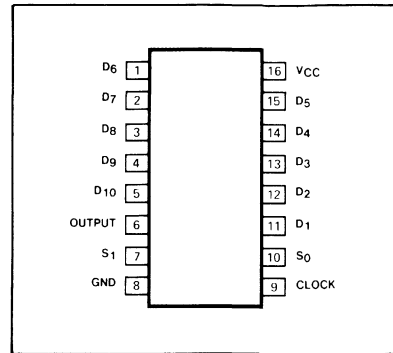


DESCRIPTION

The 8274 10-Bit Shift Register is an array of binary elements interconnected to perform the parallel-in serial-out shift function. The circuit has ten parallel inputs and a single true serial output. The D₁ input can also be used for serial entry. Two control inputs, S₀ and S₁, determine the operating mode of the shift register as shown in the Truth Table. A single buffered clock line connects all ten flip-flops which are activated on the high-to-low transition of the clock pulse.

Guaranteed input clock frequency is 25MHz. With the exception of the Hold Mode, the control inputs may be changed when the clock is in either the high or low state without causing false triggering. The Hold Mode can be entered only when the clock is low. Applications for the 8274 Shift Register include Parallel-to-Serial conversion, Modem Data Transmission, Pseudo-Random Code generation and Modulo-N Frequency Division.

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

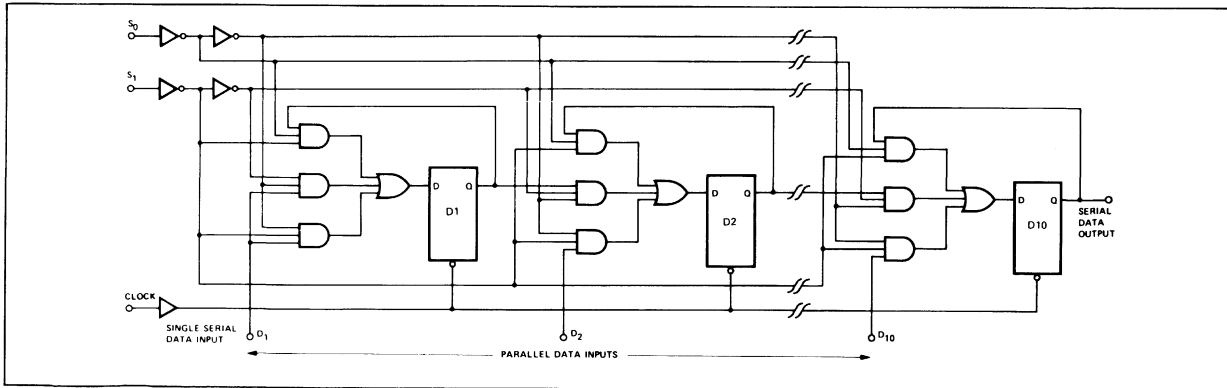
PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +75°C	MILITARY RANGES V _{CC} =5V ± 5%; T _A =-55°C to +125°C
Plastic DIP	N8274N	
Ceramic DIP	N89274F	S8274F
Flatpak		S8274W

**MODE SELECT—
FUNCTION TABLE**

S ₀	S ₁	OPERATING MODE
L	L	Hold
L	H	Clear
H	L	Load
H	H	Shift

H = HIGH voltage level
L = LOW voltage level

LOGIC DIAGRAM



NOTE

a. The slashed numbers indicate different parametric values for Military Commercial temperature ranges respectively.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	8274		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -800μA	2.6		V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 16mA		0.4	V
I _{IH} Input HIGH current	V _{CC} = 5.25V, V _{IN} = 4.5V		40	μA
I _{IL} Input LOW current D _n , S ₀ , S ₁ Clock	V _{CC} = 5.25V, V _{IN} = 0.4V	-0.2	-1.2	mA
		-0.2	-1.6	mA
V _{BD} Input breakdown voltage	V _{CC} = 5.0V, I _{IN} = 10mA	5.5		V
I _{OS} Output short circuit current	V _{CC} = 5.0V, V _{OUT} = 0V	-20	-70	mA
I _{CC} Supply current	V _{CC} = 5.0V		108	mA

AC CHARACTERISTICS: T_A = 25° C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8274		UNITS
		C _L = 18pF R ₁ = ∞Ω R ₂ = 84.5Ω		
		Min	Max	
f _{Max} Maximum clock frequency	Figure 1	25		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Figure 1		40	ns
			40	ns

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8274		UNIT
		Min	Max	
t_w Clock pulse width	Figure 1	20		ns
t_s Set-up time D _n S ₀ , S ₁	Figure 1	10		ns
		25		ns

AC WAVEFORMS

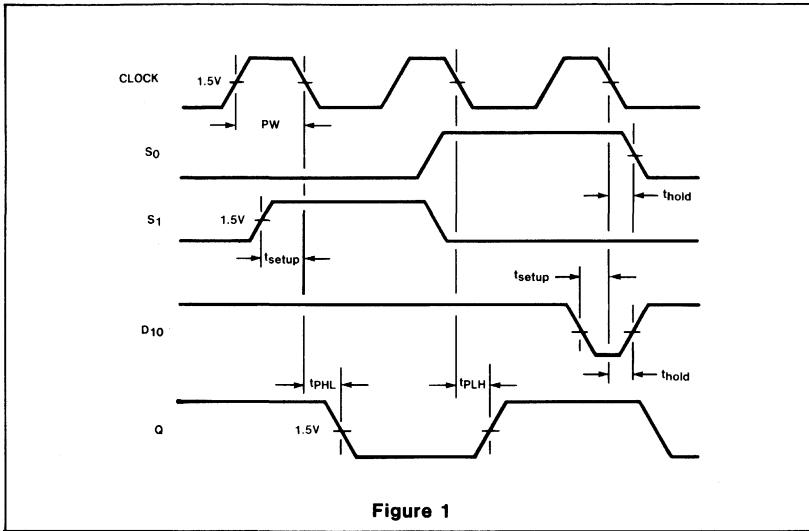


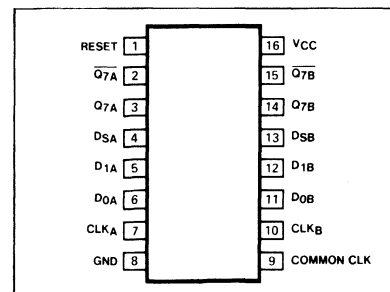
Figure 1

DESCRIPTION

The 8277 is a dual 8-Bit Shift Register which provides the designer with sixteen (16) bits of serial storage operating at a typical shift rate of 20MHz. Features of the 8277 are:

1. TRUE and COMPLEMENT outputs are provided on each register's eighth bit.
2. Positive edge triggering on clock input.
3. SEPARATE CLOCK lines (pins 7 and 10) for each 8-bit register are provided as well as a COMMON CLOCK line (pin 9) for all sixteen storage bits.
4. Common RESET (pin 1).
5. AND-OR gating to the input of each 8-bit register is provided to accomplish the multiplex function.
6. Direct replacement for 9328.

PIN CONFIGURATION



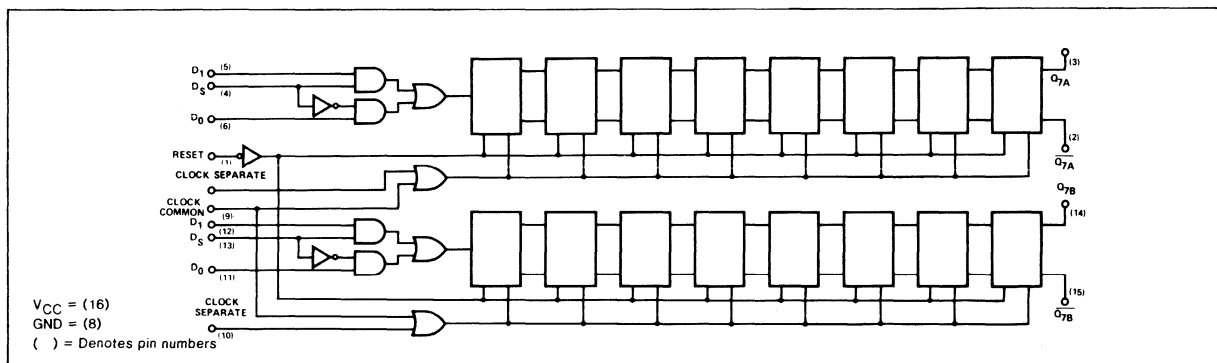
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +75°C	MILITARY RANGES V _{CC} =5V ± 5%; T _A =-55°C to +125°C
Plastic DIP	N8277N	
Ceramic DIP	N8277F	
Flatpak		

FUNCTION TABLE

D _S	D ₀	D ₁	Reset	Function
L	L	X	H	Shift in "0"
L	H	X	H	Shift in "1"
H	X	L	H	Shift in "0"
H	X	H	H	Shift in "1"
X	X	X	L	Reset "Q" to "0"

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8277		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -800μA	2.6		V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 16mA		0.4	V
I _{IH} Input HIGH Current Data, Reset, Clock separate Data select, Clock common	V _{CC} = 5.25V, V _{IN} = 4.5V		40 80	μA μA
I _{IL} Input LOW current Data, Reset, Clock separate Data select, Clock common	V _{CC} = 5.25V, V _{IN} = 0.4V		-1.6 -3.2	mA mA
V _{BD} Input breakdown voltage	V _{CC} = 4.75V, I _{IN} = 10mA	5.5		V
I _{CC} Supply current	V _{CC} = 5.25V		103	mA

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

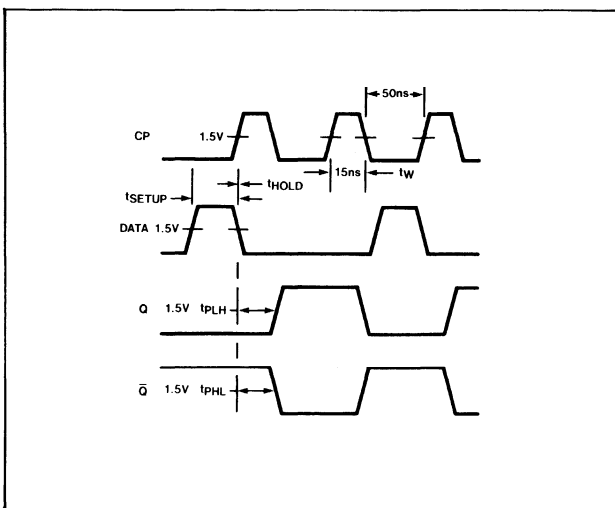
PARAMETER	TEST CONDITIONS	8277		UNIT
		$C_L = 18\text{pF}$ $R_1 = \infty\Omega$ $R_2 = 84.5\Omega$		
		Min	Max	
t_{PHL} Propagation delay t_{PLH} Clock to output	Figure 1		40	ns
t_{PHL} Propagation delay t_{PLH} Reset to output	Figure 1		40	ns

NOTE
 b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	8277		UNIT
		Min	Max	
f_{Max} Maximum clock frequency		15		MHz
t_W Clock pulse width	Figure 1	15		ns
t_s Set-up time	Figure 1	30		ns
t_h Hold time	Figure 1	5		ns

AC WAVEFORM



DESCRIPTION

The 8280 Decade Counter and 8281 16-State Binary Counter are four-bit subsystems providing a wide variety of counter/storage register applications with a minimum number of packages.

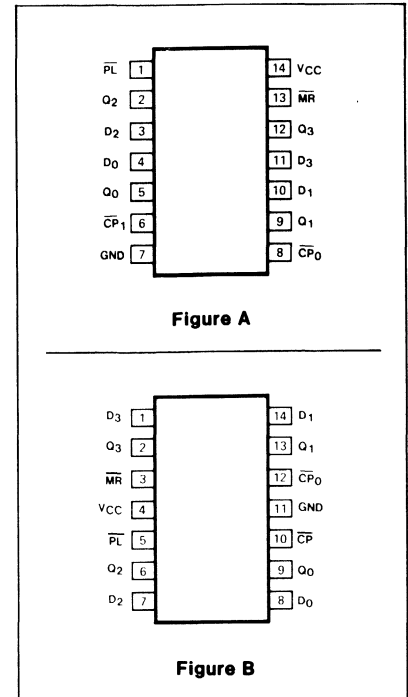
The 8280 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8281 Binary Counter may be connected as a divide-by-two, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A HIGH or LOW at data input will be transferred to the associated output when the strobe input is LOW. For additional flexibility, both units are provided with a reset input which is common to all four bits. A LOW on the Reset line forces all four outputs LOW.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

PIN CONFIGURATION



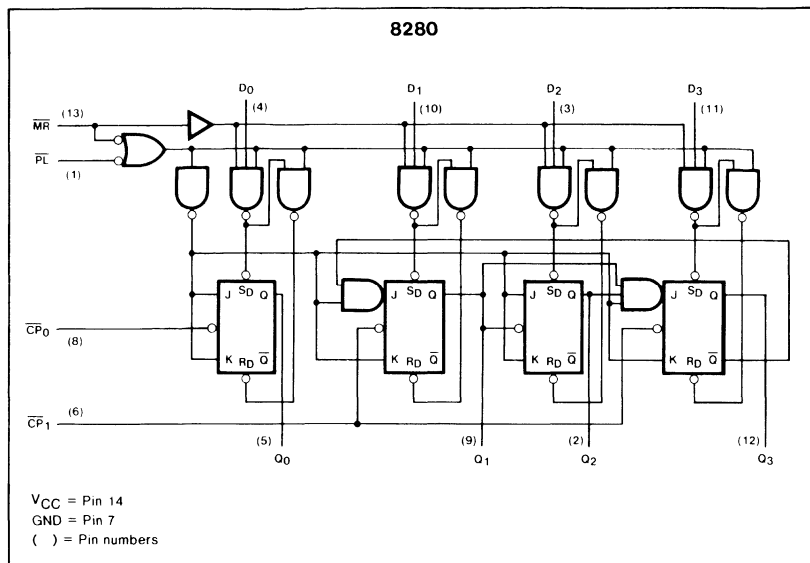
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$		$V_{CC}=5V \pm 5\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N8280N	•	N8281N	
Ceramic DIP	Fig. A	N8280F	•	N8281F	S8280F • S8281F
Flatpak	Fig. B				S8280W • S8281W

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8280		8281		UNIT
		Min	Max	Min	Max	
V_{OH} Output HIGH voltage	$V_{CC} = 4.75V, I_{OH} = -800\mu A$	2.6		2.6		V
V_{OL} Output LOW voltage	$V_{CC} = 4.75, I_{OL} = 16mA$		0.4		0.4	V
I_{IH} Input HIGH current Strobe, Data inputs Reset, Clock 1 Clock 2	$V_C = 5.25V, V_{IN} = 4.5V$		40 80 80		40 80 40	μA μA μA
I_{IL} Input LOW current Strobe input Data input Reset, Clock 1 Clock 2	$V_{CC} = 5.25V, V_{IN} = 0.4V$	-0.1 -0.1 -0.1 -0.1	-1.6 -1.2 -3.2 -3.2	-0.1 -0.1 -0.1 -0.1	-1.6 -1.2 -3.2 -1.6	mA mA mA mA
V_{BD} Input breakdown voltage	$V_{CC} = 4.75V, I_{IN} = 10mA$	5.5		5.5		V
I_{OS} Output short circuit current	$V_{CC} = 5.25V, V_{OUT} = 0V$	-10	-60	-10	-60	mA
I_{CC} Supply current	$V_{CC} = 5.25V$		45		45	mA

LOGIC DIAGRAM



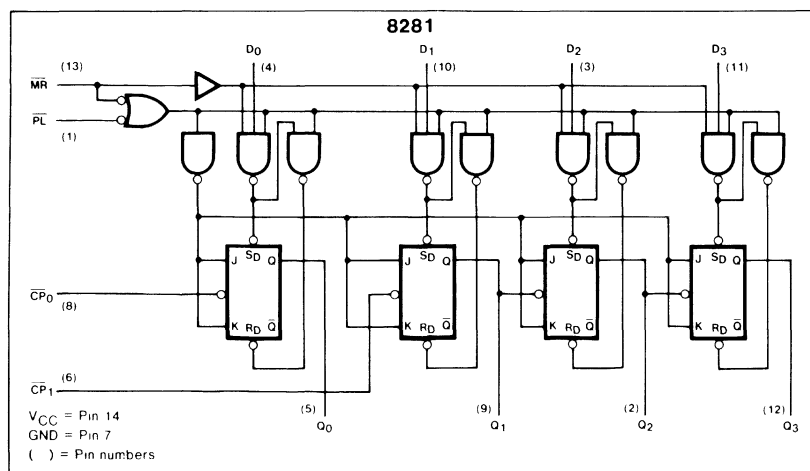
COUNT SEQUENCES for 8280

BCD DECADE (b)					BI-QUINARY (c)				
COUNT	Q ₃	Q ₂	Q ₁	Q ₀	COUNT	Q ₀	Q ₃	Q ₂	Q ₁
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES

- b. Input applied to CP₀; Q₀ connected to CP₁.
- c. Input applied to CP₁; Q₃ connected to CP₀.

LOGIC DIAGRAM



COUNT SEQUENCES for 8281

COUNT	4-BIT BINARY(b)			
	Q ₃	Q ₂	Q ₁	Q ₀
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE

- b. Q₀ connected to CP₁; input applied to CP₀

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	MR	PL	CP	D _n	Q _n
Reset (Clear)	L	X	X	X	L
Parallel Load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↓ = HIGH-to-LOW Clock Transition

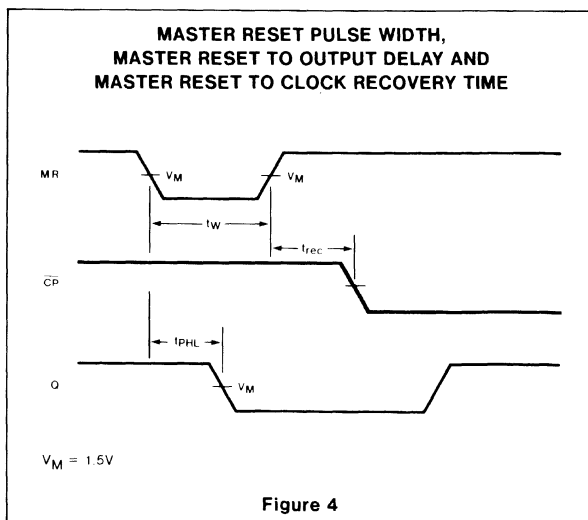
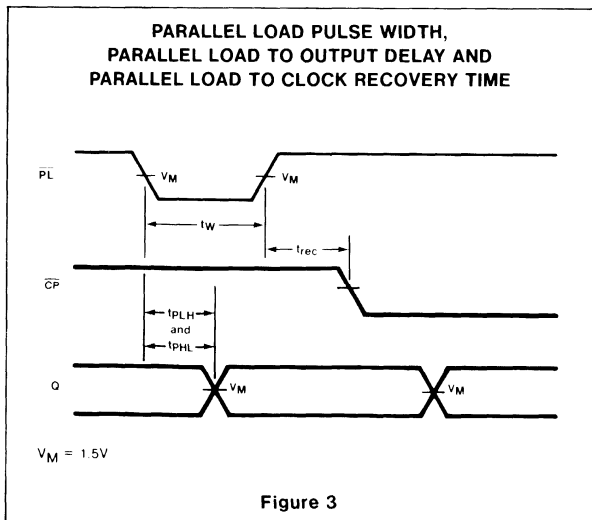
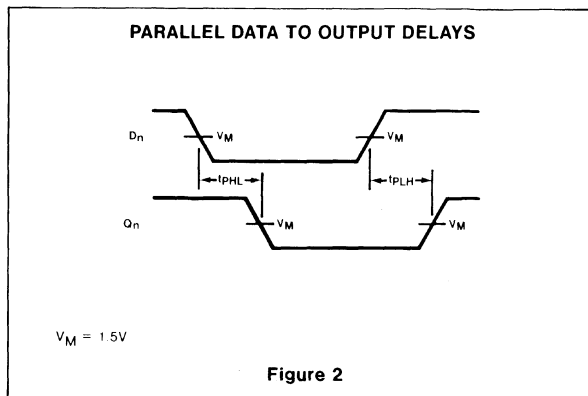
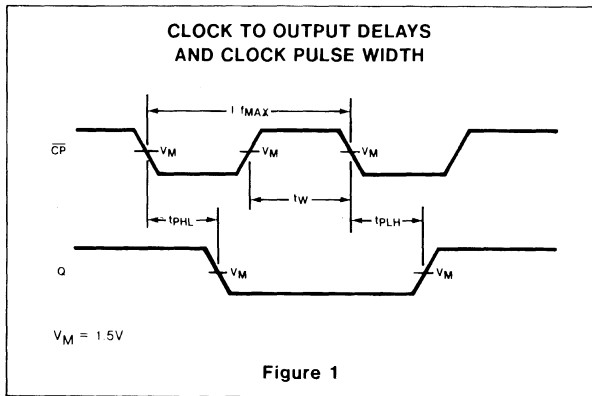
AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	8280		8281		UNIT
		C _L = 24pF R ₁ = ∞Ω R ₂ = 84.5Ω		C _L = 24pF R ₁ = ∞Ω R ₂ = 84.5Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum count frequency	Figure 1	CP ₀	20		20	MHz
		CP ₁	10		10	MHz
t _{PLH} t _{PHL} Propagation delay CP ₀ to Q ₀	Figure 1		25 25		25 25	ns ns
t _{PLH} t _{PHL} Propagation delay CP ₁ to Q ₁	Figure 1		25 25		25 25	ns ns
t _{PLH} t _{PHL} Propagation delay CP ₁ to Q ₂	Figure 1		50 50		50 50	ns ns
t _{PLH} t _{PHL} Propagation delay CP ₁ to Q ₃	Figure 1		25 25		75 75	ns ns
t _{PLH} t _{PHL} Propagation delay Data to output	Figure 2		40 35		40 35	ns ns
t _{PLH} t _{PHL} Propagation delay PL to output	Figure 3		40 35		40 35	ns ns
t _{PHL} Propagation delay MR to output	Figure 4		45		45	ns

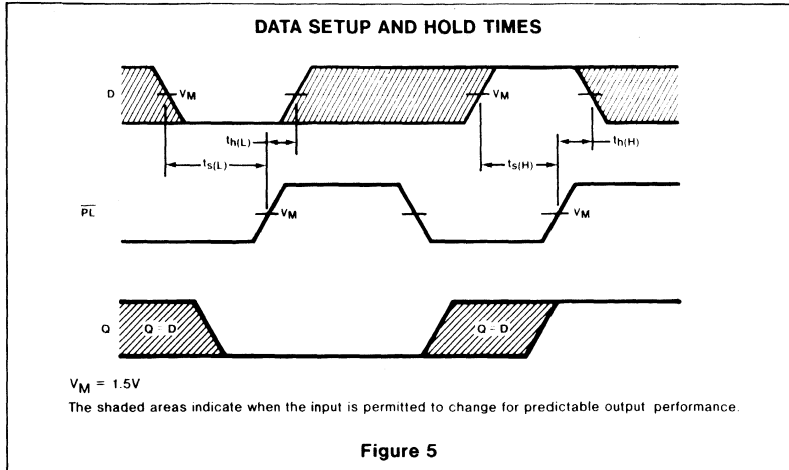
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	8280		8281		UNIT	
		Min	Max	Min	Max		
t_W Clock pulse width	Figure 1	\overline{CP}_0	25		25		ns
		\overline{CP}_1	25		25		ns
t_W \overline{MR} pulse width	Figure 4	35		35		ns	
t_W \overline{PL} pulse width	Figure 3	35		35		ns	
t_{rec} Recovery time \overline{MR} to \overline{CP}	Figure 4	75		75		ns	
t_{rec} Recovery time \overline{PL} to \overline{CP}	Figure 3	40		40		ns	

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



DESCRIPTION

The 82S82 binary coded (BCD) arithmetic unit is a high speed Schottky MSI circuit with lookahead carry/borrow that has been designed for easy systems usage. Depending on the state of the add/subtract control line, the unit produces the BCD sum or difference of two decimal numbers presented to the BCD inputs in the 8-4-2-1 weighted BCD format. A comparison output ($A=B$) is provided as well. When in the subtract mode, this output indicates if two BCD numbers are equal and its open collector feature allows easy comparison of several decades.

The 82S82 BCD arithmetic unit has been designed such that input and output logic levels including the carry/borrow are in their true logic form. Compared to multichip hardware solutions previously at the designer's disposal, the 82S82 arithmetic unit generates the BCD carry/borrow terms internally in the look-ahead mode and does BCD arithmetic directly. For more than one BCD decade the carry/borrow term may ripple between 82S82's. For ultra fast BCD arithmetic operations the Signetics 74182 fast-carry extender may be used together with the 82S82's. The 74182 suitably combines the 82S82's active LOW carry generate (\overline{CgOUT}) and carry propagate (\overline{CpOUT}) terms for complete look-ahead carry between decades.

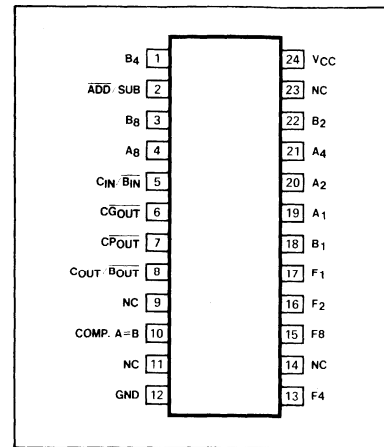
When the $\overline{ADD}/SUBTRACT$ control input is LOW, BCD addition is performed ($A + B +$

$CIN = F$). Input codes above 9 to either the A_N or B_N inputs are not defined to give valid output sums except for the special case of binary to BCD conversion. In the normal BCD addition mode the F outputs show true BCD results and an active HIGH carryout signal results for sums greater than 9.

For subtraction the $\overline{ADD}/SUBTRACT$ control input be HIGH. Internally subtraction is performed by 9's complement addition yielding the difference ($A - B - 1 = F$) of two BCD numbers when the CIN/\overline{BIN} input is LOW. If the CIN/\overline{BIN} is HIGH during subtraction, the absence of a borrow in signal gives $A - F = F$. For $A \geq B$ the BCD difference is available at the F outputs in its true form. If $A < B$, the 10's complement of the correct answer appears at the F outputs with CIN/\overline{BIN} HIGH or if CIN/\overline{BIN} is LOW the 9's complement results. As long as $A < B$ an active LOW borrow is also generated.

The 82S82 BCD arithmetic unit is also useful for binary to BCD conversion. By summing $B = 0$ with binary inputs $0 \leq A \leq 15$, where A is the number being converted, a true BCD output results. A carry is generated to the next decade for $A > 9$.

The function table for the 82S82 summarizes the device operation. In those applications where only BCD addition is required, the Signetics 82S82 BCD adder should be considered.

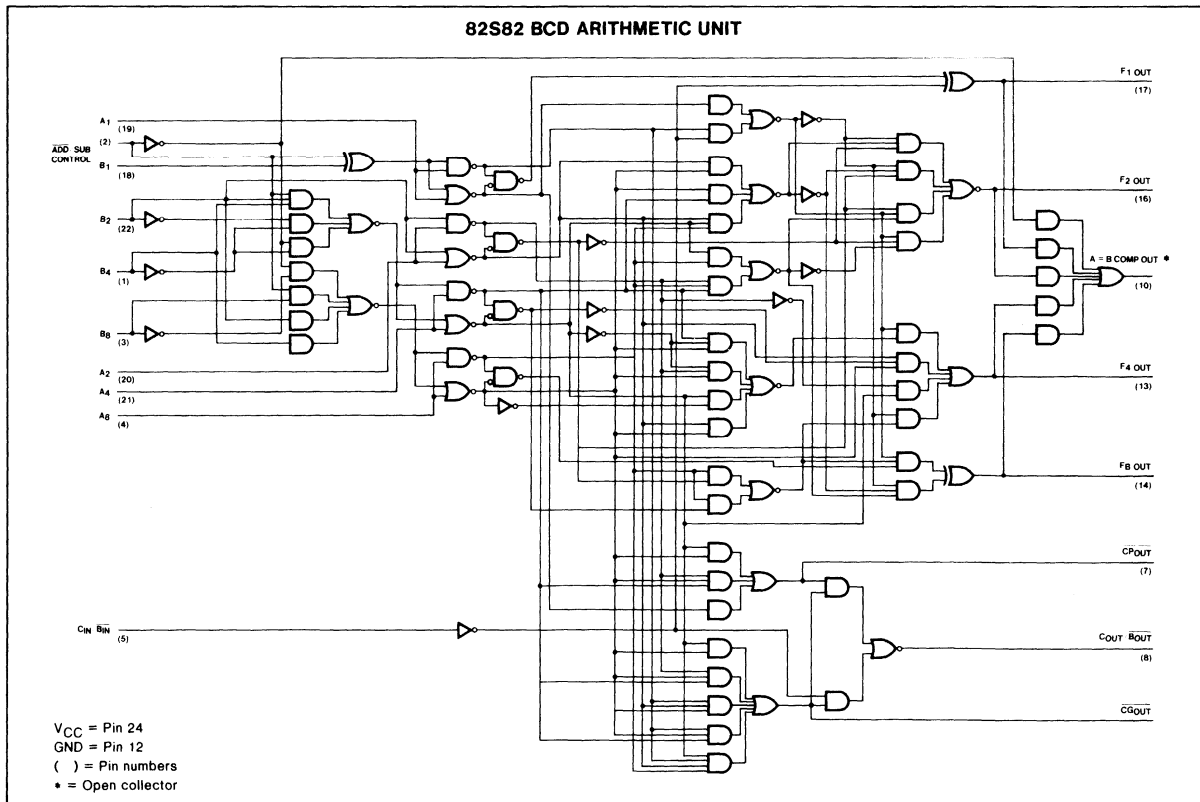
PIN CONFIGURATION**ORDERING CODE (See Section 9 for further Package and Ordering Information)**

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$	$V_{CC}=5V \pm 5\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N82S82N	
Ceramic DIP	N82S82F	
Flatpak		

FUNCTION TABLE

FUNCTION	ADD/ SUB	A(A ₈ ,A ₄ ,A ₂ ,A ₁)	B(B ₈ ,B ₄ ,B ₂ ,B ₁)	C _{in} / $\overline{B_{in}}$	F(F ₈ ,F ₄ ,F ₂ ,F ₁)	C _{out} / $\overline{B_{out}}$	COMPARE (A = B)
Add	L	BCD Augend	BCD Addend	H = Carry L = No Carry	IF C _{in} = H F = A + B + 1 IF C _{in} = L F = A + B	$F \leq 9$ C _{OUT} / $\overline{B_{OUT}}$ = L $F > 9$ C _{OUT} / $\overline{B_{OUT}}$ = H	X
Subtract	H	BCD Minuend	BCD Subtrahend	L = Borrow H = No Borrow	IF B _{in} = L F = A - B - 1 IF B _{in} = H F = A - B	$A > B$ C _{OUT} / $\overline{B_{OUT}}$ = H $A \leq B$ C _{OUT} / $\overline{B_{OUT}}$ = L $A < B$ C _{OUT} / $\overline{B_{OUT}}$ = L $A \geq B$ C _{OUT} / $\overline{B_{OUT}}$ = H	X
Compare	H	BCD Word A	BCD Word B	H	A - B	$A < B$ C _{OUT} / $\overline{B_{OUT}}$ = L $A > B$ C _{OUT} / $\overline{B_{OUT}}$ = H	If A = B Compare = H If A ≠ B Compare = L
Binary to BCD Con- version	L	0 ≤ A ≤ 15	B = 0	X	BCD	$A \leq 9$ C _{OUT} = L $A > 9$ C _{OUT} = H	X

LOGIC DIAGRAM



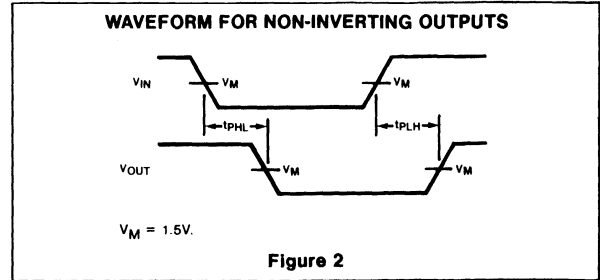
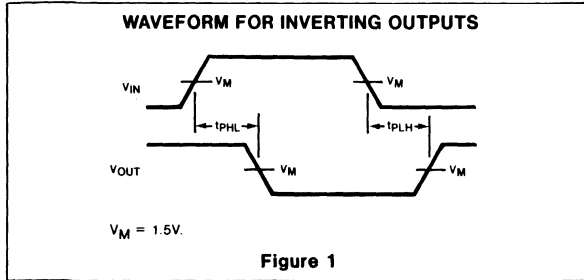
DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	82S82		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -1mA	2.6		V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 16mA		0.5	V
I _{OH} Output HIGH current	V _{CC} = 4.75V, V _{OUT} = 5.5V		250	μA
I _{IH} Input HIGH current A _N , B ₁ , B ₈ , C _{IN} / \overline{B} _{IN} B ₂ , B ₄ , Add/Sub	V _{CC} = 4.75V, V _{IN} = 4.75V		10 20	μA μA
I _{IL} Input LOW current A _N , B ₁ , B ₈ , C _{IN} / \overline{B} _{IN} B ₂ , B ₄ , Add/Sub	V _{CC} = 5.25V, V _{IN} = 0.5V		-400 -800	μA μA
V _{CD} Input clamp voltage	V _{CC} = 4.75V, I _{IN} = -18mA		-1.2	V
I _{OS} Output short circuit current	V _{CC} = 5.25V, V _{OUT} = 0V	-20	-100	mA
I _{CC} Supply current	V _{CC} = 5.25V		122	mA

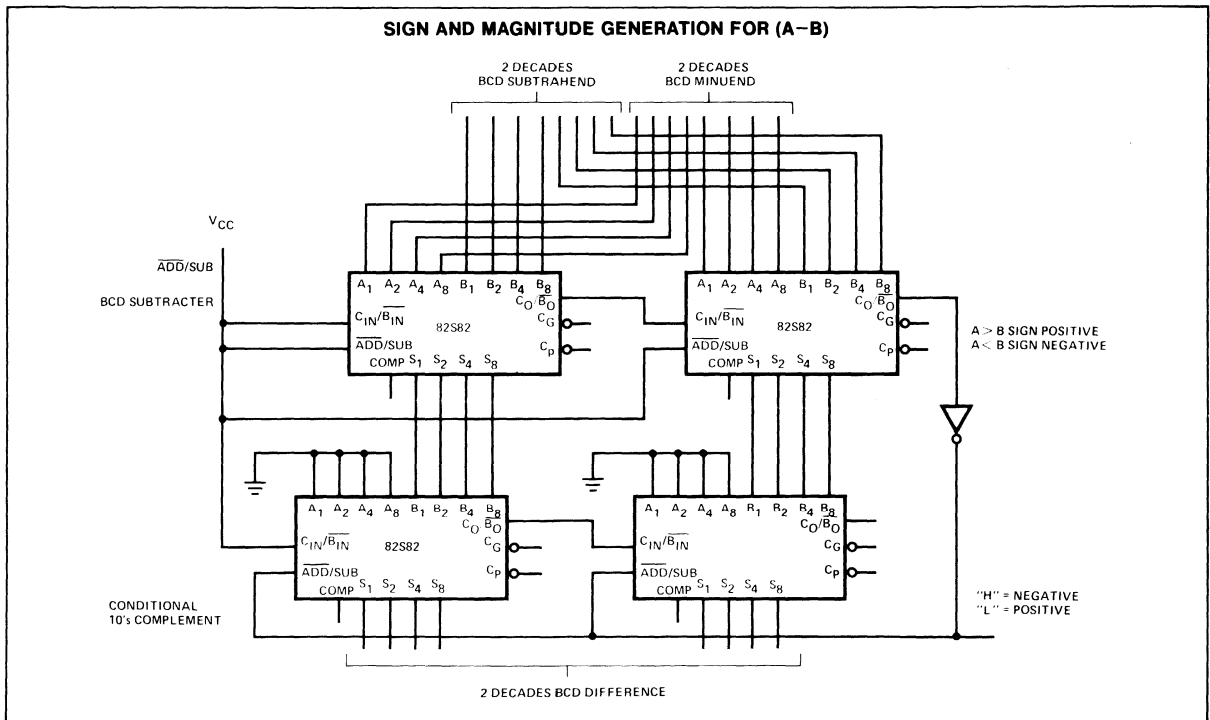
AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	82S82		UNIT
		C _L = 15pF R _L = 280Ω		
		Min	Max	
t _{PLH} Propagation delay t _{PHL} Any A _N , B _N , C _{IN} / \overline{B} _{IN} to F _N	Figures 1 & 2		35 35	ns ns
t _{PLH} Propagation delay t _{PHL} Any A _N to C _{OUT} / \overline{B} _{OUT}	Figures 1 & 2		40 35	ns ns
t _{PLH} Propagation delay t _{PHL} Any B _N to C _{OUT} / \overline{B} _{OUT}	Figures 1 & 2		45 35	ns ns
t _{PLH} Propagation delay t _{PHL} C _{IN} / \overline{B} _{IN} to C _{OUT} / \overline{B} _{OUT}	Figure 2		25 15	ns ns
t _{PLH} Propagation delay t _{PHL} Add/Sub to F _N	Figures 1 & 2		35 35	ns ns
t _{PLH} Propagation delay t _{PHL} A _N , B _N to C _P _{OUT}	Figures 1 & 2		25 25	ns ns
t _{PLH} Propagation delay t _{PHL} A _N , B _N to C _G _{OUT}	Figures 1 & 2		25 32	ns ns
t _{PLH} Propagation delay t _{PHL} A _N , B _N to (A=B) _{OUT}	Figures 1 & 2		50 50	ns ns

AC WAVEFORMS



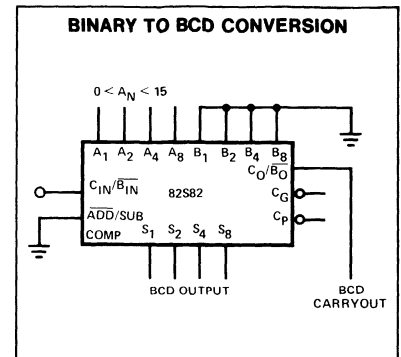
TYPICAL APPLICATIONS



TRUTH TABLE FOR BINARY TO BCD CONVERSION

(10 ≤ AN ≤ 15, BN = 0)

Add/Sub	CIN/BIN	A8	A4	A2	A1	S8	S4	S2	S1	COU/BOUT
L	L	H	L	H	L	H	L	L	L	H
L	L	H	L	H	H	H	L	L	H	H
L	L	H	H	L	L	H	L	H	L	H
L	L	H	H	L	H	H	L	H	H	H
L	L	H	H	H	L	H	H	L	L	H
L	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	L	H	L	L	H	H
L	H	H	L	H	H	H	L	H	L	H
L	H	H	H	L	L	H	L	H	H	H
L	H	H	H	L	H	H	H	L	L	H
L	H	H	H	H	L	H	H	L	H	H
L	H	H	H	H	H	H	H	H	L	H



DESCRIPTION

The 82S83 4-bit binary coded (BCD) adder is a high speed Schottky MSI circuit that has been designed for easy systems usage. This unit produces the BCD sum of two decimal numbers presented in the 8-4-2-1 weighted BCD format. Carry-in and carry-out terms are provided for easy expansion to any number of decades. The 82S83 BCD adder has been designed such that input and output logic levels including the carry are in their true logic form.

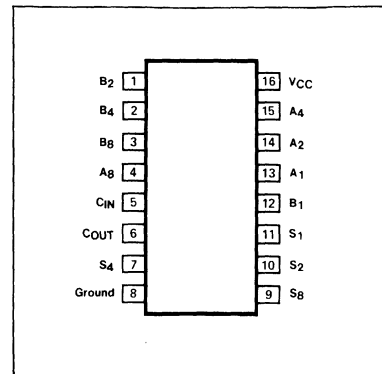
Compared to cumbersome hardware implementations previously at the designer's disposal that consist of binary addition followed by decimal correction, the 82S83 BCD adder generates the BCD carry terms internally in the look-ahead mode and does BCD addition directly. For valid BCD numbers (0 through 9) at the A and B inputs the BCD sum is formed at the output. If addition (A+B+CIN) would yield a number greater

than 9, a valid BCD number and a carry result.

Input codes above 9 are not defined except for binary to BCD conversion. Binary to BCD conversion is obtained by applying any 4-bit binary number of the AN or BN inputs while the remaining inputs are grounded. For input codes 0 through 9 a BCD number result at the output is usual. If binary inputs 10 through 15 are applied a carry term is generated and the carry output together with the sum out are the BCD equivalent of the binary input. Conversion of binary numbers greater than 16 can be achieved by cascading 82S83's.

Subtraction can be done with the 82S83 by using 9's complement addition. Rather than implementing a 9's complement circuit with gates or ROM's, the 82S82 BCD arithmetic unit should be used. The 82S82 incorporates the 9's complement feature and performs BCD addition, BCD subtraction, and number comparison.

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V _{CC} =5V ± 5%; T _A =0°C to +75°C	MILITARY RANGES V _{CC} =5V ± 5%; T _A =-55°C to +125°C
Plastic DIP	N82S83N	
Ceramic DIP	N82S83F	
Flatpak		

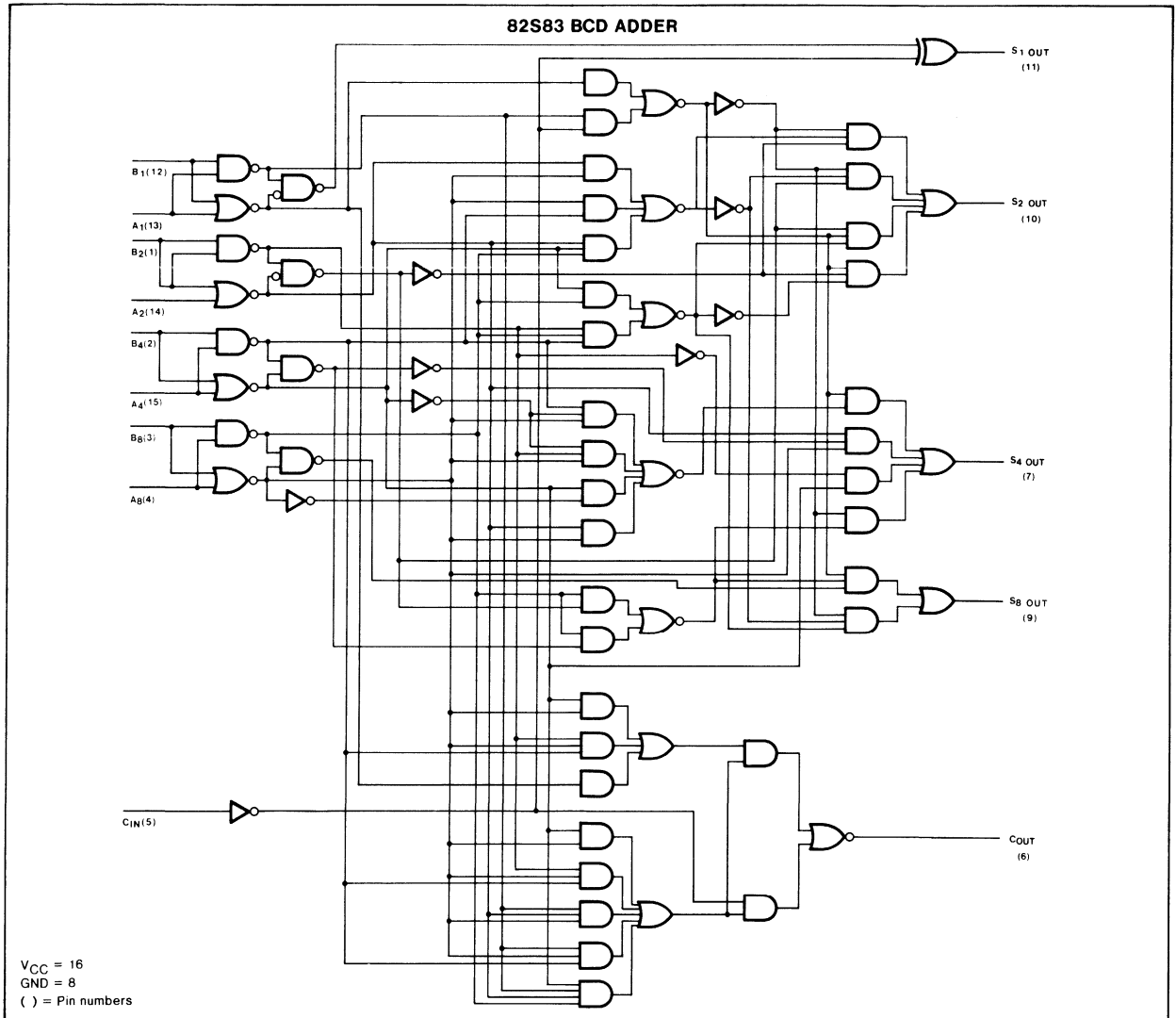
PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION
4, 15, 14, 13	A ₈ , A ₄ , A ₂ , A ₁	BCD inputs word A weighted (8-4-2-1)
3, 2, 1, 12	B ₈ , B ₄ , B ₂ , B ₁	BCD inputs word B weighted (8-4-2-1)
9, 7, 10, 11	S ₈ , S ₄ , S ₂ , S ₁	BCD sum outputs weighted (8-4-2-1)
5	C _{in}	Carry input
6	C _{out}	Carry output
16	V _{CC}	Supply voltage
8	GND	Ground

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	82S83		UNIT
		Min	Max	
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -1mA	2.6		V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 16mA		0.5	V
I _{IH} Input HIGH current	V _{CC} = 5.25V, V _{OUT} = 5.25V		10	μA
I _{IL} Input LOW current	V _{CC} 5.25V, V _{IN} = 0.5V		-400	μA
V _{CD} Input clamp voltage	V _{CC} = 4.75V, I _{IN} = -18mA		-1.2	V
I _{OS} Output short circuit current	V _{CC} = 5.25V, V _{OUT} = 0V	-20	-100	mA
I _{CC} Supply current	V _{CC} = 5.25V		114	mA

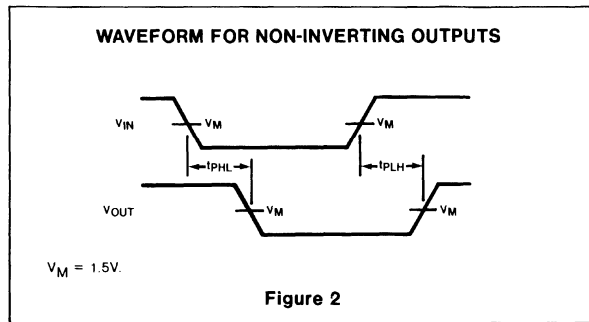
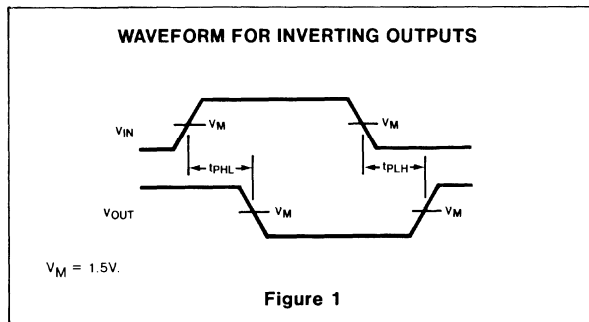
LOGIC DIAGRAM



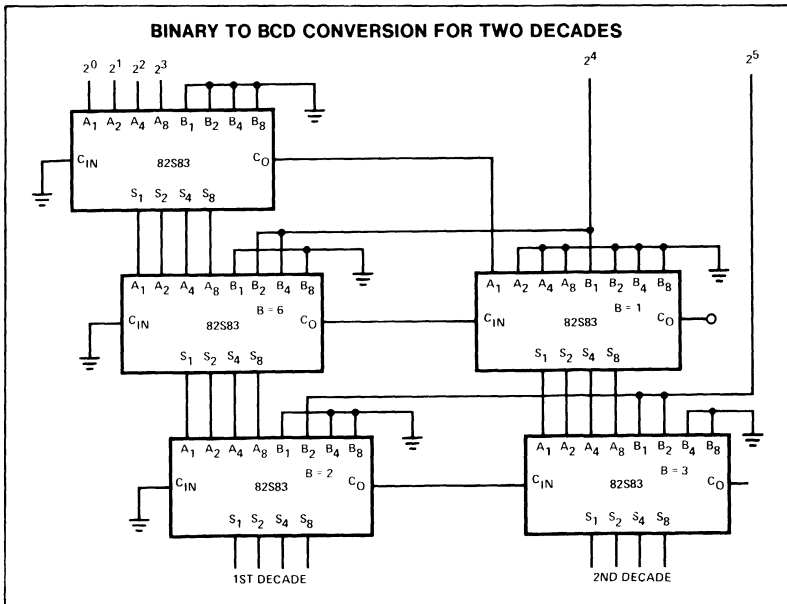
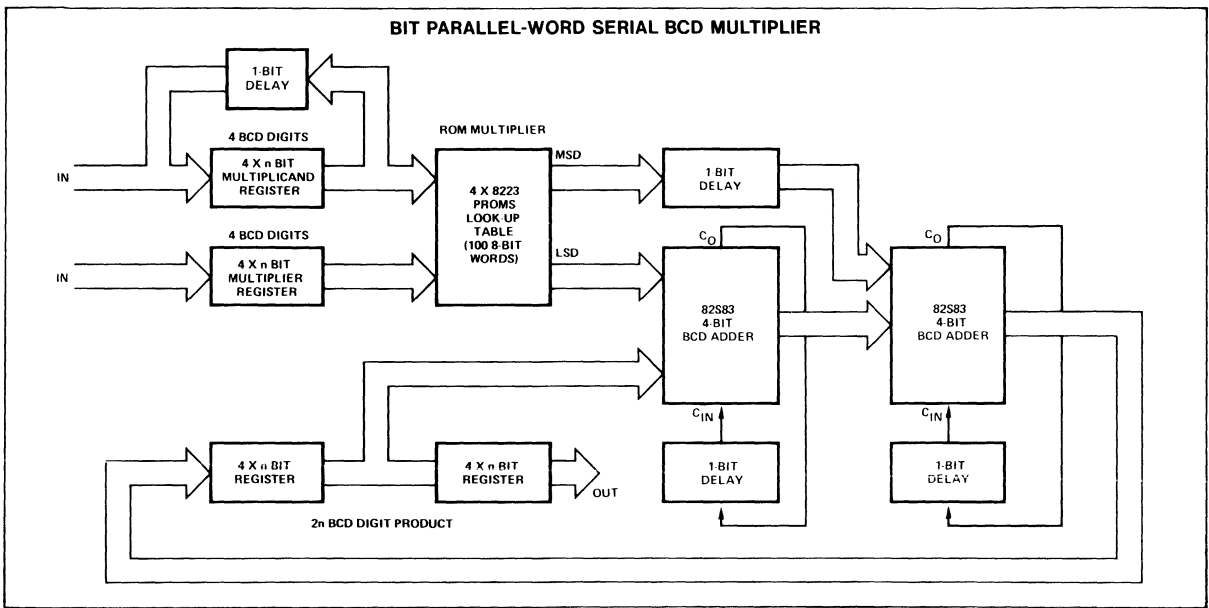
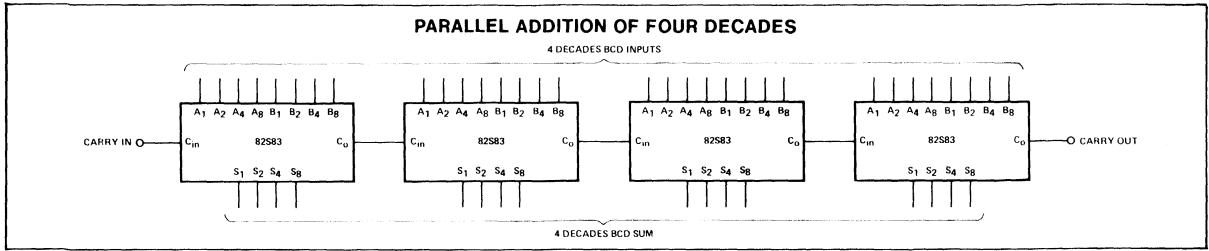
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	82S83		UNITS	
		$C_L = 15\text{pF}$ $R_L = 280\Omega$			
		Min	Max		
t_{PHL} t_{PLH}	Propagation delay Any AN, BN, C_{in} to SN	Figures 1 & 2		35 35	ns ns
t_{PHL} t_{PLH}	Propagation delay Any AN, BN to C_{out}	Figures 1 & 2		40 25	ns ns
t_{PHL} t_{PLH}	Propagation delay C_{in} to C_{out}	Figure 2		25 15	ns ns

AC WAVEFORMS



TYPICAL APPLICATIONS



DESCRIPTION

The 8290 Decade Counter and 8291 Binary Counter are high speed devices providing a wide variety of counter/storage register applications with a minimum number of packages.

The 8290 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8291 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A HIGH or LOW at a data input will be transferred to the associated output when the strobe input is LOW. For additional flexibility, both units are provided with a Reset input which is common to all four bits. A LOW on the Reset lines forces all four outputs LOW.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES		MILITARY RANGES	
		$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$		$V_{CC}=5V \pm 5\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
Plastic DIP	Fig. A	N8290N	• N8291N		
	Fig. A	N82S90N	• N82S91N		
Ceramic DIP	Fig. A	N8290F	• N8291F	S8290F	• S8291F
	Fig. A	N82S90F	• N82S91F		
Flatpak	Fig. B			S8290W	• S8291W

PIN DESIGNATIONS

SYMBOL	FUNCTION DESCRIPTION
\overline{CP}_0	Clock (active LOW going edge) input to $\div 2$ section
\overline{CP}_1	Clock (active LOW going edge) input to $\div 5$ section for 8290
\overline{CP}_1	Clock (active LOW going edge) input to $\div 8$ section for 8291
D_0 - D_3	Parallel Data inputs
\overline{PL}	Parallel Load (active LOW) input
\overline{MR}	Master Reset (active LOW) input
Q_0 - Q_3	Counter outputs

PIN CONFIGURATIONS

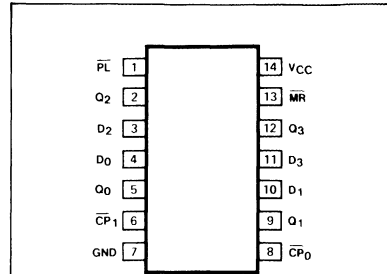


Figure A

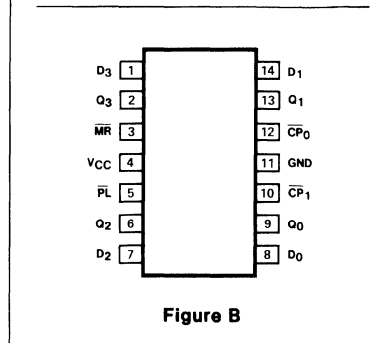


Figure B

FUNCTIONAL DESCRIPTION

1. 8290 DECADE COUNTER

The 8290 can be used in three basic modes as follows:

- a. BCD Counter. The \overline{CP}_1 input must be connected to the Q_0 output and \overline{CP}_0 receives the count input. The count sequence obtained is BCD in accordance with the truth table.
- b. Bi-Quinary Counter. If a symmetrical output is required for divide-by-10 operation, the Q_3 output must be connected to the \overline{CP}_0 input and the count input applied to \overline{CP}_1 . A symmetrical square wave is then obtained at Q_0 of one-tenth the input frequency present at \overline{CP}_1 in accordance with the truth table.
- c. Separate Divide-by-Two and Five Counters. Because the inherent structure of the counter is that of separate divide-by-two and divide-by-five sections, no other connections are required for this mode of operation. An input presented to \overline{CP}_0 will appear at Q_0 output at half the input frequency. An input presented to \overline{CP}_1 will appear at outputs Q_1, Q_2 and Q_3 as a binary divide-by-five count (i.e., from 0 = 000 to 4 = 100). Operation of the \overline{PL} and \overline{MR} inputs remain common to all four flip flops as with any other count mode.

2. 8291 BINARY COUNTER

The 8291 can be used in two basic count modes as follows:

- a. Binary Counter—For this mode of operation Q_0 output must be connected to \overline{CP}_0 . Subdivisions of the count input frequency then appear at $Q_0 = -2, Q_1 = -4, Q_2 = -8, Q_3 = -16$ as shown in the truth table.
- b. Separate Divide-by-Two and Divide-by-Eight Counters—In similar manner to the 8290 in the 8291 inherent structure allows separate use of the first and last three stages. In the first stage the input count frequency presented to \overline{CP}_1 appears as outputs $Q_1 = \div 2, Q_2 = \div 4$ and $Q_3 = \div 8$ simultaneously. Operation of the \overline{PL} and \overline{MR} inputs remains common to all stages.

3. OPERATION OF THE \overline{PL} DATA STROBE AND \overline{MR} RESET INPUTS:

- a. Data Strobe \overline{PL} input. When $\overline{PL} = \text{LOW}$ the four stages of the 8290/91 can be used a four separate latches with the outputs Q_0-Q_3 following the data presented to the inputs D_0-D_3 regardless of clock inputs. With $\overline{PL} = \text{HIGH}$ the four stages remain unchanged until the next clock inputs,

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	\overline{MR}	\overline{PL}	\overline{CP}	D_n	Q_n
Reset (Clear)	L	X	X	X	L
Parallel Load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↓ = HIGH-to-LOW Clock Transition

COUNT SEQUENCES for 8290/82S90

BCD DECADE (b)					BI-QUINARY (c)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES
 b. Input applied to \overline{CP}_0 ; Q_0 connected to \overline{CP}_1 .
 c. Input applied to \overline{CP}_1 ; Q_3 connected to \overline{CP}_0 .

which activate counting in accordance with the various modes described previously. The Reset \overline{MR} inputs when LOW overrides \overline{PL} as described below.

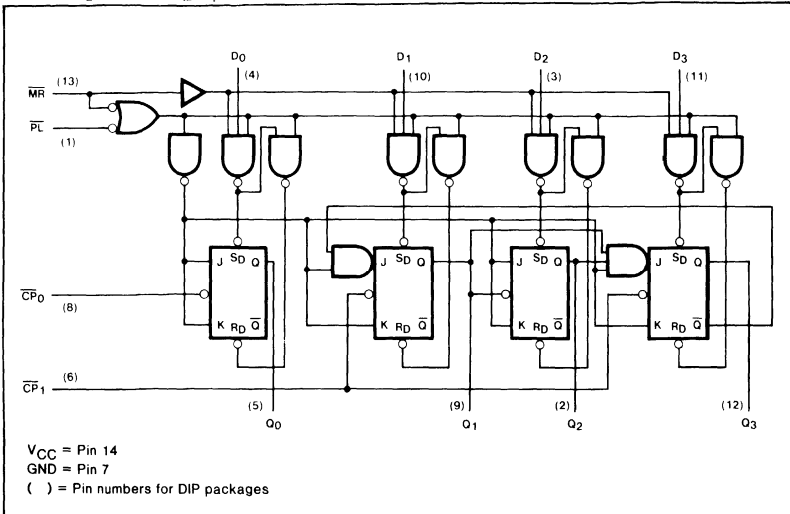
- b. Reset \overline{MR} Input. With $\overline{MR} = \text{LOW}$ the clock inputs $\overline{CP}_0, \overline{CP}_1$ and \overline{PL} input are overridden, all stages of the 82S90/91 are cleared. When $\overline{MR} = \text{HIGH}$ operation is controlled by \overline{PL} or \overline{CP}_0 and \overline{CP}_1 clock inputs as described above.

COUNT SEQUENCE for 8291/82S91

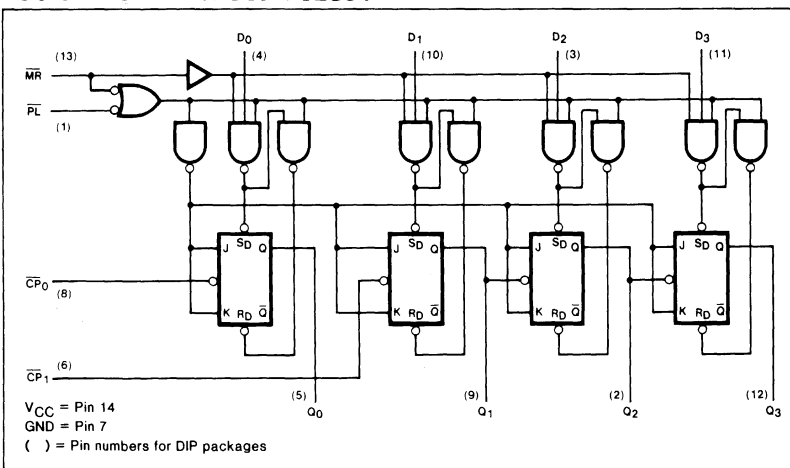
COUNT	4-BIT BINARY(b)			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE
 b. Q_0 connected to \overline{CP}_1 ; input applied to \overline{CP}_0

LOGIC DIAGRAM for 8290/82S90



LOGIC DIAGRAM for 8291/92S91



DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8290		8291		82S90		82S91		UNITS
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH voltage V _{CC} = 4.75V 8290/91 I _{OH} = -200μA 82S90/S91 I _{OH} = -1mA	2.6		2.6		2.6		2.6		V
V _{OL}	Output LOW voltage V _{CC} = 4.75V I _{OL} = 9.6mA 8290/91 I _{OL} = 20mA 82S90/91		0.4		0.4		0.5		0.5	V
I _{IH}	Input HIGH current P _L , D ₀ -D ₃ inputs M _R inputs C _{P1} inputs C _{P2} inputs V _{CC} = 5.25V, V _{IN} = 4.5V		40 80 80 120		40 80 80 80		10 10 100 10		10 10 100 50	μA μA μA μA
I _{IL}	Input LOW current P _L inputs D ₀ -D ₃ inputs M _R inputs C _{P1} input C _{P2} input V _{CC} = 5.25V, V _{IN} = 0.4V		-1.6 -1.2 -2.8 -4.8 -4.8		-1.6 -1.2 -2.8 -4.8 -2.4		-0.4 -0.4 -0.4 -6.0 -6.0		-0.4 -0.4 -0.4 -6.0 -3.0	mA mA mA mA mA
I _{OS}	Output short circuit current Q ₀ output Q ₁ -Q ₃ output V _{CC} = 5.25V, V _{OUT} = 0V	-20 -10	-70 -60	-20 -10	-70 -60	-40 -40	-100 -100	-40 -40	-100 -100	mA mA
I _{CC}	Supply current V _{CC} = 5.25V						88		88	mA
	V _{CC}		48.5		48.5					

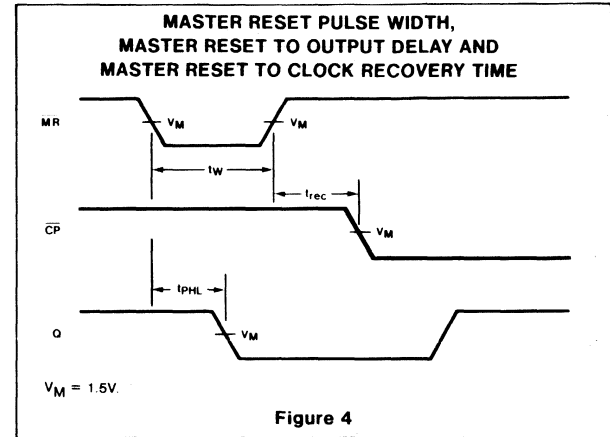
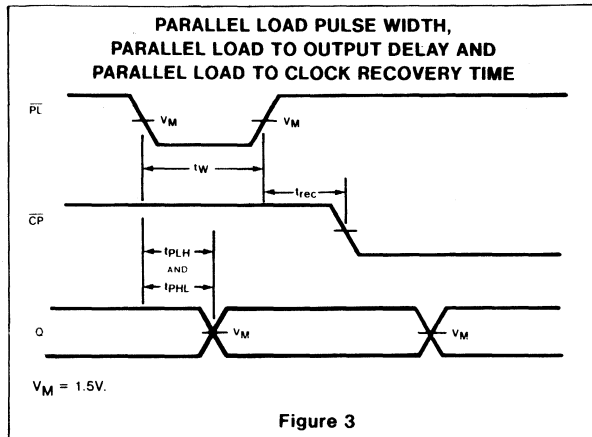
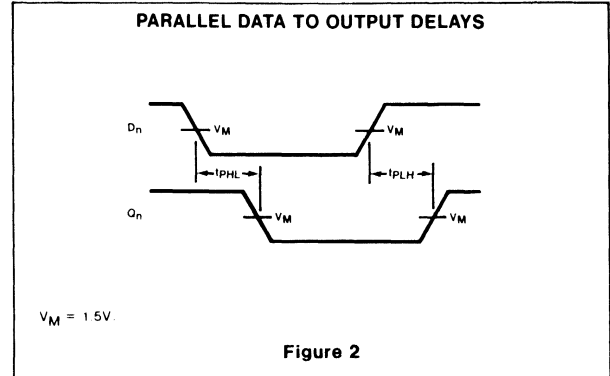
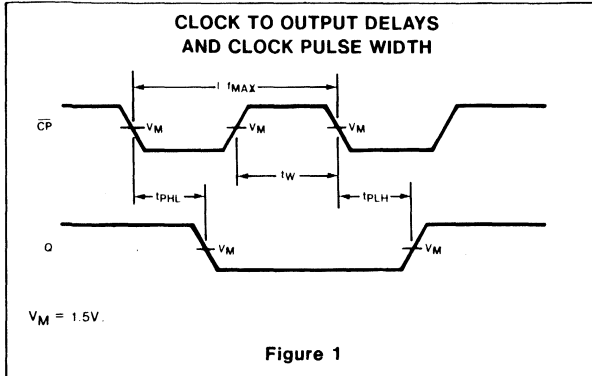
AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS		8290		8291		82S90		82S91		UNITS
				C _L = 30pF R ₁ = ∞Ω R ₂ = 146Ω		C _L = 30pF R ₁ = ∞Ω R ₂ = 146Ω		C _L = 15pF R _L = 280Ω		C _L = 15pF R _L = 280Ω		
				Min	Max	Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum count frequency	Figure 1	CP ₀	40		40		85		85		MHz
			CP ₁	20		20		42.5		42.5		MHz
t _{PLH}	Propagation delay CP ₀ to Q ₀	Figure 1		23		23		8.0		8.0		ns
t _{PHL}				25		25		12		12		ns
t _{PLH}	Propagation delay CP ₁ to Q ₁	Figure 1		25		25		10		10		ns
t _{PHL}				30		30		13		13		ns
t _{PLH}	Propagation delay CP ₁ to Q ₂	Figure 1		55		55		23		23		ns
t _{PHL}				60		60		26		26		ns
t _{PLH}	Propagation delay CP ₁ to Q ₃	Figure 1		25		85		10		36		ns
t _{PHL}				30		90		13		39		ns
t _{PLH}	Propagation delay Data to output	Figure 2		42		42		20		20		ns
t _{PHL}				42		42		22		22		ns
t _{PLH}	Propagation delay PL to output	Figure 3		42		42		20		20		ns
t _{PHL}				42		42		22		22		ns
t _{PHL}	Propagation delay	Figure 4		50		50		30		30		ns

AC SET-UP REQUIREMENTS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS		8290		8291		82S90		82S91		UNITS
				Min	Max	Min	Max	Min	Max	Min	Max	
t _w	Clock pulse width	Figure 1	CP ₀	12.5		12.5		6.0		6.0		ns
			CP ₁	12		12		25		25		ns
t _w	MR pulse width	Figure 4		40		40		15		15		ns
t _w	PL pulse width	Figure 3		25		25		10		10		ns
t _{rec}	Recovery time MR to CP	Figure 4		30		30		15		15		ns
t _{rec}	Recovery time PL to CP	Figure 3		30		30		15		15		ns

AC WAVEFORMS



DESCRIPTION

The 8292 Decade Counter and 8293 Binary Counter are low power devices providing a wide variety of counter/storage register applications with a minimum number of packages.

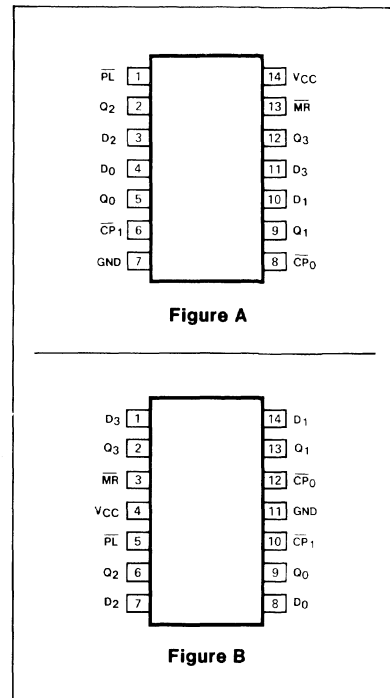
The 8292 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

The 8293 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

Both devices have strobed parallel-entry capability so that the counter may be set to any desired output state. A HIGH or LOW at a data input will be transferred to the associated output when the strobe input is LOW. For additional flexibility, both units are provided with a reset input which is common to all four bits. A LOW on the Reset line forces all four outputs LOW.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse, however there is no restriction on the transition time since the individual binaries are level-sensitive.

PIN CONFIGURATIONS



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 5\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
			•		•
Plastic DIP	Fig. A	N8292N	•	N8293N	
Ceramic DIP	Fig. A	N8292F	•	N8293F	S8292F • S8293F
Flatpak	Fig. B				S8292W • S8293W

PIN DESIGNATIONS

SYMBOL	FUNCTION DESCRIPTION
\overline{CP}_0	Clock (active LOW going edge) input to $\div 2$ section
\overline{CP}_1	Clock (active LOW going edge) input to $\div 5$ section for 8292
\overline{CP}_1	Clock (active LOW going edge) input to $\div 8$ section for 8293
D_0-D_3	Parallel Data inputs
\overline{PL}	Parallel Load (active LOW) input
\overline{MR}	Master Reset (active LOW) input
Q_0-Q_3	Counter outputs

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	\overline{MR}	\overline{PL}	\overline{CP}	D_n	Q_n
Reset (Clear)	L	X	X	X	L
Parallel Load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↓ = HIGH-to-LOW Clock Transition

COUNT SEQUENCES for 8292

BCD DECADE (b)					BI-QUINARY (c)				
COUNT	Q ₃	Q ₂	Q ₁	Q ₀	COUNT	Q ₀	Q ₃	Q ₂	Q ₁
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTE

- b. Input applied to CP₀; Q₀ connected to CP₁.
- c. Input applied to CP₁; Q₃ connected to CP₀.

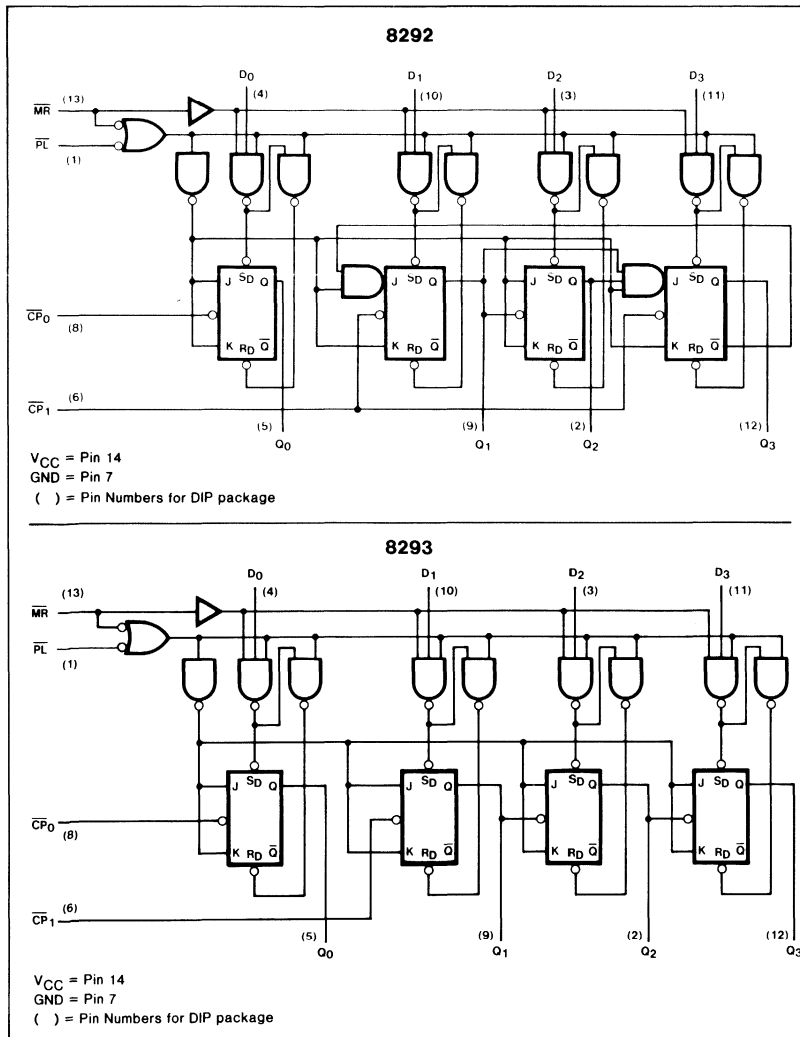
COUNT SEQUENCE for 8292

COUNT	4-BIT BINARY (b)			
	Q ₃	Q ₂	Q ₁	Q ₀
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE

- b. Q₀ connected to CP₁; input applied to CP₀

LOGIC DIAGRAMS



DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8292		8293		UNIT
		Min	Max	Min	Max	
V _{OH}	Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = -100μA		2.6		V
V _{OL}	Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 3.2mA			0.4	V
I _{IH}	Input HIGH current PL, D ₀ -D ₃ inputs MR inputs CP ₁ inputs CP ₂ inputs	V _{CC} = 5.25V, V _{IN} = 4.5V				
			20		20	μA
			40		40	μA
			40		40	μA
			80		40	μA
I _{IL}	Input LOW current PL inputs D ₀ -D ₃ inputs MR inputs CP ₁ input CP ₂ input	V _{CC} = 5.25V, V _{IN} = 0.4V				
			-0.4		-0.4	mA
			-0.4		-0.4	mA
			-0.6		-0.6	mA
			-0.6		-0.6	mA
			-1.2		-0.6	mA
I _{OS}	Output short circuit current	V _{CC} = 5.25V, V _{OUT} = 0V		-5	-45	mA
V _{BD}	Input breakdown voltage	V _{CC} = 5.25V, V _{OUT} = 0V		5.5		V
I _{CC}	Supply current	V _{CC} = 5.25V			13.1	mA

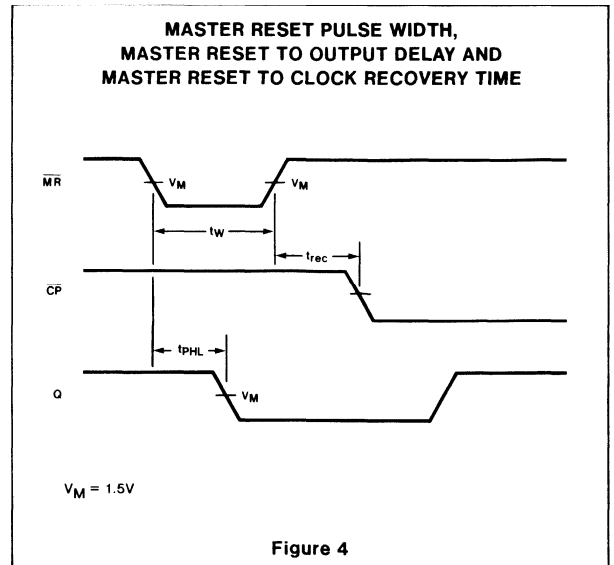
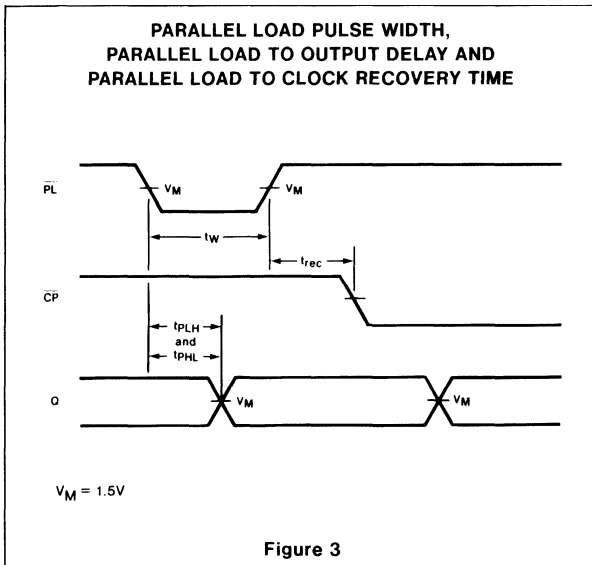
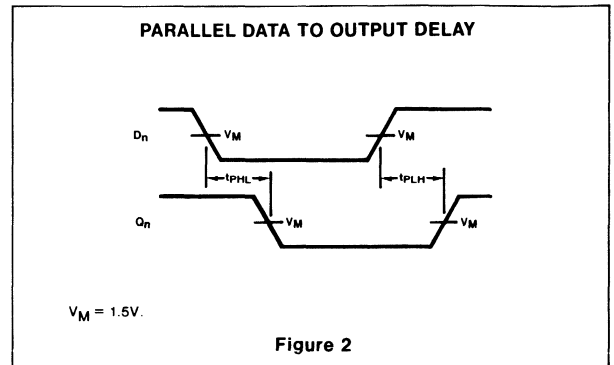
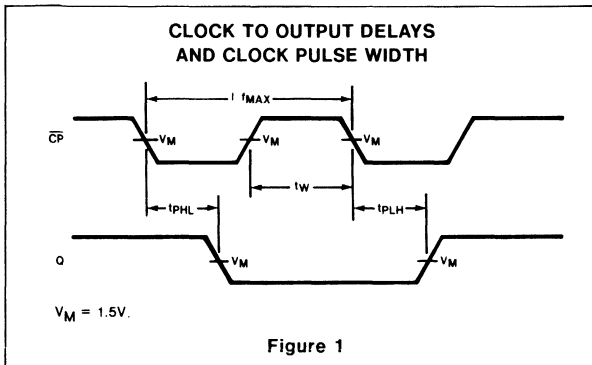
AC CHARACTERISTICS: (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8292		8293		UNIT
		C _L = 12pF R ₁ = ∞Ω R ₂ = 440Ω		C _L = 12pF R ₁ = ∞Ω R ₂ = 440Ω		
		Min	Max	Min	Max	
f _{MAX}	Maximum count frequency	Figure 1				
		CP ₀	5.0		5.0	MHz
		CP ₁	5.0		5.0	MHz
t _{PLH} t _{PHL}	Propagation delay CP ₀ to Q ₀	Figure 1				
			55		55	ns
			55		55	ns
t _{PLH} t _{PHL}	Propagation delay CP ₁ to Q ₁	Figure 1				
			55		55	ns
			55		55	ns
t _{PLH} t _{PHL}	Propagation delay CP ₁ to Q ₂	Figure 1				
			110		110	ns
			110		110	ns
t _{PLH} t _{PHL}	Propagation delay CP ₁ to Q ₃	Figure 1				
			55		165	ns
			55		165	ns
t _{PLH} t _{PHL}	Propagation delay Data to output	Figure 2				
			100		100	ns
			100		100	ns
t _{PLH} t _{PHL}	Propagation delay PL to output	Figure 3				
			100		100	ns
			100		100	ns
t _{PHL}	Propagation delay	Figure 4				
			120		120	ns

AC SET-UP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8292		8293		UNIT
		Min	Max	Min	Max	
t_W Clock pulse width	Figure 1	100		100		ns
t_W $\overline{\text{MR}}$ pulse width	Figure 4	60		60		ns
t_W $\overline{\text{PL}}$ pulse width	Figure 3	75		75		ns
t_{rec} Recovery time $\overline{\text{MR}}$ to $\overline{\text{CP}}$	Figure 4	100		100		ns
t_{rec} Recovery time $\overline{\text{PL}}$ to $\overline{\text{CP}}$	Figure 3	100		100		ns

AC WAVEFORMS



SECTION 6

9300 Series

Data Sheets

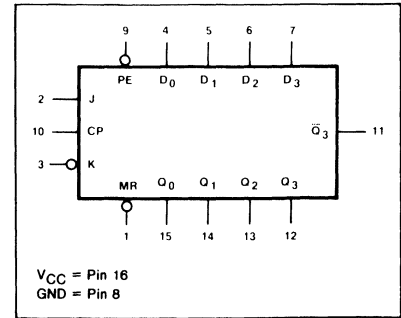
DESCRIPTION

The 9300 is a high speed 4-Bit Parallel Access Shift Register useful for a wide variety of register and counting applications. It features fully synchronous parallel and serial data transfers. The Master Reset is asynchronous, and clears the register when LOW.

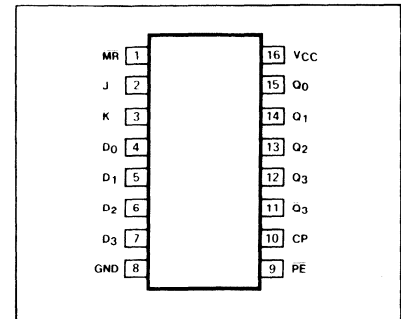
FEATURES

- Buffered clock and control inputs
- Shift right and parallel load capability
- Fully synchronous data transfers
- J-K̄ (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +75°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N9300N	
Ceramic DIP	N9300F	S9300F
Flatpak		S9300W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION	LIMITS	
CP	Clock (active HIGH going edge) input	I _{IH} (μA) I _{IL} (mA)	80 -3.2
D ₀ -D ₃	Parallel Data inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6
J	First stage J (active HIGH) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6
K̄	First stage K (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6
PĒ	Parallel Enable (active LOW) input	I _{IH} (μA) I _{IL} (mA)	92 -3.7
MR̄	Master Reset (active LOW) input	I _{IH} (μA) I _{IL} (mA)	40 -1.6
Q ₀ -Q ₃	Parallel outputs	I _{OH} (μA) I _{OL} (mA)	-480 9.6
Q ₃ ̄	Complementary lost stage output	I _{OH} (μA) I _{OL} (mA)	-640 12.8

FUNCTIONAL DESCRIPTION

The functional characteristics of the 9300 4-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 9300 operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable (\overline{PE}) input. Serial data enters the first flip-flop (Q_0) via the J and \overline{K} inputs when the \overline{PE} input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and \overline{K} inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the \overline{PE} input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 \text{--} D_3$) is transferred to the respective $Q_0 \text{--} Q_3$ outputs. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the \overline{PE} input LOW.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH

MODE SELECT—FUNCTION TABLE

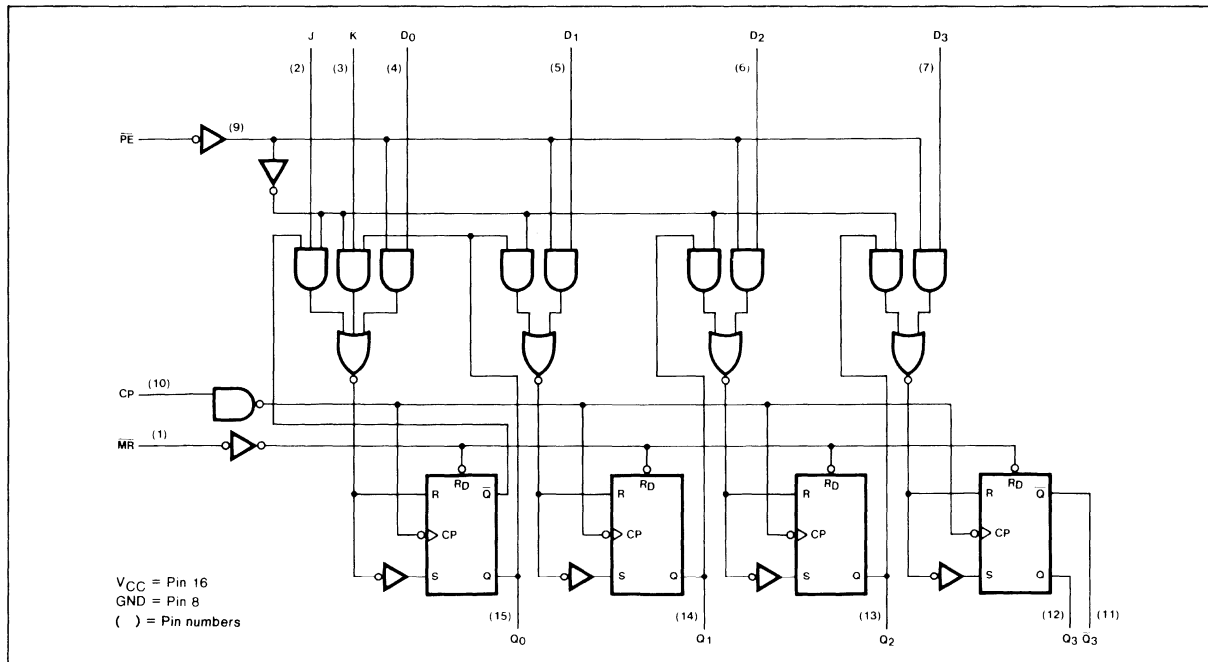
OPERATING MODES	INPUTS						OUTPUTS				
	MR	CP	\overline{PE}	J	\overline{K}	D_n	Q_0	Q_1	Q_2	Q_3	\overline{Q}_3
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	\uparrow	h	h	h	X	H	q_0	q_1	q_2	\overline{q}_2
Shift, Reset First Stage	H	\uparrow	h	l	l	X	L	q_0	q_1	q_2	\overline{q}_2
Shift, Toggle First Stage	H	\uparrow	h	h	l	X	\overline{q}_0	q_0	q_1	q_2	\overline{q}_2
Shift, Retain First Stage	H	\uparrow	h	l	h	X	q_0	q_0	q_1	q_2	\overline{q}_2
Parallel Load	H	\uparrow	l	X	X	d_n	d_0	d_1	d_2	d_3	\overline{d}_3

H = HIGH Voltage Level.
 L = LOW Voltage Level.
 X = Don't care.
 l = LOW Voltage level one setup time prior to the LOW-to-HIGH clock transition.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 \uparrow = LOW-to-HIGH clock transition.

clock transition. The 9300 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, \overline{K} , D_n , and \overline{PE} inputs for logic operation, other than the setup and release time requirements.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$	-20	-80	mA
I_{CC} Supply current	$V_{CC} = \text{Max},$	Mil	86	mA
		Com	92	mA

AC CHARACTERISTICS: $T_A = 25^\circ C$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
f_{MAX} Maximum clock frequency	Figure 1, $C_L = 15pF$	30		MHz
t_{PLH} Propagation delay	Figure 1, $C_L = 15pF$		22	ns
t_{PHL} Clock to output			26	ns
t_{PHL} Propagation delay \overline{MR} to output	Figure 2, $C_L = 15pF$		37	ns

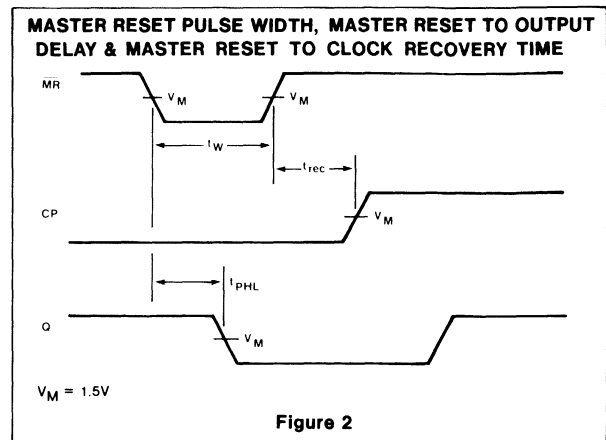
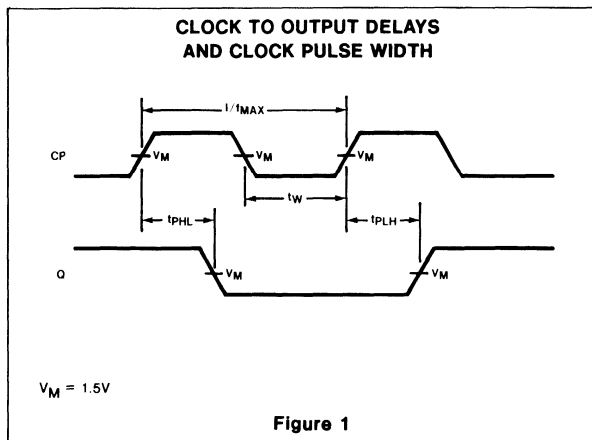
AC SETUP REQUIREMENTS: $T_A = 25^\circ C$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Figure 1, $C_L = 15pF$	17		ns
t_W Master Reset pulse width	Figure 2, $C_L = 15pF$	25		ns
t_s Setup time J, \overline{K} and Data to Clock	Figure 3, $C_L = 15pF$	20		ns
t_h Hold time J, \overline{K} and Data to Clock	Figure 3, $C_L = 15pF$	0		ns
t_s Setup time \overline{PE} to Clock	Figure 4, $C_L = 15pF$	39		ns
t_h Hold time \overline{PE} to Clock	Figure 4, $C_L = 15pF$	-5.0		ns
t_{rec} Recovery time \overline{MR} to Clock	Figure 2, $C_L = 15pF$	25		ns

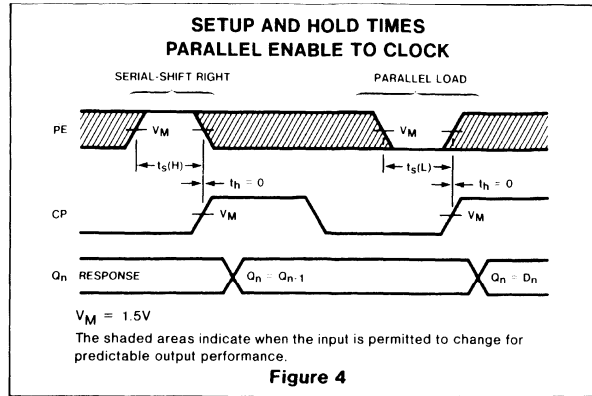
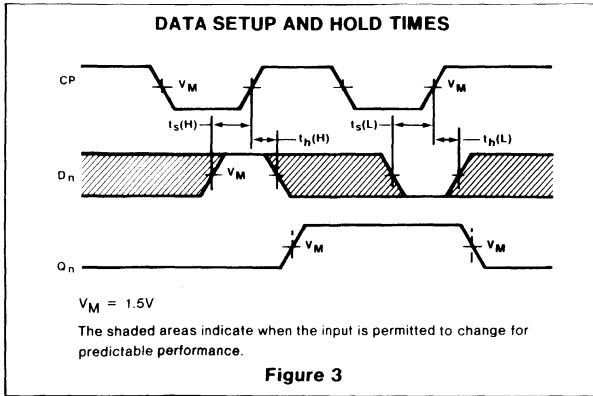
NOTE

b. For family dc characteristics use the 54 / 74 limits shown on the inside front cover.

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



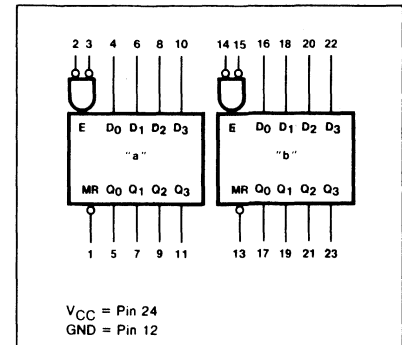
DESCRIPTION

The 9308 is a Dual 4-Bit Transparent Latch. Each 4-bit latch has a 2-input enable gate for easy expansion and an asynchronous Master Reset to clear the latch. When both Enable inputs (\bar{E}_0 & \bar{E}_1) are LOW, the data on the D inputs is loaded into the latch and appear at the outputs. A HIGH on either \bar{E}_0 or \bar{E}_1 will latch the data and hold the outputs stable.

FEATURES

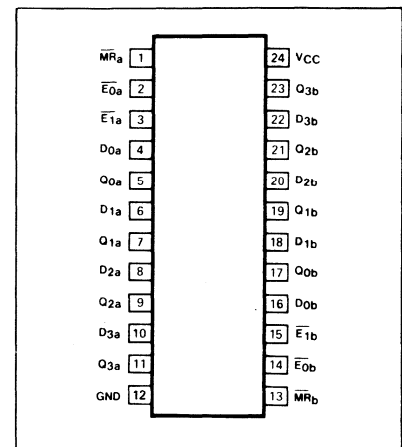
- Two independent 4-bit latches
- 2-input enable gates for easy expansion
- Asynchronous Master Reset

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +75°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N9308N	
Ceramic DIP	N9308F	S9308F
Flatpak		S9308Q

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		LIMITS
D ₀ -D ₃	Parallel Latch inputs	I _H (μA) I _L (mA)	60 -2.4
\bar{E}_0, \bar{E}_1	Enable (active LOW) inputs	I _H (μA) I _L (mA)	40 -1.6
\bar{MR}	Master Reset (active LOW) inputs	I _H (μA) I _L (mA)	40 -1.6
Q ₀ -Q ₃	Parallel Latch outputs	I _{OH} (μA) I _{OL} (mA)	-720 14.4

FUNCTIONAL DESCRIPTION

The 9308 has two independent 4-bit transparent latches. Each 4-bit latch is controlled by a 2-input active LOW Enable gate (\bar{E}_0 & \bar{E}_1). When both \bar{E}_0 & \bar{E}_1 are LOW, the data enters the latch and appears at the output. The outputs follow the data inputs as long as \bar{E}_0 and \bar{E}_1 are LOW. The data on the D inputs one setup time before the LOW-to-HIGH transition of \bar{E}_0 or \bar{E}_1 will be stored in the latch. The latched outputs remain stable as long as either \bar{E}_0 or \bar{E}_1 is HIGH.

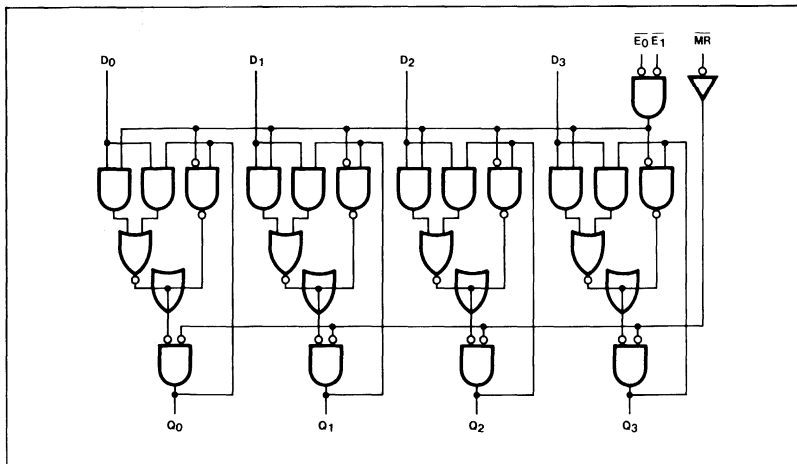
Each 4-bit latch has an active LOW asynchronous Master Reset (\bar{MR}) input. When LOW, the \bar{MR} input overrides the data and enable inputs and sets the four latch outputs LOW.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	\bar{MR}	\bar{E}_0	\bar{E}_1	D_n	Q_n
Reset (clear)	L	X	X	X	L
Enable latch	H	L	L	L	L
	H	L	L	H	H
Latch data	H	↑	L	l	L
	H	L	↑	h	H

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Enable transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Enable transition
 X = Don't care
 ↑ = LOW-to-HIGH Enable transition

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0$	-20	-70	mA
I_{CC} Supply current	$V_{CC} = \text{Max}, \text{All inputs} = 0V$		100	mA

NOTE

b. For family dc characteristics use the 54/74 limits shown on the inside front cover.

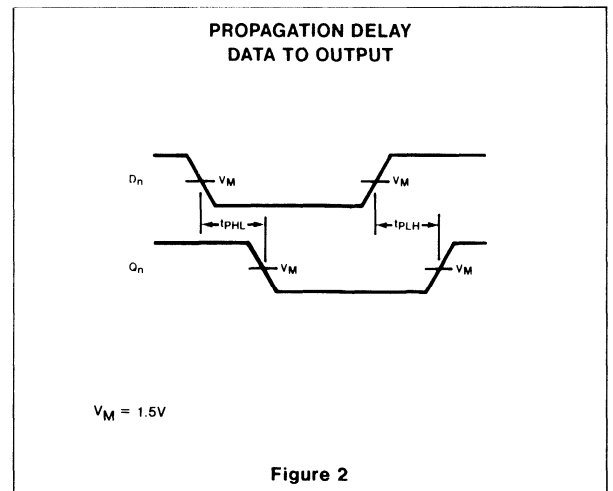
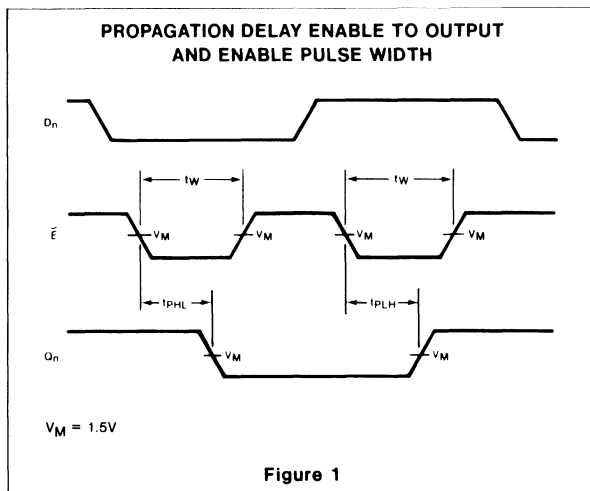
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	(Mil) S9308		(Com) N9308		UNIT
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output		30 18		35 22	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output		20 18		23 20	ns ns
t_{PHL}	Propagation delay MR to output		20		22	ns

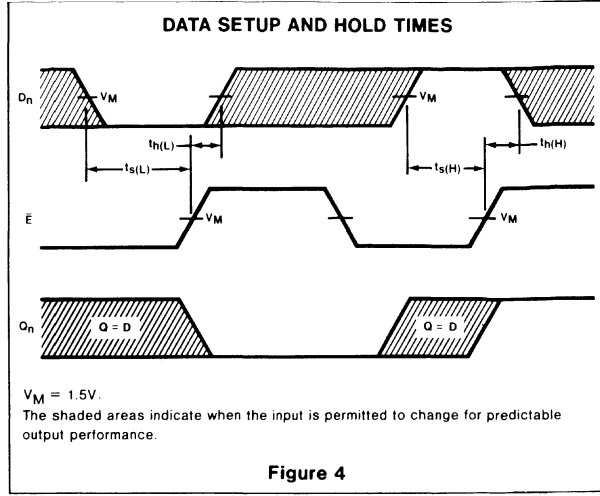
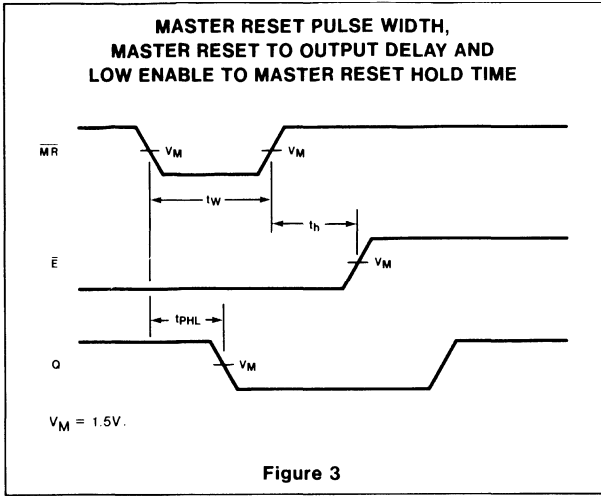
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	(Mil) S9308		(Com) N9308		UNIT
		Min	Max	Min	Max	
t_W	Enable pulse width	15		18		ns
t_W	Master Reset pulse width	15		18		ns
$t_S(H)$	Setup time HIGH Data to Enable	6.0		10		ns
$t_H(H)$	Hold time HIGH Data to Enable	-4.0		-2.0		ns
$t_S(L)$	Setup time LOW Data to Enable	10		12		ns
$t_H(L)$	Hold time LOW Data to Enable	4.0		8.0		ns
$t_H(L)$	Hold time LOW Enable to Master Reset to load HIGH	10		12		ns

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



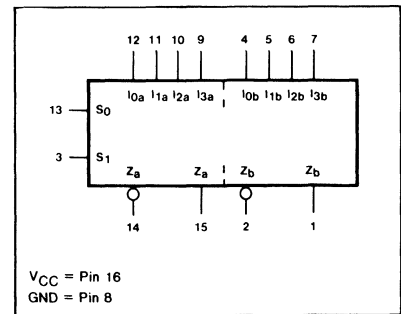
DESCRIPTION

The 9309 is a monolithic, high speed, Dual Four-Input digital Multiplexer circuit, consisting of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to multiplexer operation, the 9309 can generate any two functions of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss.

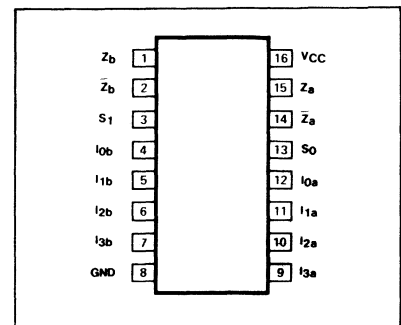
FEATURES

- Multifunction capability
- 25ns through delay
- On-Chip select logic decoding
- Fully buffered complementary outputs

LOGIC SYMBOL



PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +70°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N9309N	
Ceramic DIP	N9309F	S9309F
Flatpak		S9309W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION		LIMITS
S ₀ , S ₁	Common Select inputs	I _{IH} (μA) I _{IL} (mA)	40 -1.6
I _{0a} , I _{0b}	Data inputs from Source "0"	I _{IH} (μA) I _{IL} (mA)	40 -1.6
I _{1a} , I _{1b}	Data inputs from Source "1"	I _{IH} (μA) I _{IL} (mA)	40 -1.6
I _{2a} , I _{2b}	Data inputs from Source "2"	I _{IH} (μA) I _{IL} (mA)	40 -1.6
I _{3a} , I _{3b}	Data inputs from Source "3"	I _{IH} (μA) I _{IL} (mA)	40 -1.6
Z _a , Z _b	Multiplexer outputs	I _{OH} (μA) I _{OL} (mA)	-800 16
Z _a -bar, Z _b -bar	Complementary multiplexer outputs	I _{OH} (μA) I _{OL} (mA)	-800 16

FUNCTIONAL DESCRIPTION

The 9309 is a dual four-input multiplexer. It provides the ability to select two bits of either data or control from up to four sources, in one package.

The 9309 dual four-input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations or the outputs are shown below:

$$Z_a = I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0$$

$$Z_b = I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0$$

A common use of the 9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious use is as a function generator. The 9309 can generate any two functions of three variables. This is useful for implementing random gating functions.

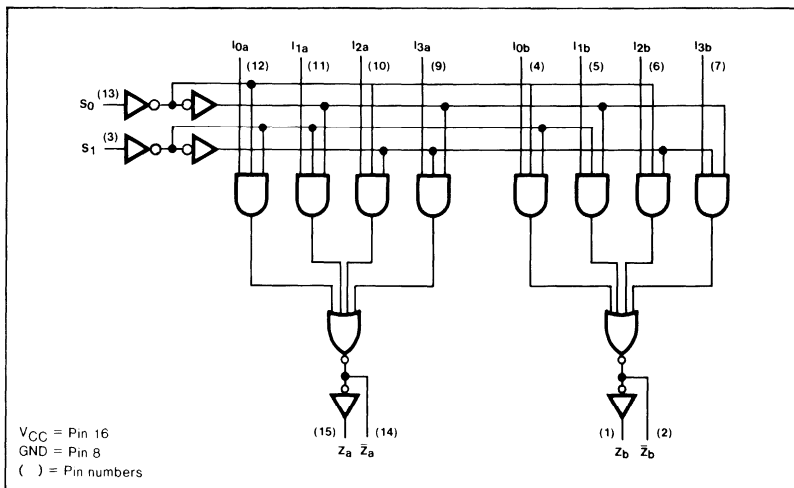
TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S ₀	S ₁	I _{0a}	I _{1a}	I _{2a}	I _{3a}	Z _a	\bar{Z}_a
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

S ₀	S ₁	I _{0b}	I _{1b}	I _{2b}	I _{3b}	Z _b	\bar{Z}_b
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = LOW voltage level
 H = HIGH voltage level
 X = Don't care

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-20	-70	mA
I _{CC} Supply current	V _{CC} = Max		44	mA

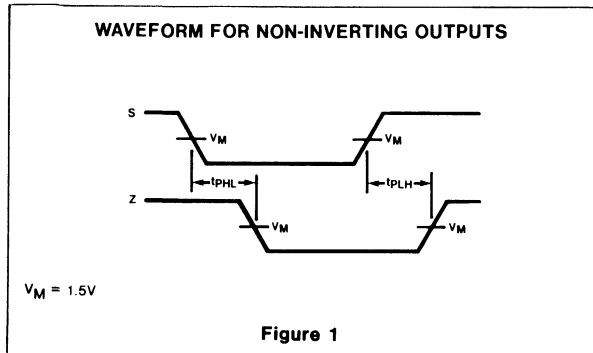
NOTE

b. For family dc characteristics use the 54/74 limits shown on the inside front cover.

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
t_{PLH}	Figure 1, $C_L = 15\text{pF}$		32	ns
t_{PHL}			32	ns

AC WAVEFORMS



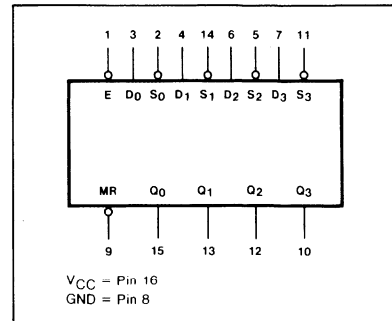
DESCRIPTION

The 9314 is a multifunctional 4-Bit Latch. The latch is designed for general purpose storage applications in high speed digital systems. All inputs feature diode clamping to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good ac noise immunity.

FEATURES

- Can be used as single input D latches or set reset latches
- Active level LOW Enable Gate input
- Overriding Master Reset
- 25 ns through delay

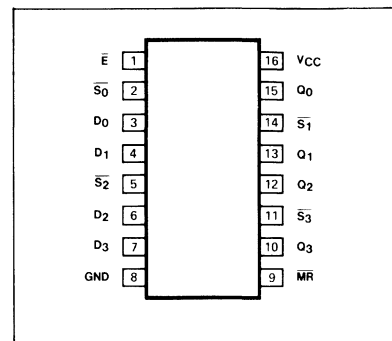
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+75^{\circ}C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N9314N	
Ceramic DIP	N9314F	S9314F
Flatpak		S9314W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		LIMITS
\bar{E}	Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)	40 -1.6
D ₀ -D ₃	Data inputs	I_{IH} (μA) I_{IL} (mA)	60 -2.4
S ₀ -S ₃	Set (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6
\bar{MR}	Master Reset (active LOW) inputs	I_{IH} (μA) I_{IL} (mA)	40 -1.6
Q ₀ -Q ₃	Latch outputs	I_{OH} (μA) I_{OL} (mA)	-800 16

FUNCTIONAL DESCRIPTION

Latch operation: The 9314 consists of four latches with a common active LOW enable and active LOW master reset. When the common enable goes HIGH, data present in the latches is stored and the state of a latch is no longer affected by the \bar{S} and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs LOW.

Each of the four latches can be operated in one of two modes:

D type latch: For D type operation the \bar{S} input of a latch is held LOW. While the common enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the enable goes HIGH.

Set/Reset latch: During set/reset operation when the common enable is LOW a latch is reset by a LOW on the D input, and latch will be reset. When the enable goes HIGH, the latch remains in the last state prior to the LOW to HIGH transition.

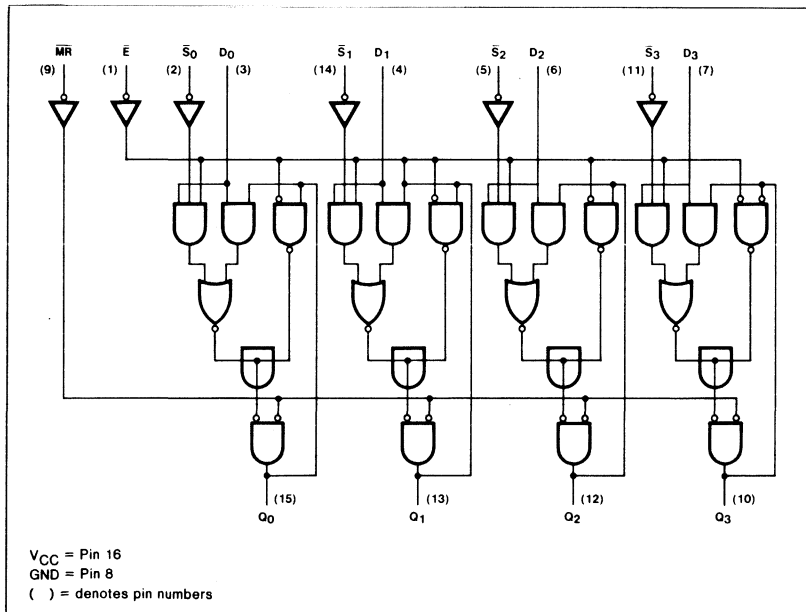
The two modes of operation of the 9314 latches are shown in the Truth Table.

FUNCTION TABLE

OPERATION	MR	\bar{E}	D	\bar{S}	Q_n
D Mode	H	L	L	L	L
	H	L	H	L	H
	H	H	X	X	Q_{n-1}
R/S Mode	H	L	L	L	L
	H	L	H	L	H
	H	L	L	H	L
	H	L	H	H	Q_{n-1}
	H	H	X	X	Q_{n-1}
Reset	L	X	X	X	L

X = Don't care
 L = LOW voltage level
 H = HIGH voltage level
 Q_{n-1} = Previous output state
 Q_n = Present output state

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$	-20	-70	mA
I_{CC} Supply current	$V_{CC} = \text{Max}$		55	mA

NOTE

b. For family dc characteristics use the 54/74 limits shown on the inside front cover.

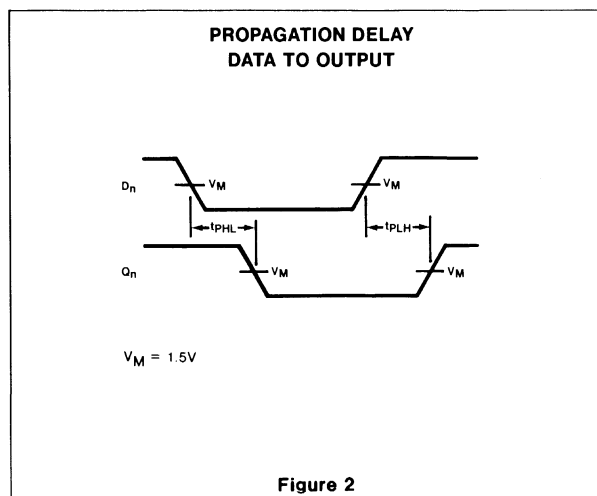
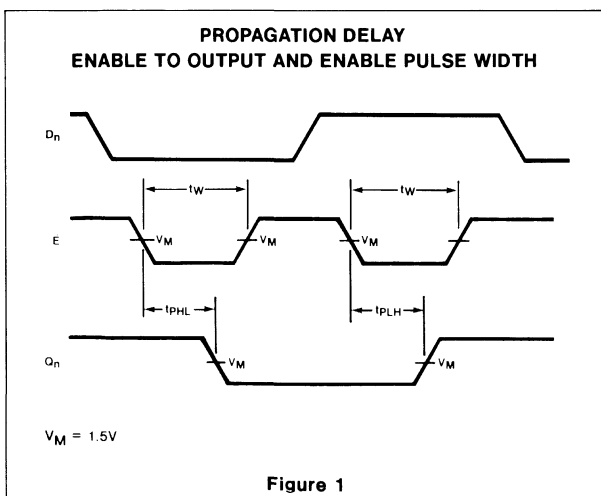
AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

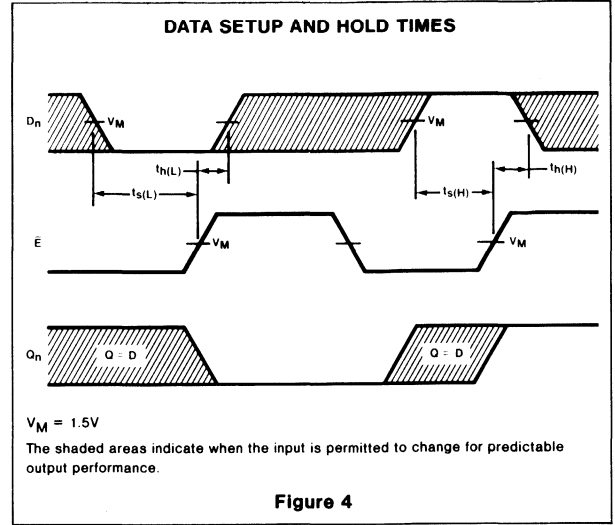
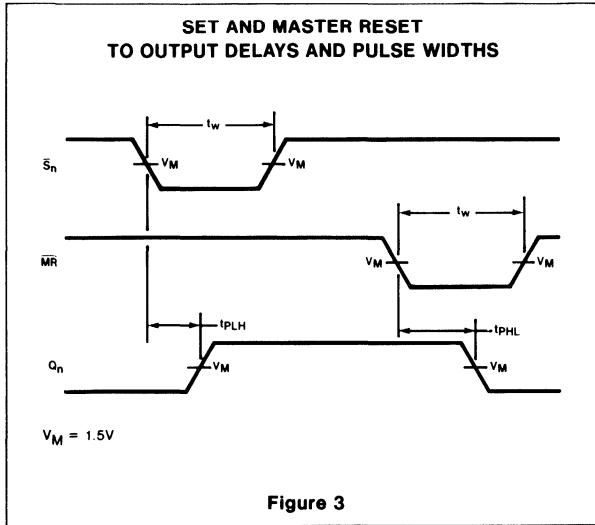
PARAMETER		TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output	Figure 1, $C_L = 15\text{pF}$		24 24	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Figure 2, $C_L = 15\text{pF}$		12 24	ns ns
t_{PHL}	Propagation delay MR to output	Figure 3, $C_L = 15\text{pF}$		18	ns
t_{PLH}	Propagation delay Set to output	Figure 3, $C_L = 15\text{pF}$		24	ns

AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Enable pulse width	Figure 1	18		ns
t_W	Master Reset pulse width	Figure 3	18		ns
$t_S(H)$	Setup time HIGH Data to Enable	Figure 4	5.0		ns
$t_H(H)$	Hold time HIGH Data to Enable	Figure 4	0		ns
$t_S(L)$	Setup time LOW Data to Enable	Figure 4	18		ns
$t_H(L)$	Hold time LOW Data to Enable	Figure 4	5.0		ns
$t_S(H)$	Setup time HIGH Data to positive going Set input		8.0		ns
$t_H(L)$	Hold time LOW Data to positive going Set input		8.0		ns

AC WAVEFORMS





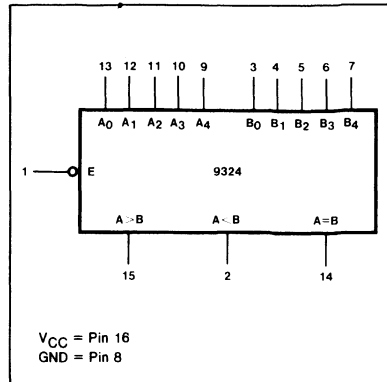
DESCRIPTION

The 9324 is a high speed Expandable Comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than" and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

FEATURES

- Three separate outputs . . . A < B, A > B, A = B
- Easily expandable
- Active low level enable input
- High drive output circuitry
- Input clamp diodes limit high speed
- Termination effects

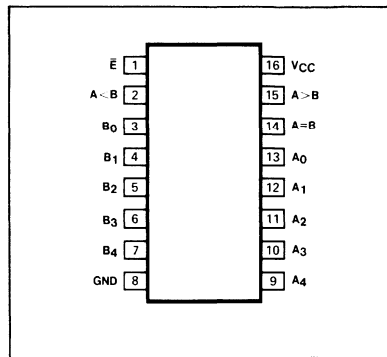
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} =5V ± 5%; T _A =0°C to +75°C	V _{CC} =5V ± 10%; T _A =-55°C to +125°C
Plastic DIP	N9324N	
Ceramic DIP	N9324F	S9324F
Flatpak		S9324W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	LIMITS	
E	Enable (active LOW) input	I _{IH} (μA)	80
		I _{IL} (mA)	-3.2
A ₀ -A ₄	Operand "A" inputs	I _{IH} (μA)	80
		I _{IL} (mA)	-3.2
B ₀ -B ₄	Operand "B" inputs	I _{IH} (μA)	80
		I _{IL} (mA)	-3.2
A < B	A less than B output	I _{OH} (μA)	-800
		I _{OL} (mA)	16
A > B	A greater than B output	I _{OH} (μA)	-800
		I _{OL} (mA)	16
A = B	A equal to B output	I _{OH} (μA)	-800
		I _{OL} (mA)	16

FUNCTIONAL DESCRIPTION

The 9324 5-bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable input (\bar{E}).

Tying the $A > B$ output from one device into an A input on another device and the $A < B$ output into the corresponding B input permits easy expansion.

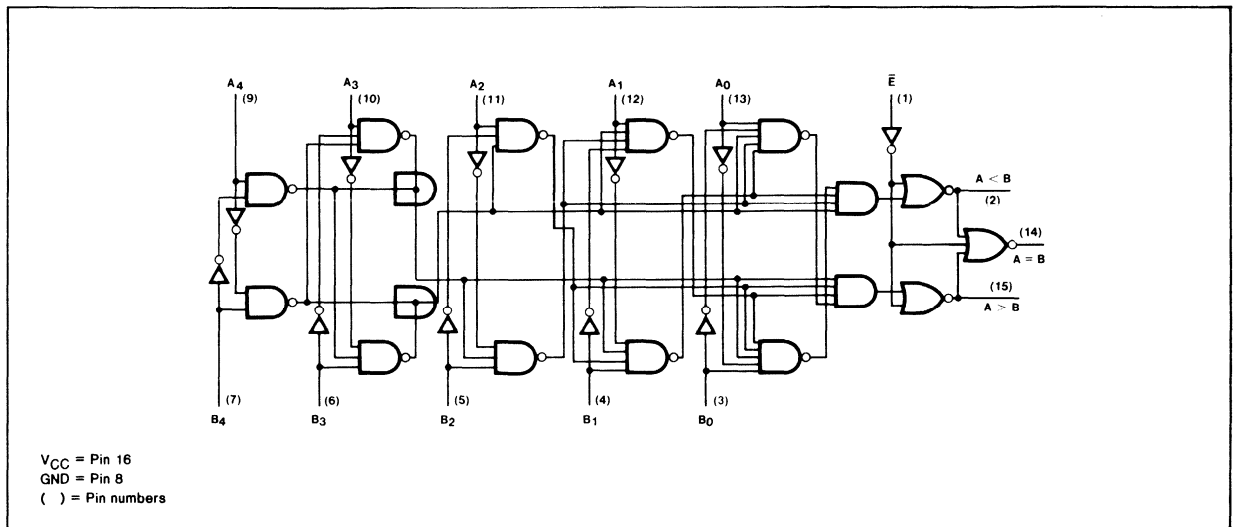
The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the $A > B$ output will be HIGH regardless of all other inputs except \bar{E} .

TRUTH TABLE

INPUTS			OUTPUTS		
\bar{E}	A_Y	B_Y	$A < B$	$A > B$	$A = B$
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word B > Word A		H	L	L

H = HIGH voltage level
 L = LOW voltage level
 X = Either HIGH or LOW voltage level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

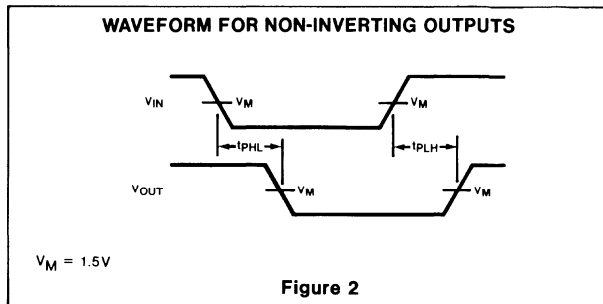
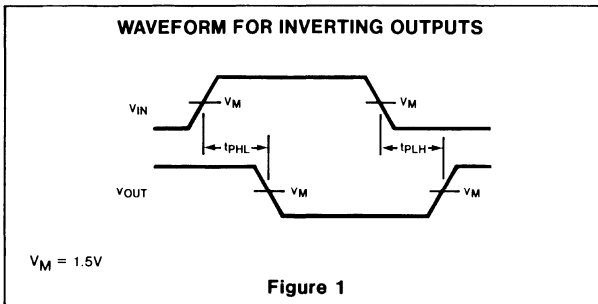
PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
I_{OS}	Output short circuit current	$V_{CC} = \text{Max}, V_{OUT} = 0V$		mA
I_{CC}	Supply current	$V_{CC} = \text{Max}$		mA

NOTE
 b. For family dc characteristics use the 54/74 limits shown on the inside front cover.

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to A=B output		48 45	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to A=B output		17 16	ns ns
t_{PLH} t_{PHL}	Propagation delay A input to A>B output		28 23	ns ns
t_{PLH} t_{PHL}	Propagation delay A input to A<B output		37 29	ns ns

AC WAVEFORMS



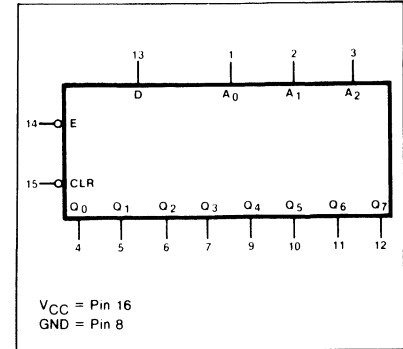
DESCRIPTION

The "9334" is an 8-Bit Addressable Latch with these control inputs; three Address inputs (A_0, A_1, A_2), an active LOW Enable input (\bar{E}) and an active LOW Clear input (\overline{CLR}). Each latch has a common D input and a separate Q output. The "9334" combines the features of a 1-of-8 demultiplexer and 8-bit transparent latch into one sixteen pin package.

FEATURES

- Combines demultiplexer and 8-bit latch
- Serial-to-Parallel capability
- Output from each storage bit available
- Random (Addressable) data entry
- Easily expandable
- Common Clear input
- Useful as dual 1-of-8 active HIGH decoder
- See 54LS/74LS259 for low power version
- See the NE590 for 250mA output version

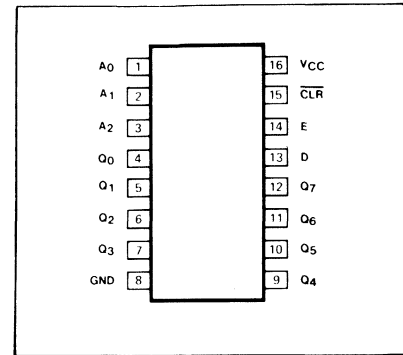
LOGIC SYMBOL



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+75^\circ C$	$V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$
Plastic DIP	N9334N	
Ceramic DIP	N9334F	S9334F
Flatpak		S9334W

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS	DESCRIPTION	LIMITS	
A_0-A_2	Address inputs	I_{IH} (μA)	40
		I_{IL} (mA)	-1.6
D	Data input	I_{IH} (μA)	40
		I_{IL} (mA)	-1.6
\bar{E}	Enable (active LOW) input	I_{IH} (μA)	60
		I_{IL} (mA)	-2.4
\overline{CLR}	Clear (active LOW) input	I_{IH} (μA)	40
		I_{IL} (mA)	-1.6
Q_0-Q_7	Parallel Latch outputs	I_{OH} (μA)	-720
		I_{OL} (mA)	9.6

FUNCTIONAL DESCRIPTION

The "9334" Addressable Latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see the function table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states

and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, ($\overline{\text{CLR}} = \overline{\text{E}} = \text{LOW}$) addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the address and data inputs.

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	$\overline{\text{CLR}}$	$\overline{\text{E}}$	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L

	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q=d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q=d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q=d	q ₃	q ₄	q ₅	q ₆	q ₇

	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q=d

H = HIGH voltage level steady state
 L = LOW voltage level steady state
 X = Don't care
 d = HIGH or LOW data one setup time prior to LOW-to-HIGH Enable transition
 q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

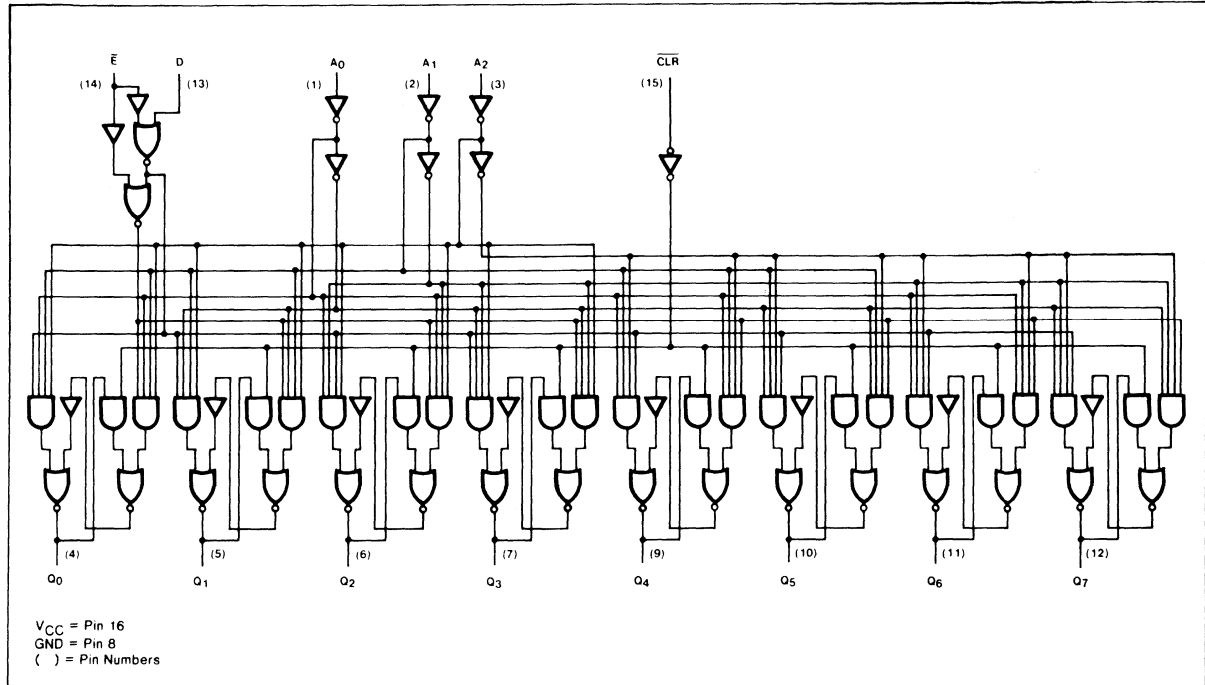
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE^(b)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = OV	-30	-100	mA
I _{CC} Supply current	V _{CC} = Max		86	mA

NOTE

b. For family dc characteristics use the 54/74 limits shown on the inside front cover.

LOGIC DIAGRAM



AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output		23 24	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output		35 24	ns ns
t_{PLH} t_{PHL}	Propagation delay Address to output		35 35	ns ns
t_{PHL}	Propagation delay clear to output		25	ns

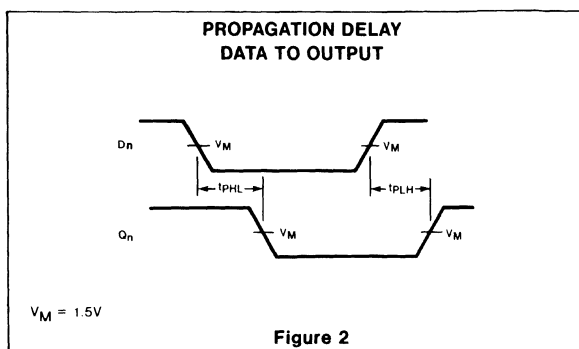
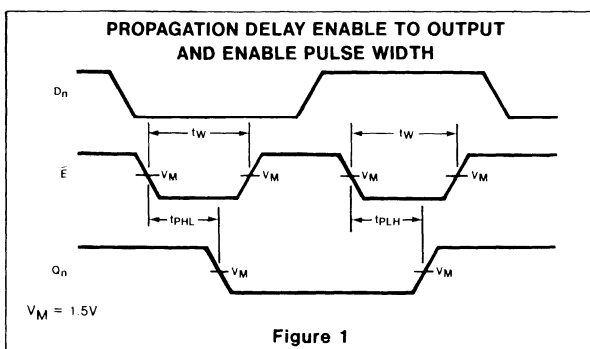
AC SETUP REQUIREMENTS: $T_A = 25^\circ\text{C}$ (See Section 4 for Test Circuits and Conditions)

PARAMETER	TEST CONDITIONS	LIMITS		UNIT
		Min	Max	
t_W	Enable pulse width	17		ns
t_W	Clear pulse width	17		ns
$t_s(H)$	Setup time HIGH Data to Enable	20		ns
$t_h(H)$	Hold time HIGH Data to Enable	0		ns
$t_s(L)$	Setup time LOW Data to Enable	17		ns
$t_h(L)$	Hold time LOW Data to Enable	0		ns
t_s	Setup time Address to Enable (See Note c)	5.0		ns
t_h	Hold time Address to Enable (See Note d)	5.0		ns

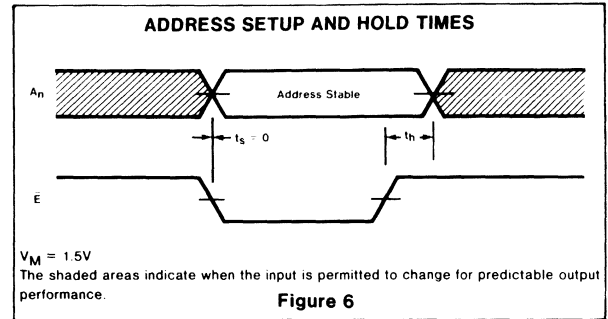
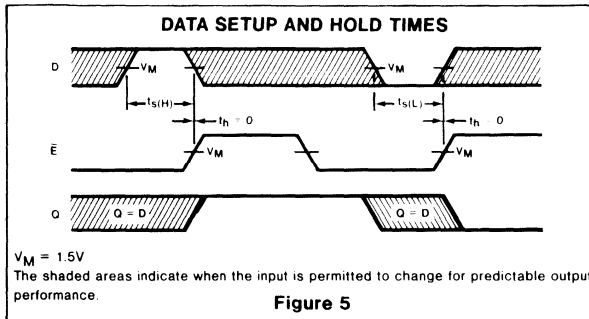
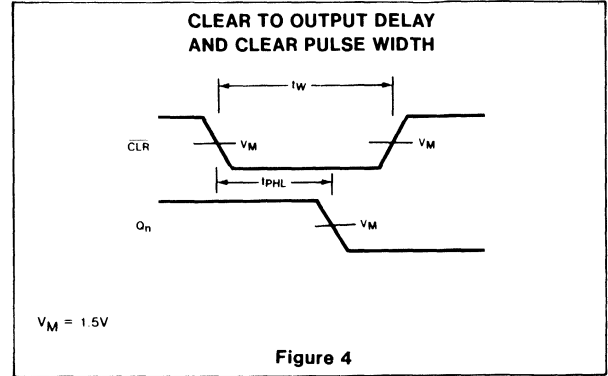
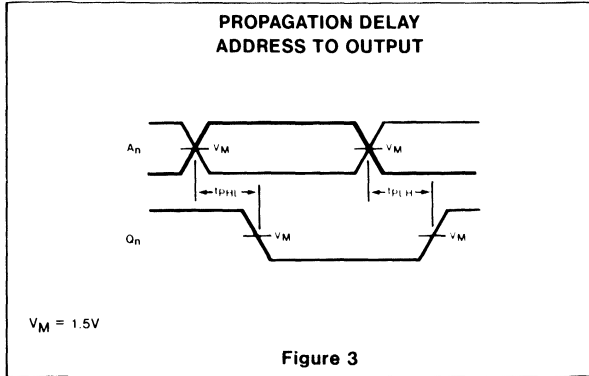
NOTES

- c. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- d. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS



AC WAVEFORMS (Cont'd)



SECTION 7

8T Interface Series

Data Sheets

The following tables contain the dc electrical characteristics for most of the 8T series of interface devices. You will find some of the dc characteristics duplicated on the individual data sheets. The dc data for the 8T125/126/127/128/129 and 8T363 is contained only on the individual data sheets and does not appear in the following tables.

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8T04			8T05			8T06			8T09			
		Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	all	2.0		all	2.0		all	2.0		all	2.0	
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage	all	0.8		all	0.8		all	0.8		all	0.8	
V _{CD}	Input clamp diode voltage	V _{CC} = Min I _{IN} = -12mA	all	-1.5		all	-1.5		all	-1.5		all	-1.5	
V _{BD}	Input breakdown voltage	V _{CC} = Max, I _{IN} = 10mA	all	5.5		all	5.5		all	5.5		all	5.5	
V _{OL}	Output LOW voltage	V _{CC} = Min	RBO	0.4 I _{OL} = 4.8mA		RBO	0.4 I _{OL} = 4.8mA		RBO	0.4 I _{OL} = 4.8mA		all	0.4 I _{OL} = 40mA	
		V _{CC} = Min	A-G	0.5 I _{OL} = 40mA		A-G	0.3 I _{OL} = 500μA		A-G	0.5 I _{OL} = 40mA				
V _{OH}	Output HIGH voltage	V _{CC} = Min	RBO	3.1 I _{OH} = -160μA		RBO	3.1 I _{OH} = -160μA		RBO	3.1 I _{OH} = -160μA		all	2.4 I _{OH} = -5.2mA	
		V _{CC} = Min				A-G	3.9 I _{OH} = -500μA							
I _{OH}	Output HIGH current (open collector)	V _{CC} = Min	A-G	100 V _{OUT} = 6V					A-G	100 V _{OUT} = 6V				
I _{OZH}	Output "off" current HIGH (3-state)	V _{CC} = Max V _{OUT} = 2.4V										all	-40	
I _{OZL}	Output "off" current LOW (3-state)	V _{CC} = Max V _{OUT} = 0.4V										all	40	
I _{IH}	Input HIGH current	V _{CC} = Max, V _{IN} = 4.5V	RBI LT BI a-d	40 160 80 80		RBI LT BI a-d	40 160 80 80		RBI LT BI a-d	40 160 80 80		all	40	
I _{IL}	Input LOW current	V _{CC} = Max V _{IN} = 0.4V	RBI LT BI a-d	-1.2 -10 -2.2 -1.6		RBI LT BI a-d	-1.2 -10 -2.2 -1.6		RBI LT BI a-d	-1.2 -10 -2.2 -1.6		all	-2.0	
I _{OS}	Output short circuit current	V _{CC} = Max V _{OUT} = 0V										all	-40	-120
I _{CC}	Power supply current	V _{CC} = Max	Mil	75		Mil	75		Mil	75		V _{CC}	65	
			Com	85		Com	85		Com	85		V _{CC}	65	

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

8T10			8T13			8T14			8T15			8T18			8T20			UNIT
Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	
all	2.0		all	2.0		all	2.0		all	2.0		all	9.0		Dig. Dif.	2.0 4mV		V
all	0.8		all	0.8		all	0.8		all	0.8		all	6.5		Dig. Dif.	0.8 -4mV		V
all	-1.5		all	-1.5		S,A,B	-1.5											V
all	5.5		all	5.5		S,A,B	5.5		all	50 $I_{IN} = 0.1\text{mA}$					Dig.	5.5		V
all	0.4 $I_{OL} = 32\text{mA}$					all	0.4 $I_{OL} = 16\text{mA}$		all	-5.0 -7.0 $I_{OL} = 4\text{mA}$		all	0.35 $I_{OL} = 7.2\text{mA}$		all	0.4 $I_{OL} = 16\text{mA}$		V
																		V
all	2.4 $I_{OH} = -5.2\text{mA}$		all	2.4 $I_{OH} = -75\text{mA}$		all	2.6 $I_{OH} = -800\mu\text{A}$		all	5.0 7.0 $I_{OH} = -4\text{mA}$		all	3.4 $I_{OH} = -225\mu\text{A}$		all	2.4 $I_{OH} = -800\mu\text{A}$		V
																		V
				80 $V_{OUT} = 3\text{V}$														μA
all	-40																	μA
all	40																	μA
D_n CP others	40 40 50		all	40		R S A B	170 40 40 40		all	40		all	50 $V_{IN} = 30\text{V}$		PEC NEC CLR	40 40 40		μA μA μA
D_n CP others	-3.2 -3.2 -2.0		all	-1.6		S A B	-1.6 -1.6 -1.6		all	-1.6		all	-1.8		PEC NEC CLR	-2.4 -2.4 -1.6		mA mA mA mA
all	-40 -120		all	-30		all	-50 -100		all	-25 +25 $V_{OUT} = \pm 25\text{V}$					all	-20 -70		mA
V_{CC}	118		V_{CC}	60		V_{CC}	76		V_{CC}	16		V_{C1}	8.4		V_{CC}	55		mA
V_{CC}	118		V_{CC}	60		V_{CC}	76		V_{EE}	-28		V_{C2}	1.7		V_{EE}	-20		mA

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8T22			8T23			8T24			8T25		
		Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max
V_{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	all	1.9		all	2.0		all	1.7		Dis. Stb.	2.0 2.0	
V_{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	all	0.9		all	0.8		all	0.7		Dis. Stb.	0.8 0.8	
V_{CD} Input clamp diode voltage	$V_{CC} = \text{Min}$ $I_{IN} = -12\text{mA}$	all	-1.5		all	-1.5		S,A,B	-1.5		Dis. Stb.	-1.5 -1.5	
V_{BD} Input breakdown voltage	$V_{CC} = \text{Max}$, $I_{IN} = 10\text{mA}$				all	5.5		S,A,B	5.5		Dis. Stb.	5.5 5.5	
V_{OL} Output LOW voltage	$V_{CC} = \text{Min}$	all	0.45 $I_{OL} = 12.8\text{mA}$		all	0.15 $I_{OL} = -240\mu\text{A}$		all	0.4 $I_{OL} = 16\text{mA}$			0.4 $I_{OL} = 16\text{mA}$	
	$V_{CC} = \text{Min}$												
V_{OH} Output HIGH voltage	$V_{CC} = \text{Min}$		2.4 $I_{OH} = -960\text{mA}$					all	2.6 $I_{OH} = -800\mu\text{A}$			2.8 $I_{OH} = -1.5\text{mA}$	
	$V_{CC} = \text{Min}$												
I_{OH} Output HIGH current (open collector)	$V_{CC} = \text{Min}$				all	40 $V_{OUT} = 3\text{V}$						100 $V_{OUT} = 3.9\text{V}$	
I_{OZH} Output "off" current HIGH (3-state)	$V_{CC} = \text{Max}$ $V_{OUT} = 2.4\text{V}$												
I_{OZL} Output "off" current LOW (3-state)	$V_{CC} = \text{Max}$ $V_{OUT} = 0.4\text{V}$												
I_{IH} Input HIGH current	$V_{CC} = \text{Max}$, $V_{IN} = 4.5\text{V}$	all	60		all	40		S,A,B R	40 170 $V_R = 3.11\text{V}$		Dis. Stb.	40 40	
I_{IL} Input LOW current	$V_{CC} = \text{Max}$ $V_{IN} = 0.4\text{V}$	all	-1.6		all	-1.6		S,A,B	-1.6		Dis. Stb.	-1.6 -1.6	
I_{OS} Output short circuit current	$V_{CC} = \text{Max}$ $V_{OUT} = 0\text{V}$	all	-10	-40		-100	-250				all	-20	-70
I_{CC} Power supply current	$V_{CC} = \text{Max}$	V_{CC}	25		V_{CC}	60		V_{CC}	72		V_{CC}	40	

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

8T26A			8T28			8T30			8T31			8T32			8T33			UNIT
Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	
all	2.0		all	2.0		all	2.0											V
all	0.85		all	0.85		all	0.8											V
all	-1.0		all	-1.0					all	-1.0 $I_{IN} = -5mA$		all	-1.0 $I_{IN} = -5mA$		all	-1.0 $I_{IN} = -5mA$		V
all	5.5		all	5.5														V
Dvr	0.5 $I_{OL} = 48mA$		Dvr	0.5 $I_{OL} = 48mA$		TTL	0.4 $I_{OL} = 25mA$		all	0.55 $I_{OL} = 20mA$		all	0.55 $I_{OL} = 16mA$		all	0.55 $I_{OL} = 16mA$		V
Rec	0.5 $I_{OL} = 20mA$		Rec	0.5 $I_{OL} = 20mA$		Bus	0.4 $I_{OL} = 60mA$											V
Dvr	2.4 $I_{OH} = -10mA$		Dvr	2.4 $I_{OH} = -10mA$		TTL	3.0 $I_{OH} = -150\mu A$		all	2.4 $I_{OH} = -3.2mA$		all	2.4 $I_{OH} = -3.2mA$		all	2.4 $I_{OH} = -3.2mA$		V
Rec	3.25 $I_{OH} = -100\mu A$		Rec	3.25 $I_{OH} = -100\mu A$		MOS	4.25 $I_{OH} = -1.6mA$											V
						Bus	250 $V_{OUT} = 5.25V$											μA
all	100		all	100														μA
all	-100		all	-100														μA
all	25		all	25		E Wrap Rec MOS	40 40 80 200		all	100		all	100		all	100		μA μA μA μA
all	-0.2		all	-0.2		E Wrap Rec MOS	-1.6 -1.6 -3.2 -0.5		all	-0.55		all	-0.55		all	-0.55		mA mA mA mA
Dvr Rec	-50 -30	-150 -75	Dvr Rec	-50 -30	-150 -75				all	-20	-200							mA
V_{CC}	87		V_{CC}	110		V_{CC}	70		V_{CC}	150		V_{CC}	150		V_{CC}	150		mA
																		mA

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8T34			8T37			8T38		
		Pins	Min	Max	Pins	Min	Max	Pins	Min	Max
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	Dis. Rec	2.0 1.8	2.5	Dis. Rec	2.0 1.8	2.5	Dis. Rec	2.0 1.8	2.5
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	Dis. Rec	1.05	0.8 1.55	Dis. Rec	1.05	0.8 1.55	Dis. Rec	1.05	0.8 1.55
V _{CD} Input clamp diode voltage	V _{CC} = Min I _{IN} = -12mA	all		-1.5	all		-1.5	all		-1.5
V _{BD} Input breakdown voltage	V _{CC} = Max, I _{IN} = 10mA	all	5.5 I _{IN} = 1.0mA					all	5.5 I _{IN} = 1.0mA	
V _{OL} Output LOW voltage	V _{CC} = Min	Rec		0.4 I _{OL} = 16mA	all		0.4 I _{OL} = 16mA	Rec		0.4 I _{OL} = 16mA
	V _{CC} = Min	Dvr		0.5 I _{OL} = 50mA				Dvr		0.5 I _{OL} = 50mA
V _{OH} Output HIGH voltage	V _{CC} = Min	Rec	2.4 I _{OH} = -5.2mA		all	2.4 I _{OH} = -400μA		Rec	2.4 I _{OH} = -5.2mA	
	V _{CC} = Min	Dvr	2.4 I _{OH} = -10.4mA							
I _{OH} Output HIGH current (open collector)	V _{CC} = Min							Dvr		100
I _{OZH} Output "off" current HIGH (3-state)	V _{CC} = Max V _{OUT} = 2.4V			100						
I _{OZL} Output "off" current LOW (3-state)	V _{CC} = Max V _{OUT} = 0.4V			-100						
I _{IH} Input HIGH current	V _{CC} = Max, V _{IN} = 4.5V	all		50	Dis. Rec		80 50	Dis. Rec		50 100
I _{IL} Input LOW current	V _{CC} = Max V _{IN} = 0.4V	all		-1.6	Dis. Rec		-3.2 -0.05	Dis. Rec		-1.6 -0.05
I _{OS} Output short circuit current	V _{CC} = Max V _{OUT} = 0V	Rec Dvr	-18 -60	-55 -105	all	-18	-55	Rec	-18	-55
I _{CC} Power supply current	V _{CC} = Max	V _{CC}		60	V _{CC}		60	V _{CC}		60

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

8T80			8T90			8T93			8T94			8T95			8T96			UNIT
Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	
all	2.0		all	2.0		all	2.0		all	2.0		all	2.0		all	2.0		V
all	0.6		all	0.6		all	0.8		all	0.8		all	0.8		all	0.8		V
all	-1.5		all	-1.5		all	-1.2 $I_{IN} = -18\text{mA}$		all	-1.2 $I_{IN} = -18\text{mA}$		all	-1.5		all	-1.5		V
						all	5.5 $I_{IN} = 1.0\text{mA}$		all	5.5 $I_{IN} = 1.0\text{mA}$		all	5.5 $I_{IN} = 1.0\text{mA}$		all	5.5 $I_{IN} = 1.0\text{mA}$		V
all	0.35 $I_{OL} = 7.2\text{mA}$		all	0.35 $I_{OL} = 7.2\text{mA}$		all	0.5 $I_{OL} = 20\text{mA}$		all	0.5 $I_{OL} = 20\text{mA}$		all	0.5 $I_{OL} = 48\text{mA}$		all	0.5 $I_{OL} = 48\text{mA}$		V
all	1.0 $I_{OL} = 20\text{mA}$		all	1.0 $I_{OL} = 20\text{mA}$														V
						all	2.7 $I_{OH} = -1.0\text{mA}$					all	2.4 $I_{OH} = -5.2\text{mA}$		all	2.4 $I_{OH} = -5.2\text{mA}$		V
																		V
all	100 $V_{OUT} = 30\text{V}$		all	100 $V_{OUT} = 30\text{V}$					all	250 $V_{OUT} = 5.5\text{V}$								μA
												all	40		all	40		μA
												all	-40		all	-40		μA
all	25		all	25		all	10		all	10		all	40		all	40		μA μA μA μA
all	-1.6		all	-1.6		all	-0.4		all	-0.4		all	-0.4 disabled -0.04		all	-0.4 disabled -0.04		mA mA mA mA
						all	-40 -100					all	-40 -115		all	-40 -115		mA
V_{CC}	15.3		V_{CC}	22.9		V_{CC}	54		V_{CC}	54		V_{CC}	98		V_{CC}	89		mA
																		mA

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

8T INTERFACE DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8T97			8T98			8T380			UNIT
		Pins	Min	Max	Pins	Min	Max	Pins	Min	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	all	2.0		all	2.0		all	2.0	2.5	V
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	all		0.8	all		0.8	all	1.1	1.5	V
V _{CD} Input clamp diode voltage	V _{CC} = Min I _{IN} = -12mA	all		-1.5	all		-1.5	all		-1.5	V
V _{BD} Input breakdown voltage	V _{CC} = Max, I _{IN} = 10mA	all	5.5	I _{IN} = 1.0mA	all	5.5	I _{IN} = 1.0mA				V
V _{OL} Output LOW voltage	V _{CC} = Min	all		0.5 I _{OL} = 48mA	all		0.5 I _{OL} = 48mA	all		0.4 I _{OL} = 16mA	V
	V _{CC} = Min										V
V _{OH} Output HIGH voltage	V _{CC} = Min	all	2.4	I _{OH} = -5.2mA	all	2.4	I _{OH} = -5.2mA	all	2.4	I _{OH} = -400μA	V
	V _{CC} = Min										V
I _{OH} Output HIGH current (open collector)	V _{CC} = Min										μA
I _{OZH} Output "off" current HIGH (3-state)	V _{CC} = Max V _{OUT} = 2.4V	all		40	all		40				μA
I _{OZL} Output "off" current LOW (3-state)	V _{CC} = Max V _{OUT} = 0.4V	all		-40	all		-40				μA
I _{IH} Input HIGH current	V _{CC} = Max, V _{IN} = 4.5V	all		40	all		40	all		50	μA μA μA
I _{IL} Input LOW current	V _{CC} = Max V _{IN} = 0.4V	all		-0.4	all		-0.4	all		-0.05	mA
		all		disabled -0.04	all		disabled -0.04				mA mA mA
I _{OS} Output short circuit current	V _{CC} = Max V _{OUT} = 0V	all	-40	-115	all	-40	-115	all	-18	-55	mA
I _{CC} Power supply current	V _{CC} = Max	V _{CC}		98	V _{CC}		89	V _{CC}		40	mA
											mA

DESCRIPTION

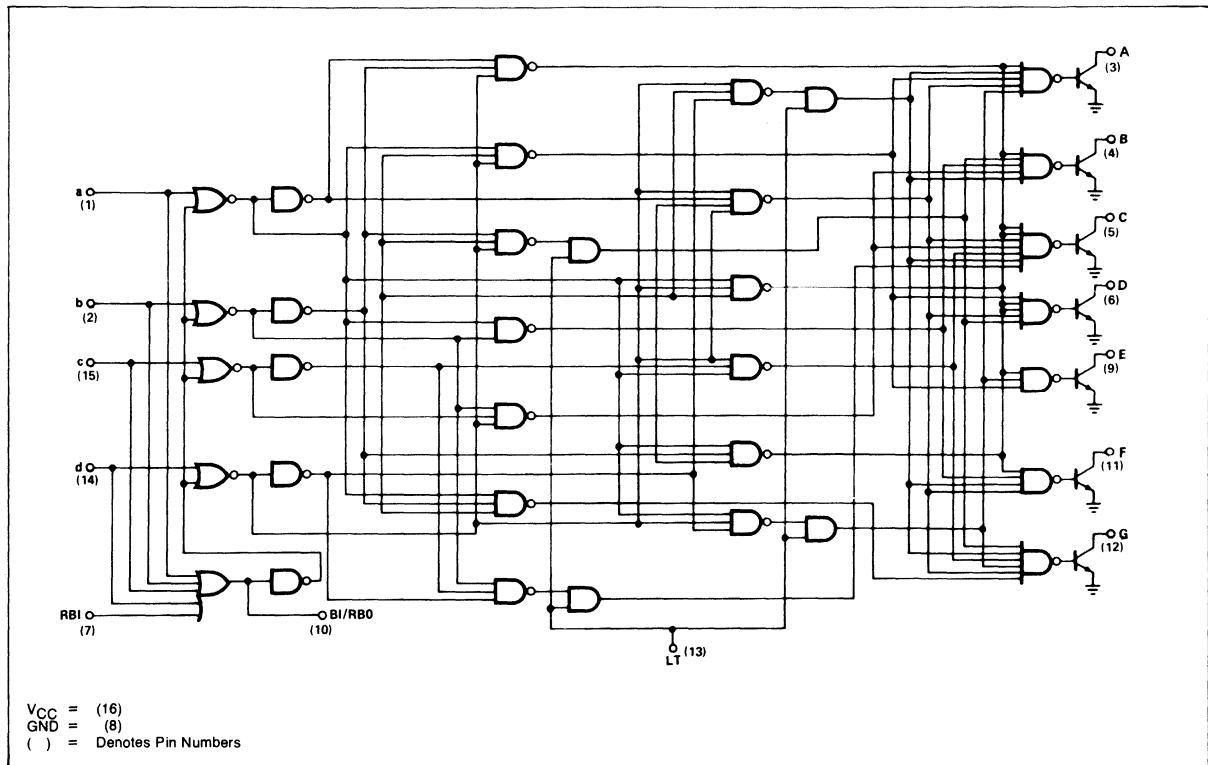
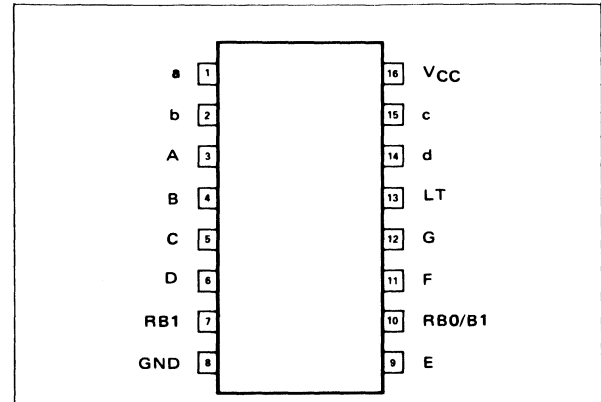
The 8T04 consists of the necessary logic to decode a 4-bit BCD code to seven segment (0 through 9) readout, as well as some selected signs and letters.

Incorporated in this device is a blanking circuit which turns all segments off when activated. The blanking circuit allows suppression of all numerically insignificant zeros, thereby presenting an easily read display.

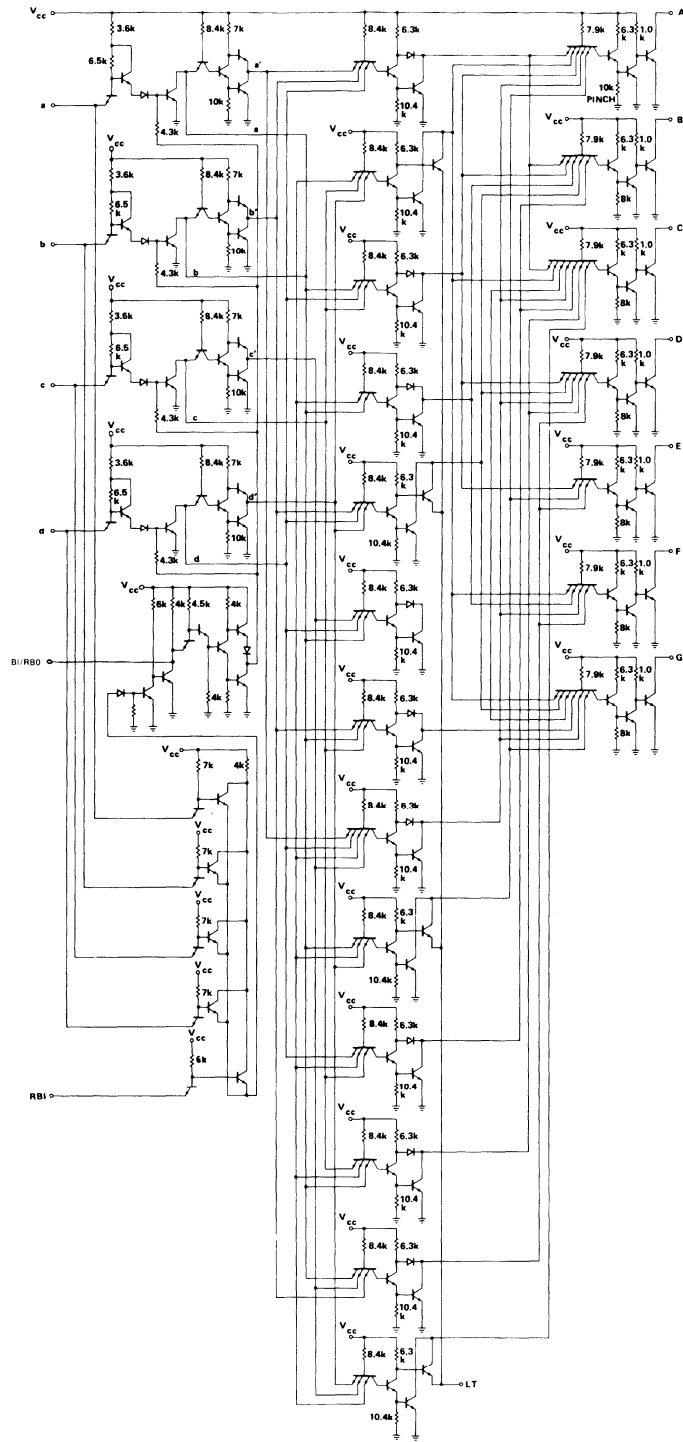
Also included is the necessary circuitry to implement suppression of leading and/or trailing zeros. A Lamp Test control is provided to turn all segments on. The Lamp Test allows the viewer to check the validity of the display lamps.

High performance bare collector output transistors are used in the 8T04 for directly driving incandescent lamps or common anode LED displays.

PIN CONFIGURATION



SCHEMATIC DIAGRAM



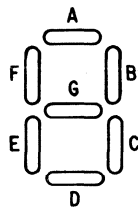
TRUTH TABLE

INPUTS						BI/RBO	OUTPUTS							DISPLAY CHARACTER
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	0	0	0	0	0	0	0	8
X	X	X	X	1	X	0 ^{1,2}	1	1	1	1	1	1	1	BLK
0	0	0	0	1	0	0 ^{1,2}	1	1	1	1	1	1	1	BLK
0	0	0	0	1	1	1 ²	0	0	0	0	0	0	1	0
0	0	0	1	1	X	1	1	0	0	1	1	1	1	1
0	0	1	0	1	X	1	0	0	1	0	0	1	0	2
0	0	1	1	1	X	1	0	0	0	0	1	1	0	3
0	1	0	0	1	X	1	1	0	0	1	1	0	0	4
0	1	0	1	1	X	1	0	1	0	0	1	0	0	5
0	1	1	0	1	X	1	1	1	0	0	0	0	0	6
0	1	1	1	1	X	1	0	0	0	1	1	1	1	7
1	0	0	0	1	X	1	0	0	0	0	0	0	0	8
1	0	0	1	1	X	1	0	0	0	1	1	0	0	9
1	0	1	0	1	X	1	1	1	1	1	1	1	0	0
1	0	1	1	1	X	1	1	1	1	1	1	1	1	1
1	1	0	0	1	X	1	0	0	0	1	0	0	0	BLK
1	1	0	1	1	X	1	1	1	0	1	1	1	1	2
1	1	1	0	1	X	1	1	1	1	0	0	0	1	3
1	1	1	1	1	X	1	1	1	1	1	1	1	1	BLK

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

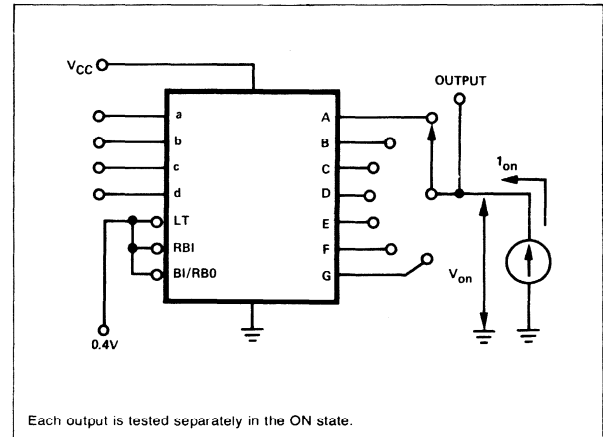
NOTE:

1. BI/RBO used as input.
2. BI/RBO should not be forced high when a,b,c,d, RBI terminals are low, or damage may occur to the unit.



*COMMA

TEST FIGURE FOR "0" OUTPUT VOLTAGE



DESCRIPTION

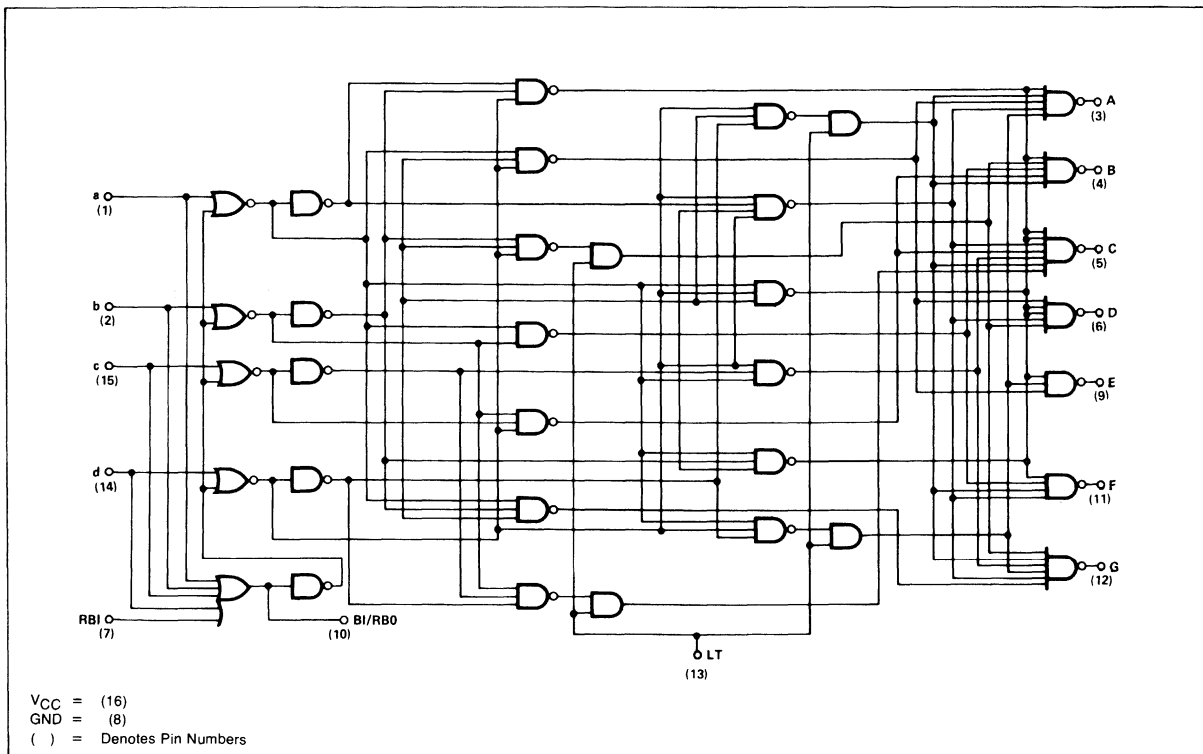
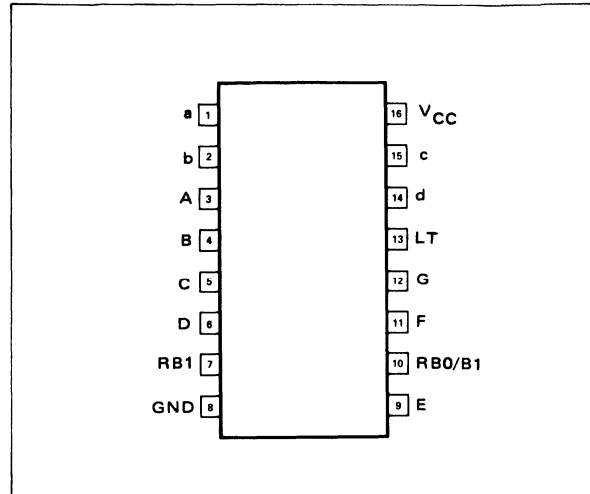
The 8T05 consists of the necessary logic to decode a 4-Bit BCD code to seven segment (0 through 9) readout as well as some selected signs and letters.

A Ripple Blanking input is provided to implement suppression of leading and/or trailing zeros. The suppression of all numerically insignificant zeros provides an easily read display.

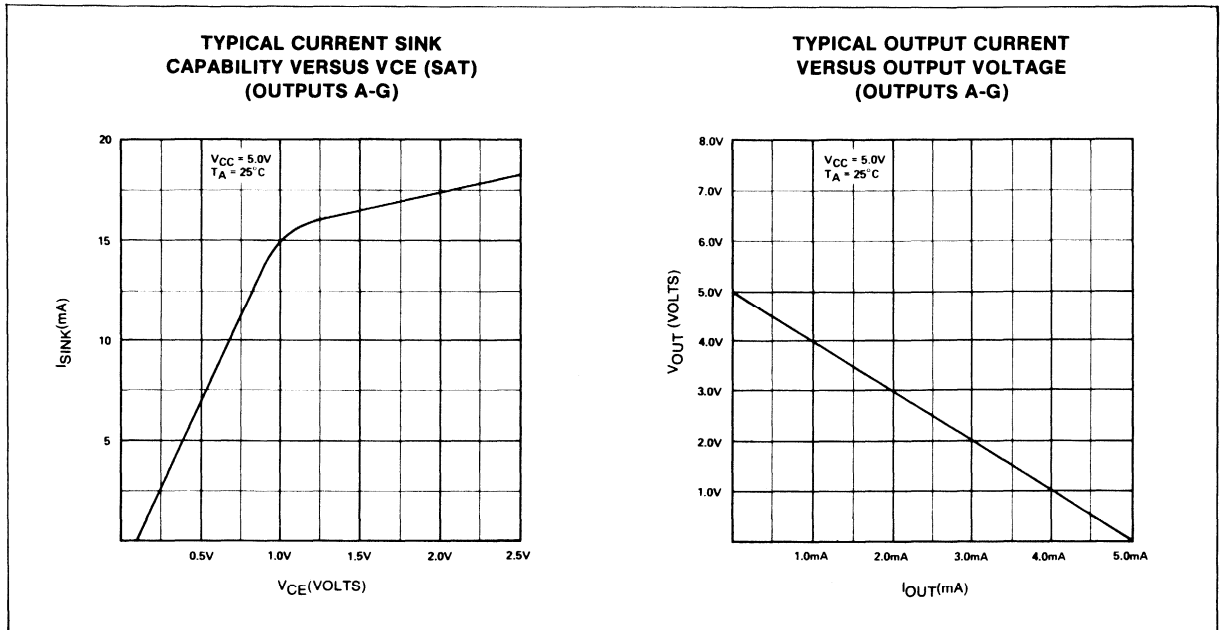
Incorporated in the Ripple Blanking output (BI/RBO) is the facility to ground all the outputs. Blanking of the outputs allows for intensity modulation.

A Lamp Test input is provided which, when grounded forces all segment outputs high. This allows the viewer to check the validity of the display presentation by testing the integrity of the lamps.

The 8T05 has resistor pullups on the outputs to provide source current sufficient to drive interfacing elements. This allows the unit to drive high voltage transistors for neon displays. The 8T05 can also be used to drive common cathode LED displays without the need for external resistors.

PIN CONFIGURATION

TYPICAL CHARACTERISTIC CURVES

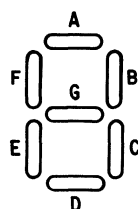


TRUTH TABLE

INPUTS				LAMP TEST	RBI	BI/RBO	OUTPUTS							DISPLAY CHARACTER
INPUT CODE							OUTPUT STATE							
d	c	b	a	LT		Note	A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	0
X	X	X	X	1	X	0 ^{1,2}	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 ²	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	0
0	0	1	0	1	X	1	1	1	0	1	1	0	1	1
0	0	1	1	1	X	1	1	1	1	0	0	0	1	1
0	1	0	0	1	X	1	0	1	1	0	0	1	1	1
0	1	0	1	1	X	1	1	0	1	1	0	1	1	1
0	1	1	0	1	X	1	0	0	1	1	1	1	1	1
0	1	1	1	1	X	1	1	1	1	0	0	0	0	0
1	0	0	0	1	X	1	1	1	1	1	1	1	1	1
1	0	0	1	1	X	1	1	1	1	0	0	1	1	1
1	0	1	0	1	X	1	0	0	0	0	0	0	1	1
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	1
1	1	0	1	1	X	1	0	0	1	0	0	0	0	0
1	1	1	0	1	X	1	0	0	0	1	1	1	0	0
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

- NOTE:
1. BI/RBO used as input.
 2. BI/RBO should not be forced high when a,b,c,d, RBI terminals are low, or damage may occur to the unit.

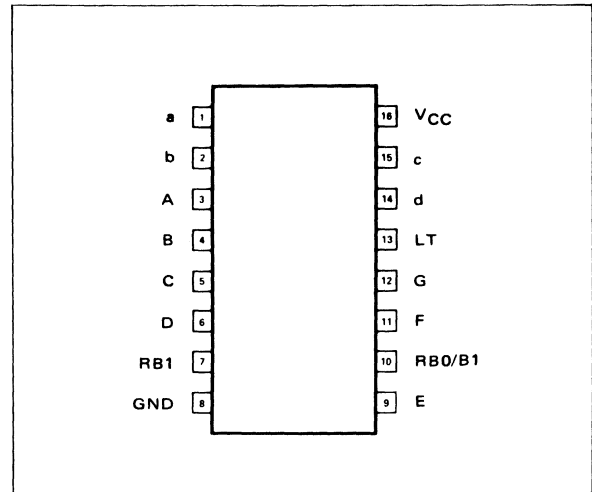


* COMMA

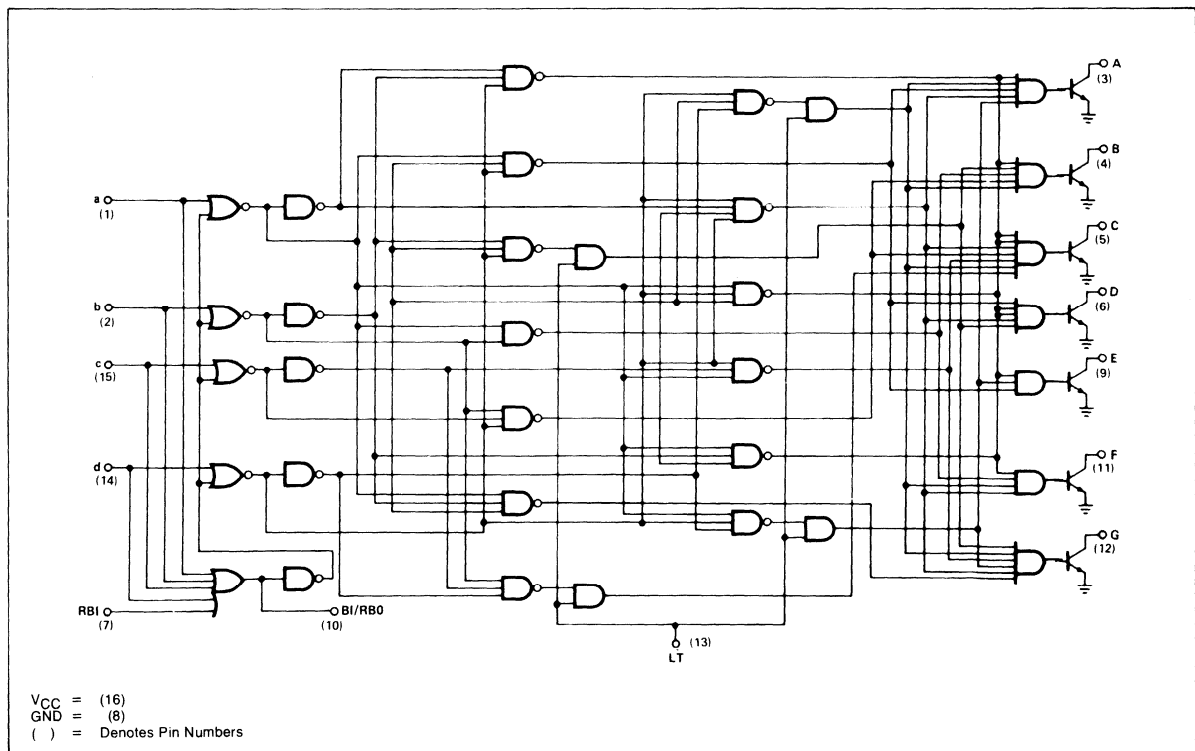
DESCRIPTION

The 8T06 is a monolithic MSI circuit consisting of the necessary logic to decode a 4-bit BCD code to drive 7-segment indicators directly. Open-collector outputs are used for high current source applications, such as driving common cathode LED displays and discrete active components. The 8T06 seven segment decoder/driver accepts a 4-bit binary code and decodes all possible inputs as decimals 0-9 or selected signs and letters. Auxiliary inputs are provided for maximum versatility. The ripple blanking inputs (RBI) and the ripple blanking output (RBO) may be used for automatic leading and/or trailing-edge zero suppression. The RBO output also acts as an overriding blanking input (BI) which may be used for intensity modulation or strobing of the display. A lamp test (LT) input is provided to check the integrity of the display by activating all outputs independent of the input code.

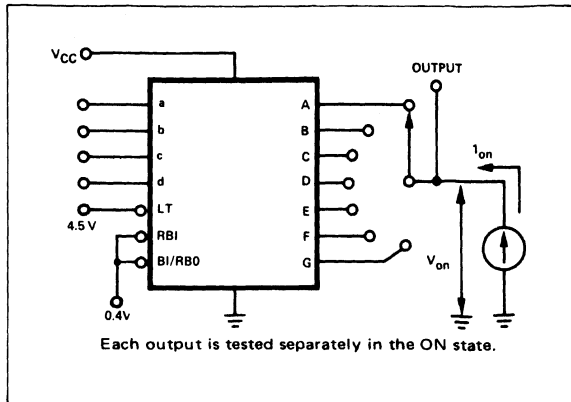
PIN CONFIGURATION



LOGIC DIAGRAM



TEST FIGURE FOR "0" OUTPUT VOLTAGE



TRUTH TABLE

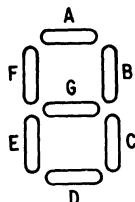
INPUTS						BI/RBO	OUTPUTS							DISPLAY CHARACTER
INPUT CODE				LAMP TEST	RBI		OUTPUT STATE							
d	c	b	a	LT			A	B	C	D	E	F	G	
X	X	X	X	0	X	X	1	1	1	1	1	1	1	8
X	X	X	X	1	X	0 ^{1,2}	0	0	0	0	0	0	0	BLK
0	0	0	0	1	0	0 ²	0	0	0	0	0	0	0	BLK
0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
0	0	0	1	1	X	1	0	1	1	0	0	0	0	1
0	0	1	0	1	X	1	1	1	0	1	1	0	1	2
0	0	1	1	1	X	1	1	1	1	1	0	0	1	3
0	1	0	0	1	X	1	0	1	1	0	0	1	1	4
0	1	0	1	1	X	1	1	0	1	1	0	1	1	5
0	1	1	0	1	X	1	0	0	1	1	1	1	1	6
0	1	1	1	1	X	1	1	1	1	0	0	0	0	7
1	0	0	0	1	X	1	1	1	1	1	1	1	1	8
1	0	0	1	1	X	1	1	1	1	0	0	1	1	9
1	0	1	0	1	X	1	0	0	0	0	0	0	1	0
1	0	1	1	1	X	1	0	0	0	0	0	0	0	BLK
1	1	0	0	1	X	1	1	1	1	0	1	1	1	8
1	1	0	1	1	X	1	0	0	1	0	0	0	0	1
1	1	1	0	1	X	1	0	0	0	1	1	1	0	1
1	1	1	1	1	X	1	0	0	0	0	0	0	0	BLK

* COMMA

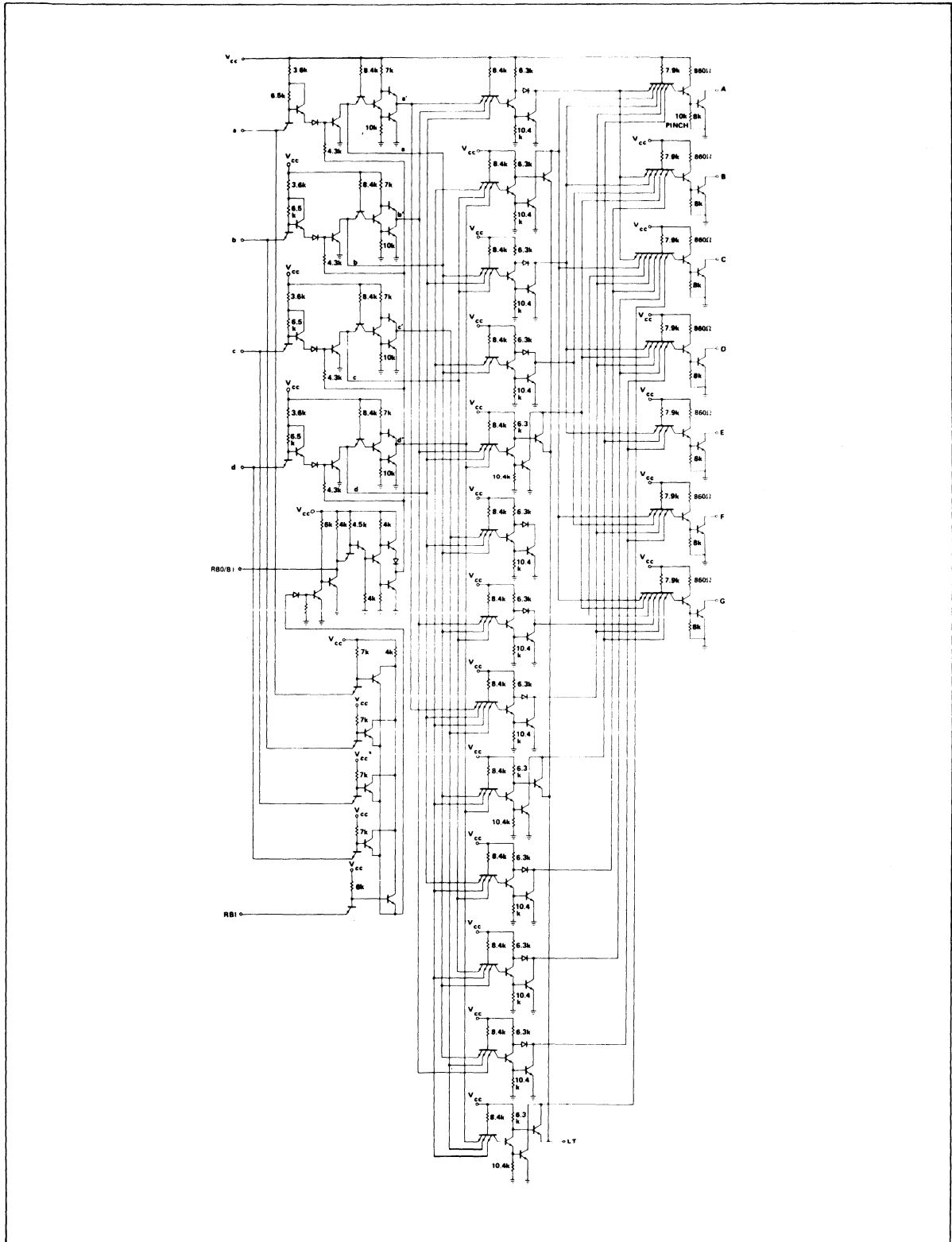
X = Don't care, either "1" or "0".
BI/RBO is an internally wired OR output.

NOTE:

1. BI/RBO used as input.
2. BI/RBO should not be forced high when a,b,c,d, RBI terminals are low, or damage may occur to the unit.



SCHEMATIC DIAGRAM

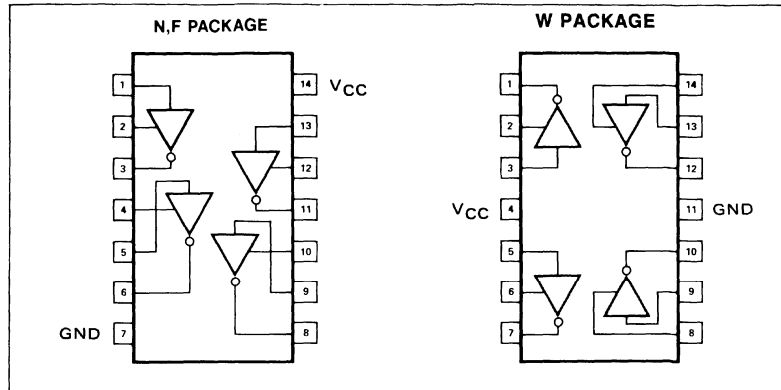


DESCRIPTION

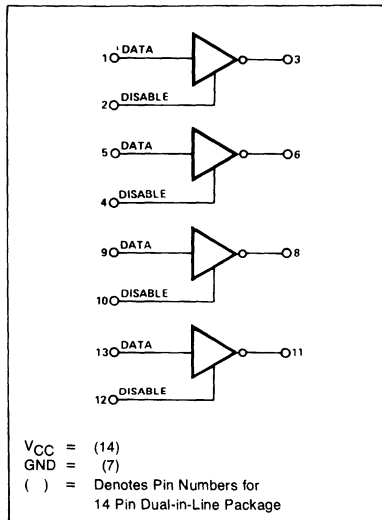
The 8T09 is a high speed quad bus driver device for applications requiring up to 25 loads interconnected on a single bus.

The tri-state outputs present a high impedance to the bus when disabled, (control input "1") and active drive when enabled (control input "0"). This eliminates the resistor pullup requirement while providing performance superior to open collector schemes. Each output can sink 40mA and drive 300pF loading with guaranteed propagation delay less than 20 nanoseconds.

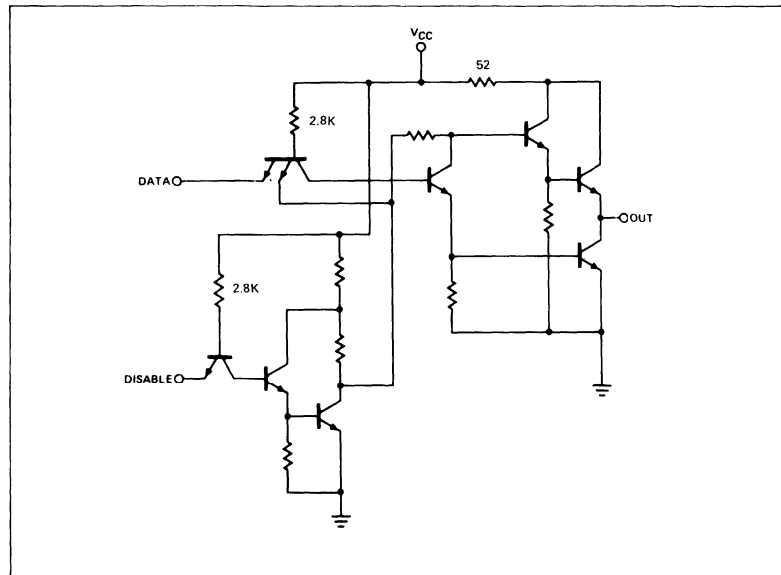
PIN CONFIGURATIONS



LOGIC DIAGRAM



SCHEMATIC DIAGRAM



TRUTH TABLE

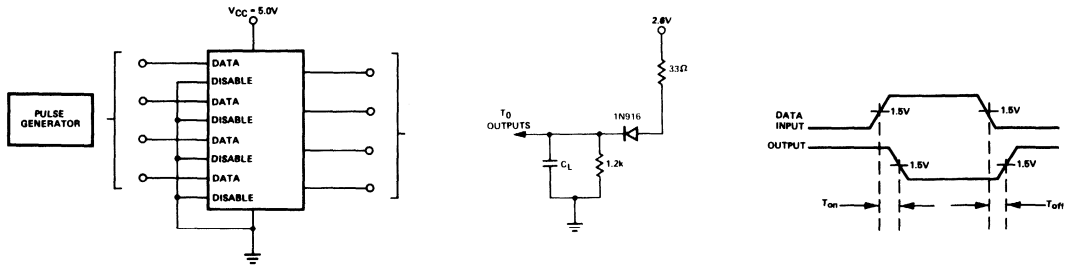
Data	Disable	Output
0	0	1
1	0	0
0	1	Hi-Z
1	1	Hi-Z

$T_A = 25^{\circ}C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS		TEST CONDITIONS	
	MAX	UNITS	OUTPUTS	NOTES
Propagation Delay Data to Output	10	ns	30pF load	9
	20	ns	300pF load	9
Disable to Output	14	ns	30pF load	9
	22	ns	300pF load	9
High Z to 0, 0 to High Z	14	ns	30pF load	9
	22	ns	300pF load	9

AC TEST FIGURES AND WAVEFORMS

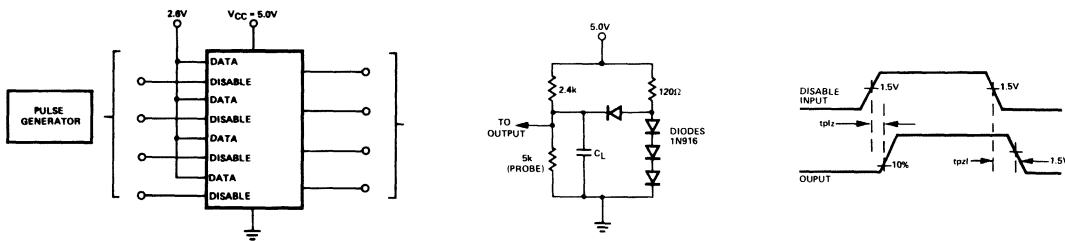
PROPAGATION DELAY (DATA TO OUTPUT)



INPUT PULSE:
 $t_r = t_f = 5\text{ns}$ (10% TO 90%)
 FREQ. = 1MHz (50% DUTY CYCLE)
 AMP. = 2.6V

FIGURE 1

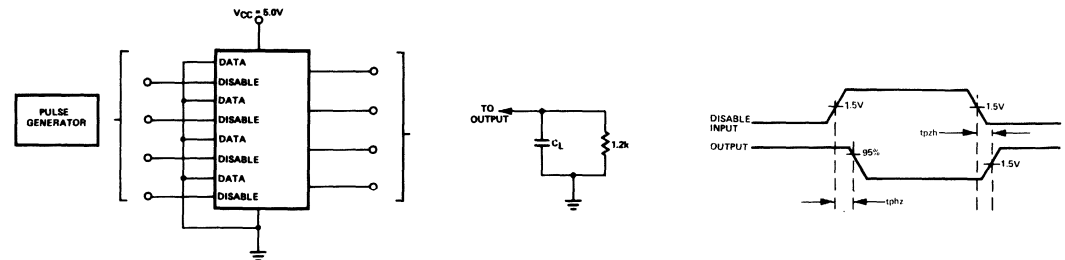
PROPAGATION DELAY ("0" TO HIGH Z, t_{pLz} ; HIGH Z TO 0, t_{pzL})



INPUT PULSE:
 $t_r = t_f = 5\text{ns}$ (10% TO 90%)
 FREQ. = 200kHz
 AMP. = 2.6V

FIGURE 2

PROPAGATION DELAY ("1" TO HIGH Z, t_{pHz} ; HIGH Z TO "1", t_{pzH})

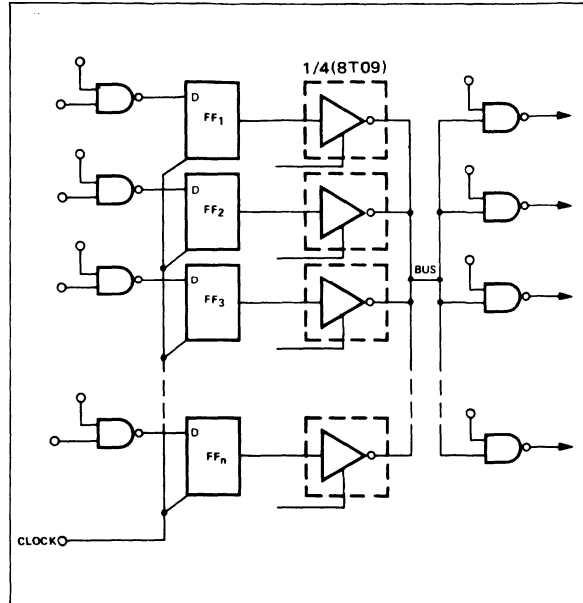


INPUT PULSE:
 $t_r = t_f = 5\text{ns}$ (10% TO 90%)
 FREQ. = 200kHz
 AMP. = 2.6V

FIGURE 3

The figure to right illustrates usage of the 8T09 in data processing logic. For example, FF₁ thru FF_n may represent bit X in each of several functions in a minicomputer (accumulators, MQ register, index registers, indirect address registers, etc.). Transfer from any source to any load, including transfers from one register to another, can take place along the single path labeled "BUS".

TYPICAL APPLICATION



DESCRIPTION

The 8T10 is a high speed Quad D flip-flop with tri-state outputs for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A common clear input resets all flip-flops upon application of a logic "1" level.

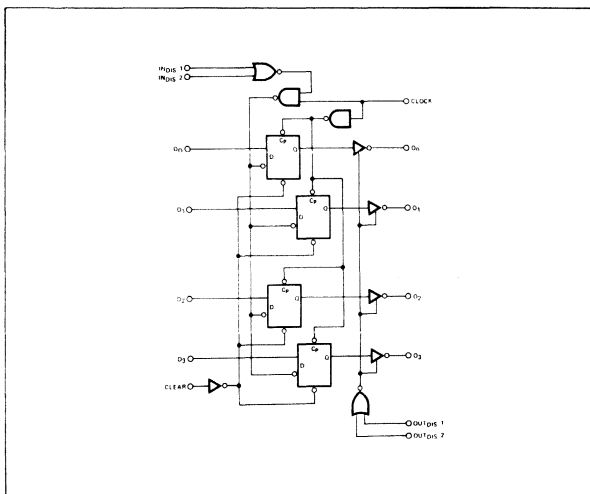
Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

TRUTH TABLE

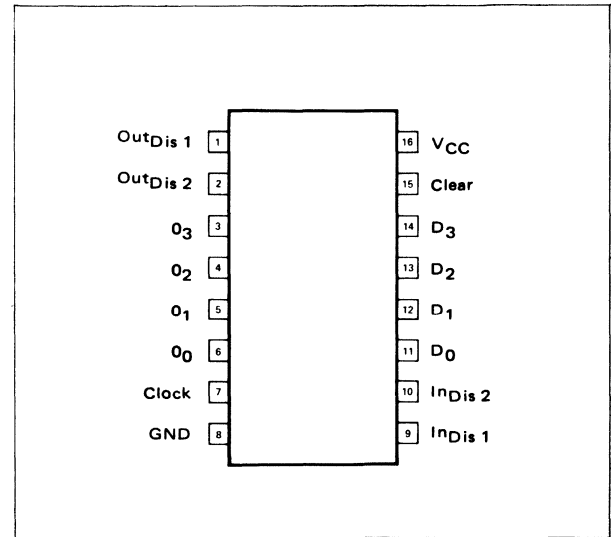
D _n	IN _{DIS}	OUT _{DIS}	O _{n+1}
0	0	0	0
1	0	0	1
X	1	0	O _n
X	X	1	High Z

O_n refers to the output state before a clock pulse.
 O_n + 1 refers to the output state after a clock pulse.

LOGIC DIAGRAM



PIN CONFIGURATION



T_A = 25° C and V_{CC} = 5.0V

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Propagation Delay (t _{on} , t _{off})				
Clock to Output				
C _L = 30pf		18	25	ns
C _L = 300pf		24	35	ns
Disable to Output				
High Z to Logic 0, t _{pZL} State (C _L = 300pf)		20	30	ns
Logic 0 to High Z, t _{pLZ} High Z (C _L = 300pf)		20	30	ns
Clear to Output				
C _L = 30pf		15	22	ns
C _L = 300pf		21	30	ns
Set Up Time, t _{setup}				
Data	+5	-1		ns
Input Disable		-6	0	ns
Hold Time, t _{hold}				
Data		-1	+5	ns
Reset Pulse Width	15			ns
Clock Frequency	35	50		MHz
Clock Pulse Width				
Positive		8	12	ns
Negative		8	12	ns

1. Measured to 1.5V level of output waveform.
2. Measured to 10% level of output waveform.
3. Refer to AC Test Circuits.

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY t_{on} , t_{off} (CLOCK TO OUTPUT)

DATA SETUP TIME, t_{setup}

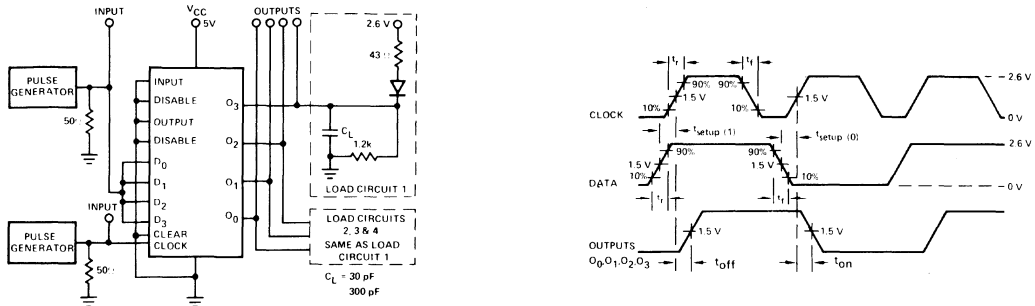


FIGURE 1

PROPAGATION DELAY (CLEAR TO OUTPUT)

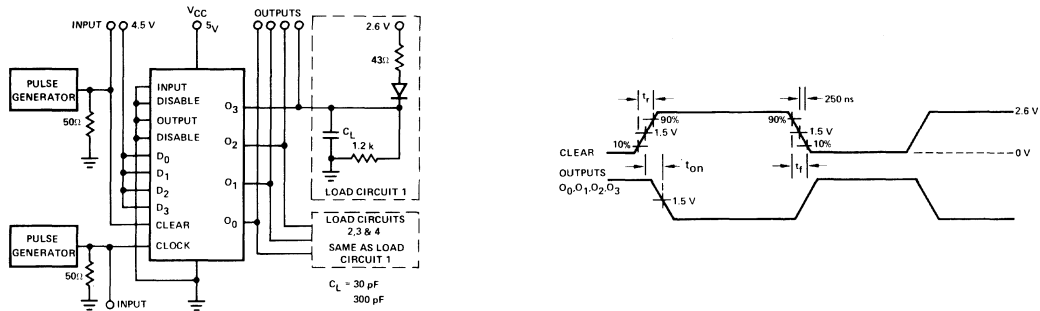


FIGURE 2

PROPAGATION DELAY (DATA HOLD TIME)

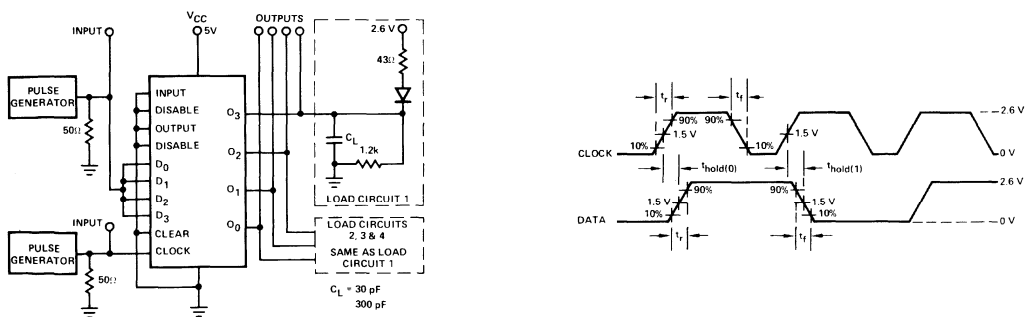
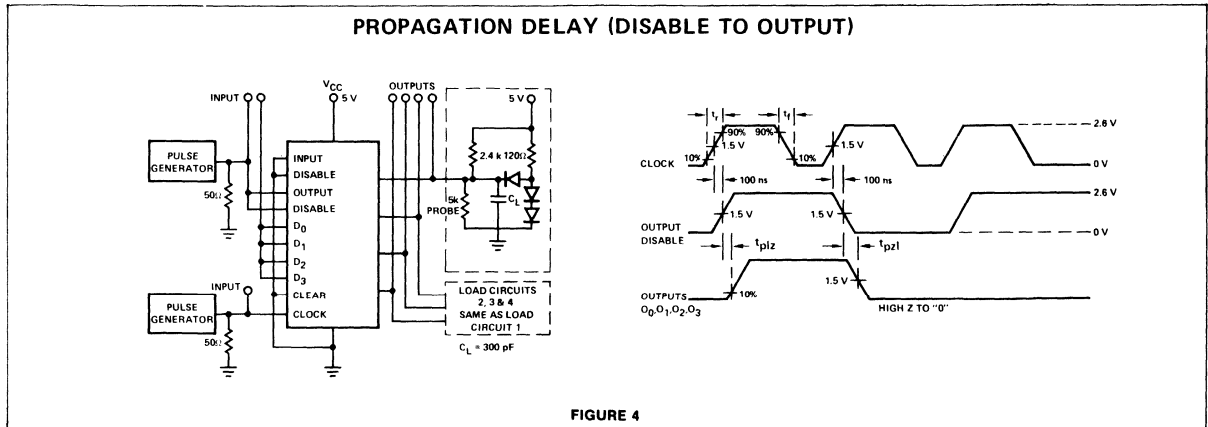
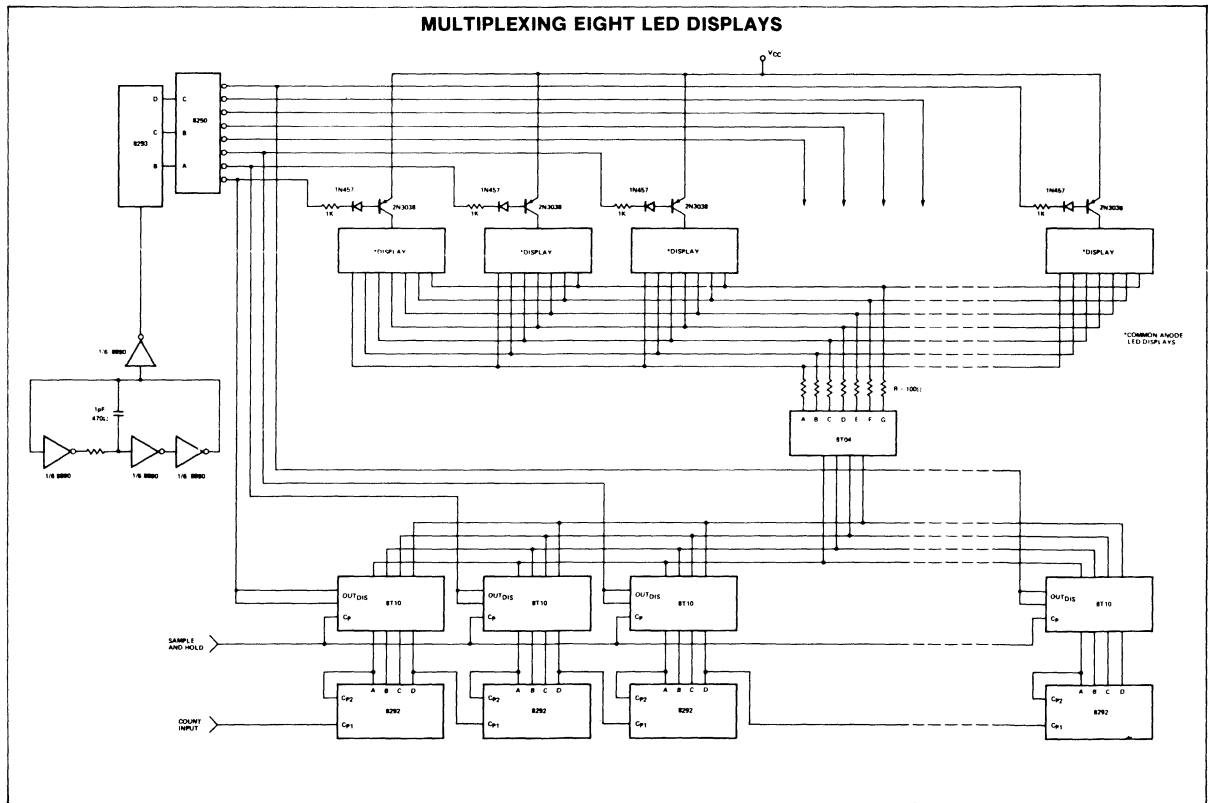


FIGURE 3

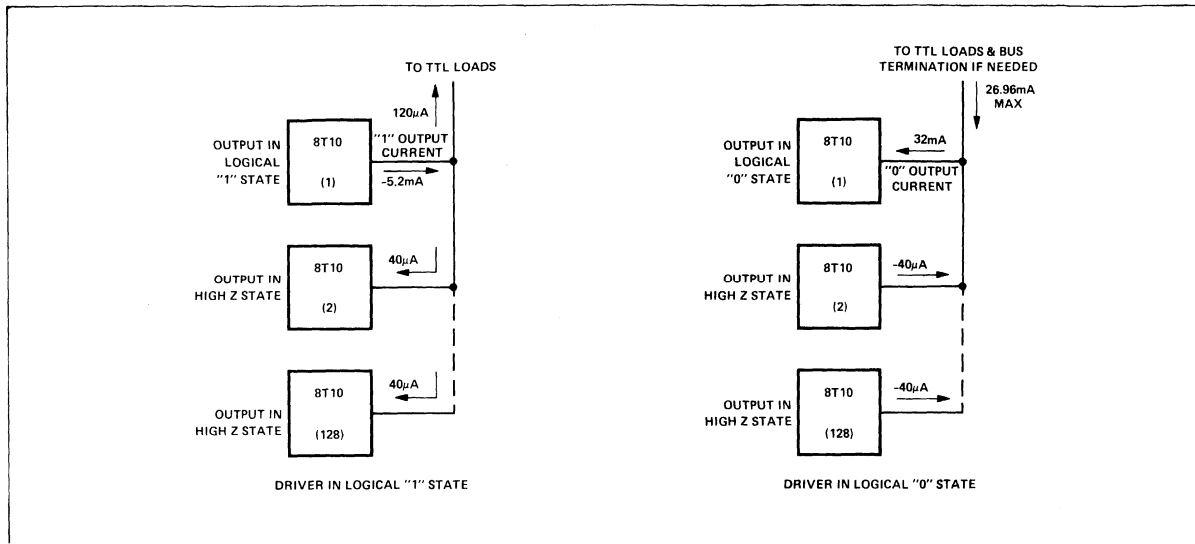
AC TEST FIGURES AND WAVEFORMS (Cont'd)



TYPICAL APPLICATIONS



TYPICAL APPLICATIONS



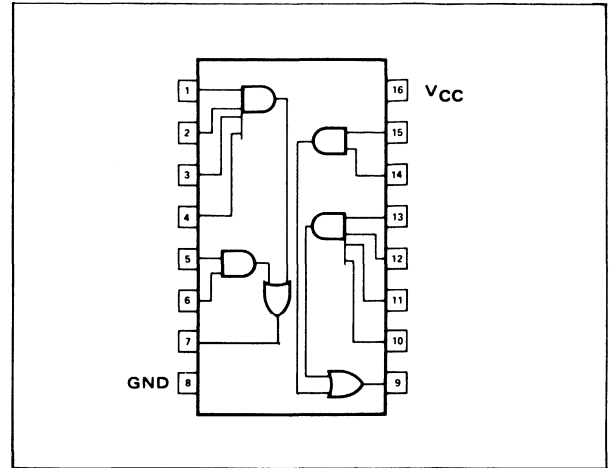
DESCRIPTION

The 8T13 is a monolithic Dual Line Driver designed to drive 50 ohm or 75 ohm coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The outputs are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with impedances of 50Ω to 500Ω.

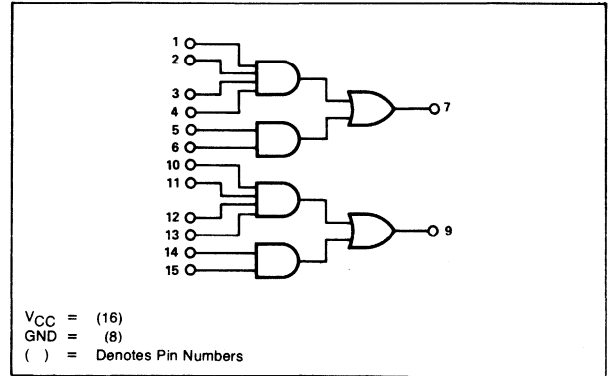
KEY DESIGN BENEFITS

- High-Power Drive Capability:
Specified at -75mA source current rating at 2.4 volts.
- Party-Line Operation:
Emitter-follower outputs enable two or more drivers to drive the same line. This permits multiple time-shared terminal connections since these drivers have no effect upon the transmission line unless activated.
- Input gating structure allows employment of the "OR" as well as the "AND" function.
- High Speed: $t_{on} = t_{off} = 20\text{ns}$ (max).
- Input Clamp Diodes: Protects inputs from line ringing.
- Single 5 Volt power supply.
- Short Circuit Protection:
Incorporates a latch-back short circuit protection feature which protects the device by limiting the current it may source when operating under conditions of zero load resistance.

PIN CONFIGURATION



LOGIC DIAGRAM



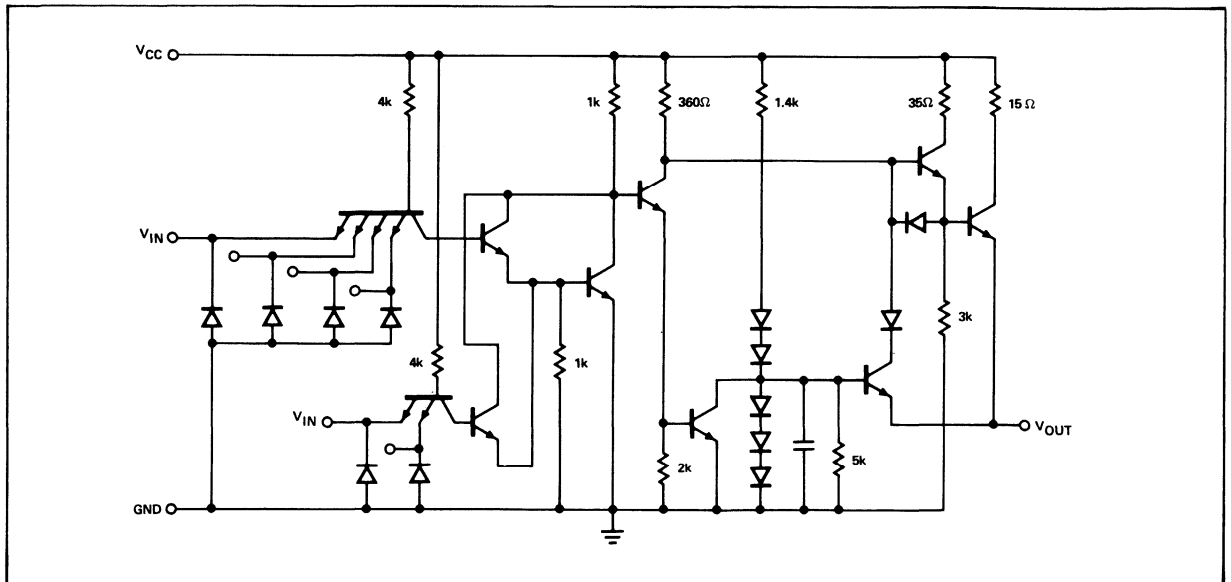
$T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{V}$

PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
t_{on} , Turn-On Delay		32	20	ns
t_{off} , Turn-Off Delay		22	20	ns

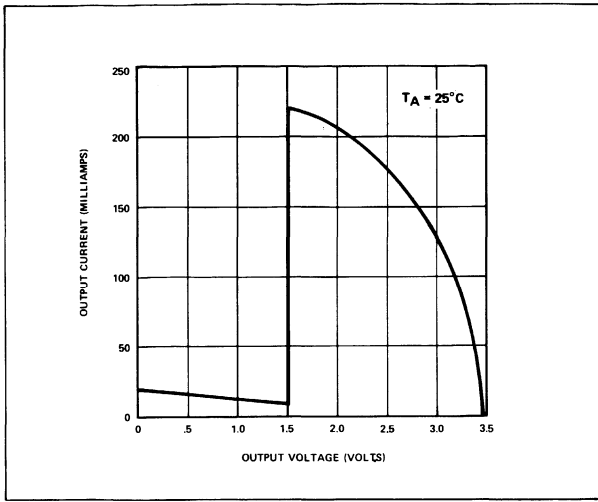
NOTES:

1. $R_L = 37\Omega$ to ground.
2. Load is 37Ω in parallel with 1000pF .
3. Reference AC Test Circuit and Pulse Requirements.

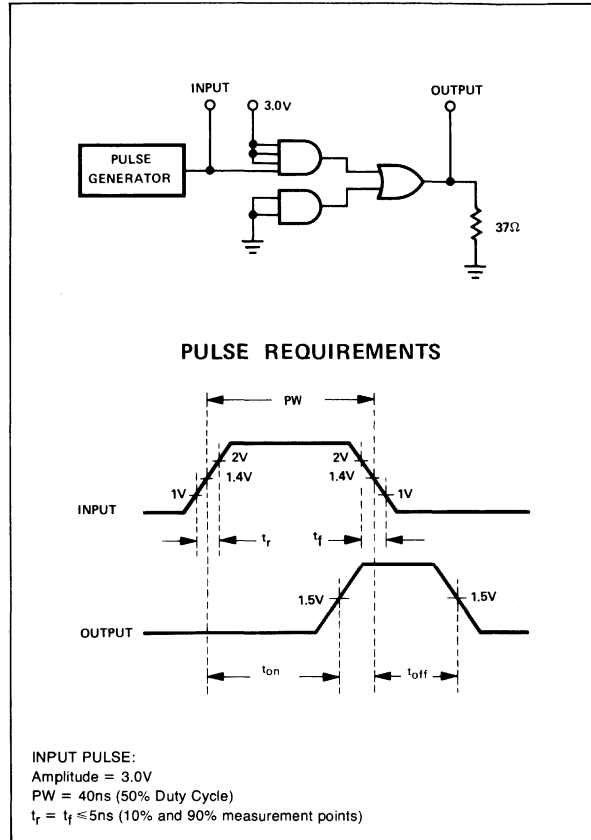
SCHEMATIC DIAGRAM



TYPICAL OUTPUT CURRENT VERSUS
 Ω OUTPUT VOLTAGE CURVE



AC TEST FIGURE AND WAVEFORMS



TYPICAL APPLICATIONS

A typical application for the 8T13 is shown in Figure 1. If only one line driver is to be used for each transmission line, the line may be terminated with 50 ohms on the receiving end only. See Figure 2.

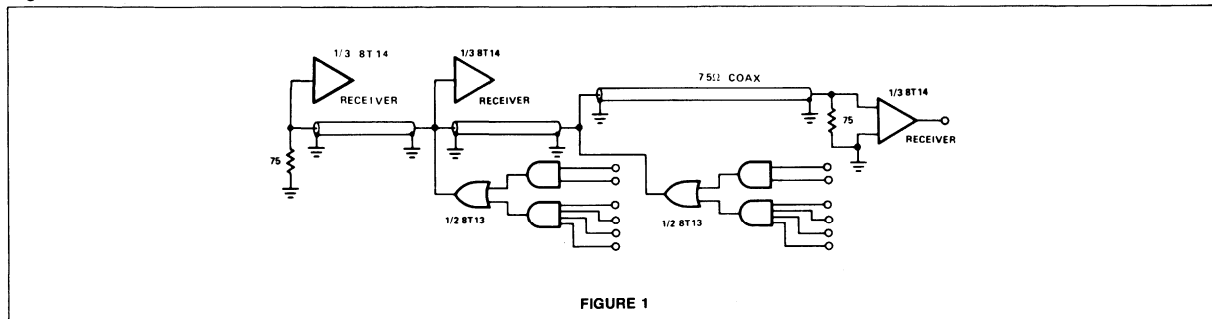


FIGURE 1

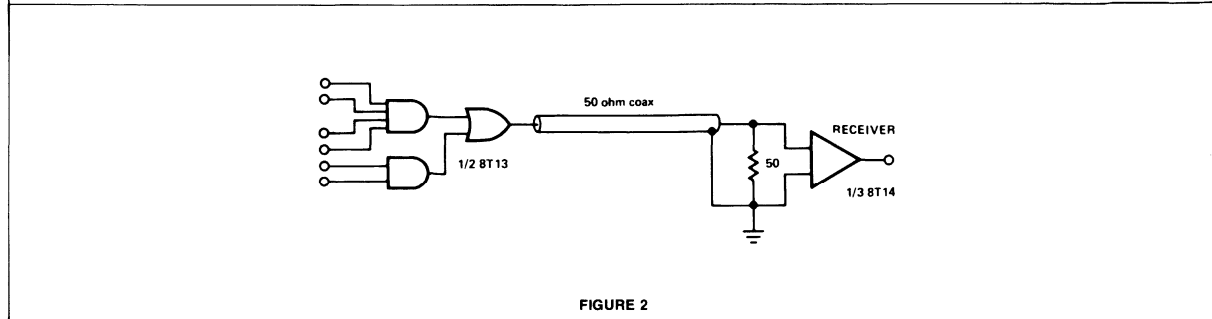


FIGURE 2

DESCRIPTION

The 8T14 is a Triple Line Receiver designed for applications requiring digital information to be transmitted over long lengths of coaxial cable, strip line, or twisted pair transmission lines. The Receiver's high impedance input structure ($\approx 30k\Omega$) presents a minimal load to the driver circuit and allows the transmission line to be terminated in its characteristic impedance to minimize line reflections.

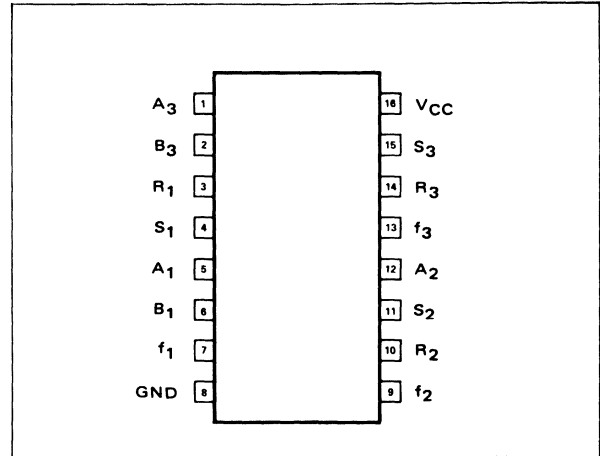
The built-in hysteresis characteristic of the 8T14 also makes it ideal for such applications as Schmitt triggers, one-shots and oscillators.

FEATURES

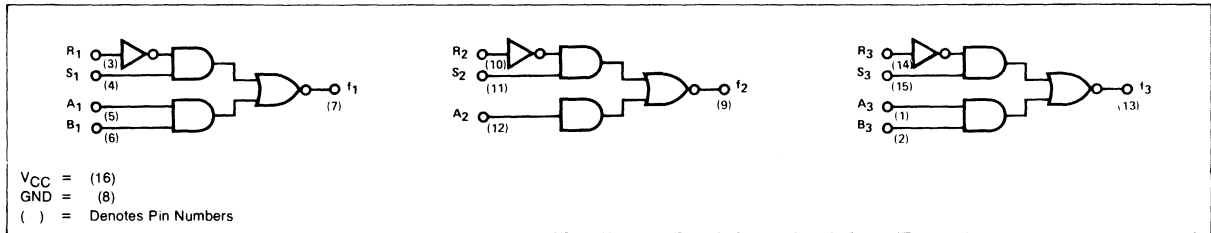
- BUILT-IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: $t_{on} = t_{off} = 20ns$ (Typical)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5 VOLT LOGIC SUPPLY

* Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.5 volts typically and 0.3 volts minimum over the operating temperature range.

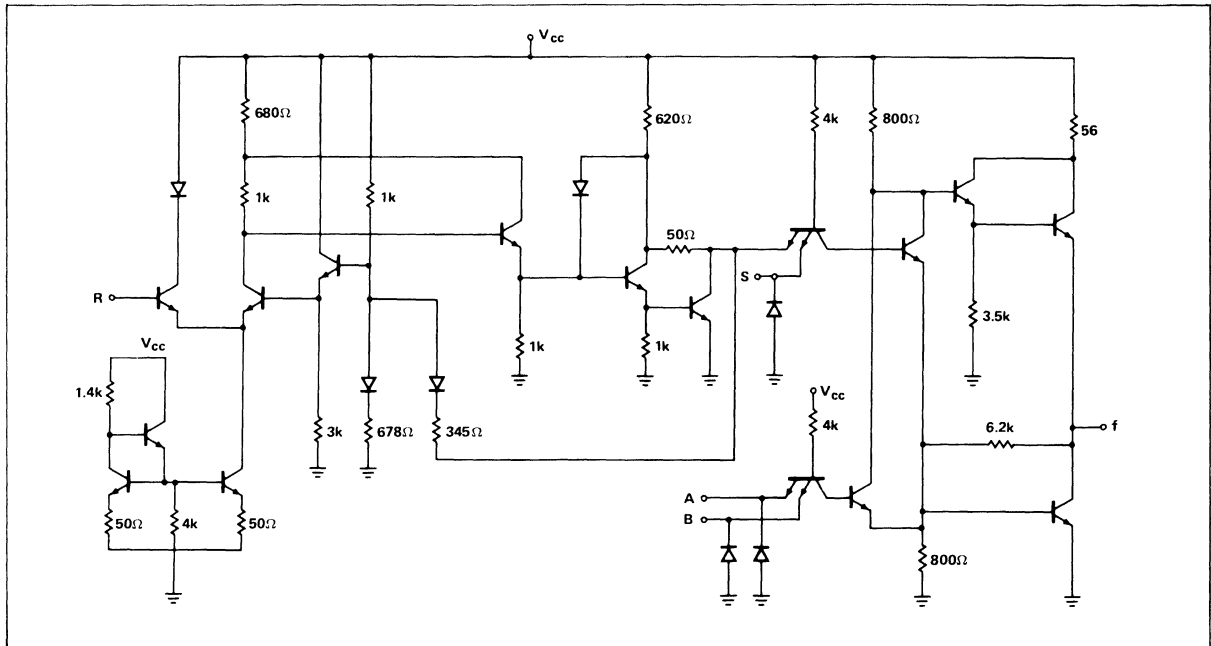
PIN CONFIGURATION



LOGIC DIAGRAMS



SCHEMATIC DIAGRAM



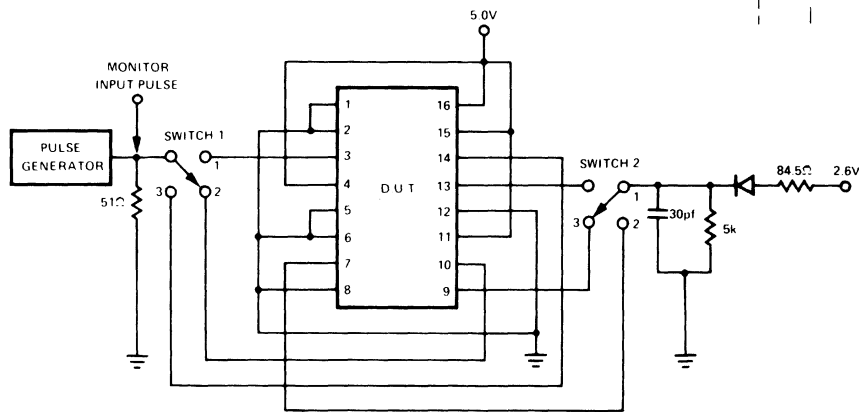
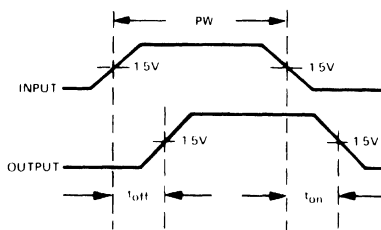
$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS			UNITS
	MIN.	TYP.	MAX.	
t_{on} , Turn-On Delay		20	30	ns
t_{off} , Turn-Off Delay		20	30	ns

AC TEST CIRCUIT AND WAVEFORMS

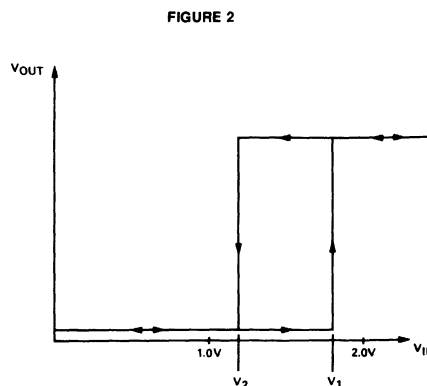
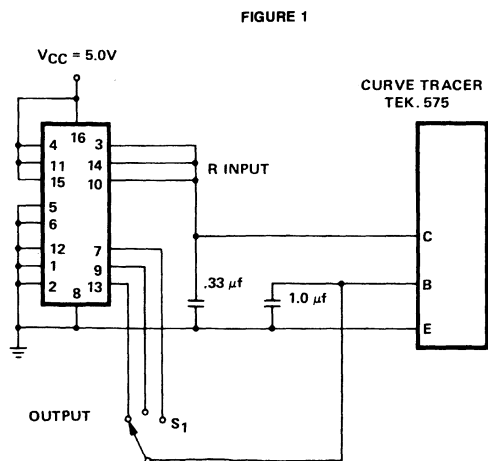
3 Receivers in the package.
Test each Receiver using switch positions as shown in Table 1.

Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3



Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
 $t_r = t_f = 5nS$ (10% to 90%)

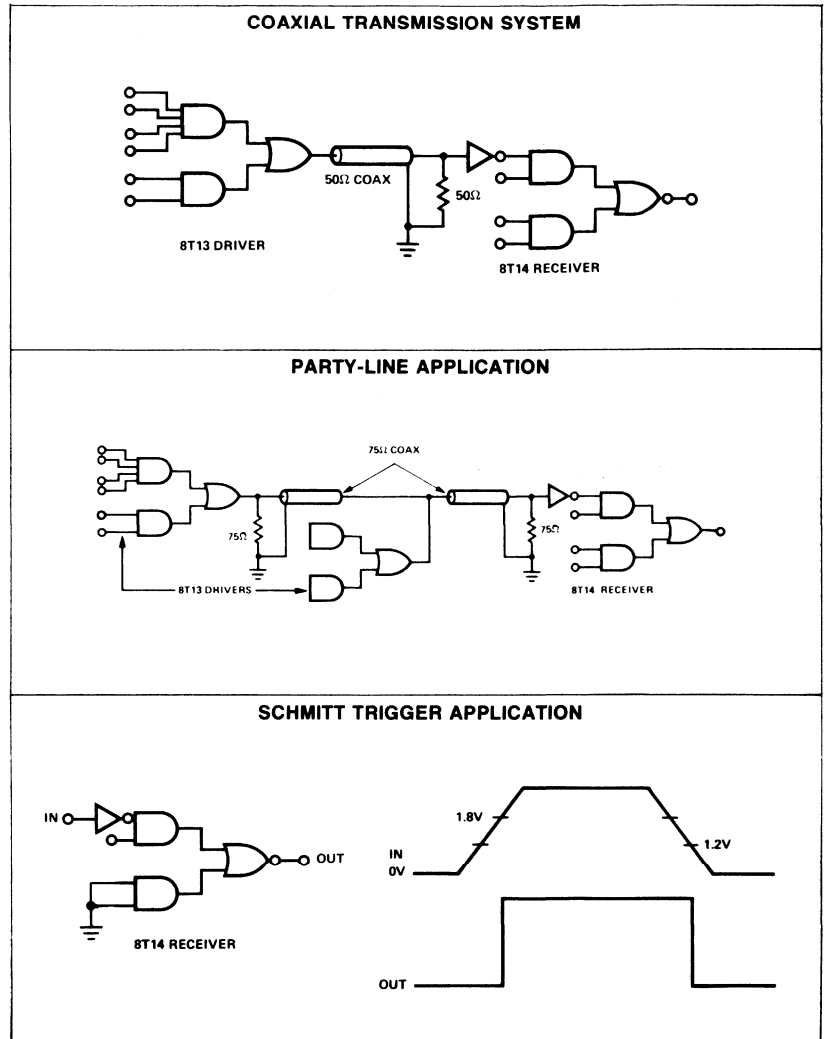
HYSTERESIS TEST CIRCUIT



Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

- V_1 and V_2 must be between 0.8V minimum and 2.0V max.
- Hysteresis = $V_1 - V_2 \geq 0.3V$.

TYPICAL APPLICATIONS

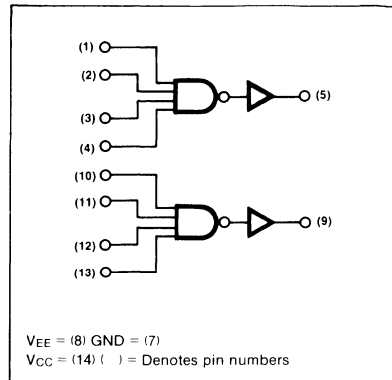


DESCRIPTION

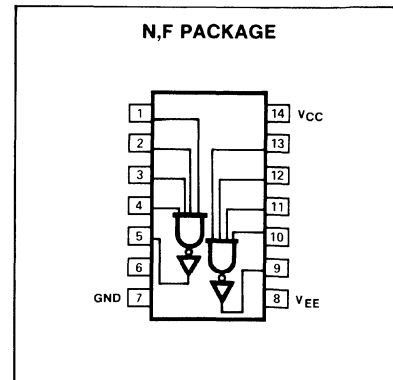
The 8T15 Dual Communications Line Driver provides line driving capability for data transmission between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, Mil std-188B and CCITT V24.

This dual 4-input NAND driver will accept standard TTL logic level inputs and will drive interface lines with nominal data levels of +6V and -6V. Output slew rate may be adjusted by attaching an external capacitor from the output terminal to ground. The outputs are protected against damage caused by accidental shorting to as high as ±25V.

LOGIC DIAGRAM



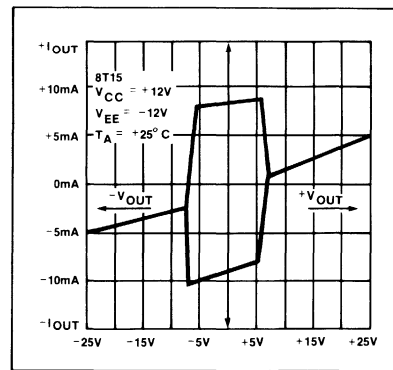
PIN CONFIGURATION



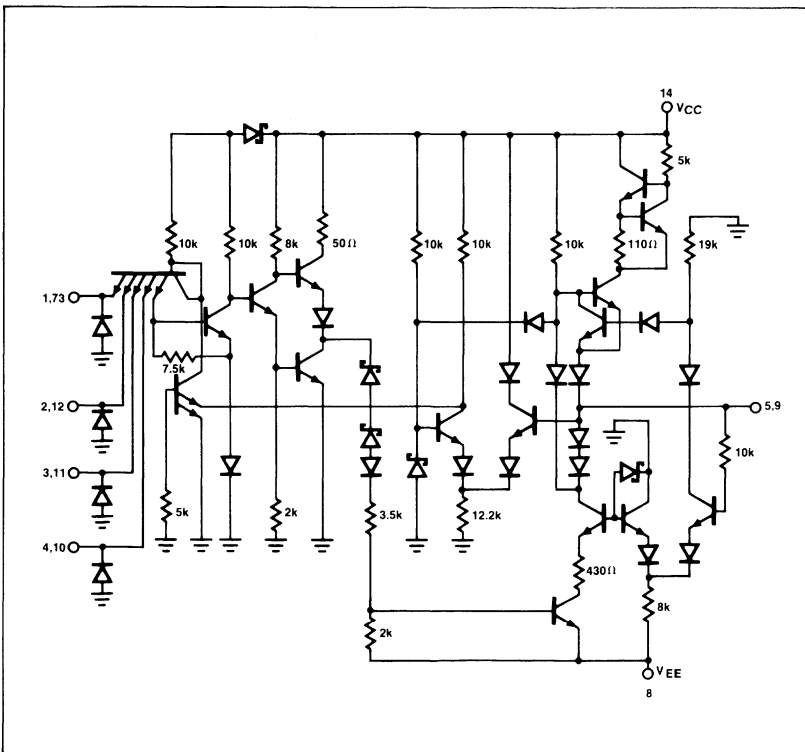
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	Power supply voltage	V
V _{IN}	Input voltage	+5.5 V
V _{OUT}	Output voltage	±25 V
V _{EE}		-15 V
T _{STG}	Storage temperature	-65 to +150 °C
T _A	Operating temperature	0 to +75 °C

TYPICAL PERFORMANCE CHARACTERISTICS



SCHEMATIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8T15			UNIT	
		Min	Typ	Max		
V_{IL} Input voltage Low	$V_{CC} = \text{MIN}, I_{IN} = -12\text{mA}$	2.0		0.8	V	
V_{IH} Input voltage High						V
V_{IC} Input voltage Clamp						V
V_{OL} Output voltage Low	$V_{CC} = \text{MIN}, V_{IN} = 2.0\text{V}, I_{OL} = 4.0\text{mA}$	-5.0	-6.0	-7.0	V	
V_{OH} Output voltage High				$V_{CC} = \text{MIN}, V_{IN} = 0.8\text{V}, I_{OH} = -4.0\text{mA}$	5.0	6.0
I_{IL} Input current Low	$V_{CC} = \text{MAX}, V_{IN} = 4.5\text{V}$	-0.1	-0.8	-1.6	mA	
I_{IH} Input current High				$V_{CC} = \text{MAX}, V_{IN} = 4.5\text{V}$		
I_{OS} Short circuit output current	$V_{CC} = 12.6\text{V}, V_{IN} = 0\text{V}, V_{CC} = -12.6\text{V}$			-25	mA	
				$V_{OUT} = -25\text{V}$		
				$V_{OUT} = 25\text{V}$		

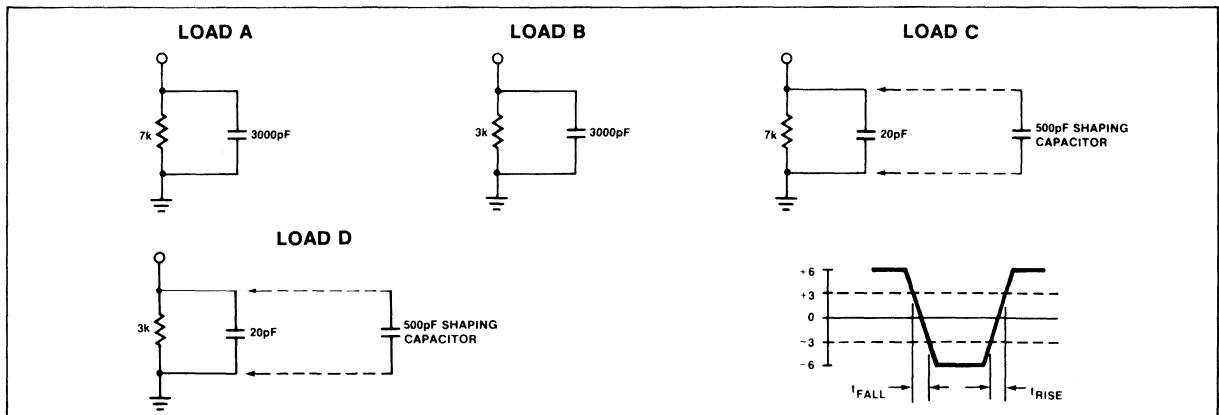
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 12.0\text{V}, V_{EE} = -12.0\text{V}$

PARAMETER	TO	8T15			UNIT
		Min	Typ	Max	
Output rise time ¹	Load A			4	ns
Output fall time ¹	Load C	200			ns
	Load B			4	ns
Current ²	Load D	200			ns
	Positive supply			16	mA
Negative supply				28	mA

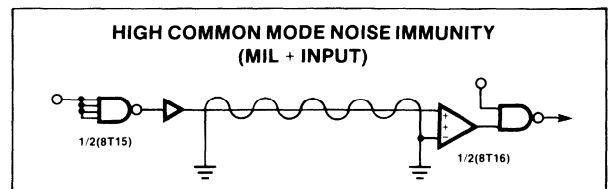
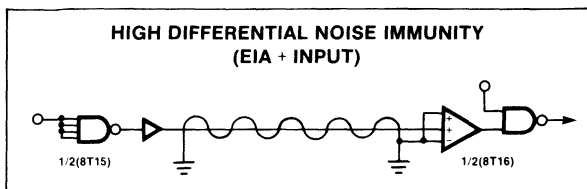
NOTES

- Rise and fall times are measured between the +3V and -3V points on the output waveform.
- $V_{CC} = 12.6\text{V}, V_{EE} = -12.6\text{V}$.

AC TEST FIGURES & WAVEFORMS



TYPICAL APPLICATIONS



DESCRIPTION

The 8T16 Dual Communications Line Receiver provides receiving capability for data lines between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL-STD-188B and CCITT V24 and operates from a single 5 volt power supply.

The receivers accept single (EIA) or double ended (MIL) inputs and are provided with an output strobing control. Both EIA and MIL input standards are accommodated.

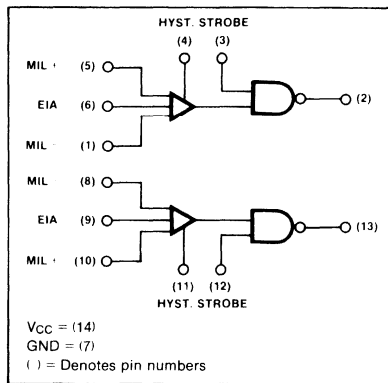
When using the EIA input terminal (with the Hysteresis terminal open), input voltage threshold levels are typically +2V and -2V with a guaranteed minimum Hysteresis of 2.4V. By grounding the "Hysteresis" terminal, the EIA input voltage threshold levels may be shifted to typically +1.0V and +2.1V with a minimum guaranteed Hysteresis of 0.75V. (Note that when using the EIA inputs, the MIL inputs—both positive and negative—must be grounded.)

The MIL input voltage threshold levels are typically +0.6V and -0.6V with a minimum guaranteed Hysteresis of 0.7V. A MIL negative terminal is provided on each receiver per specification MIL-STD-188B to provide for common mode noise rejection.

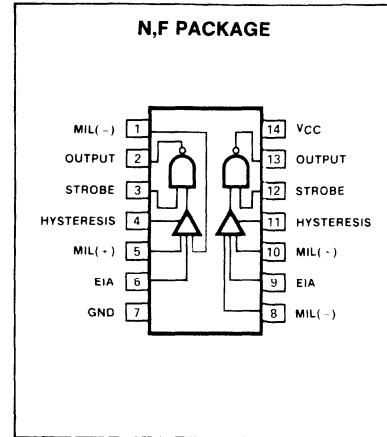
Each receiver includes a strobe input so that:

- a. A "1" on the strobe input allows data transfer.
- b. A "0" on the strobe input holds the output high.

LOGIC DIAGRAM



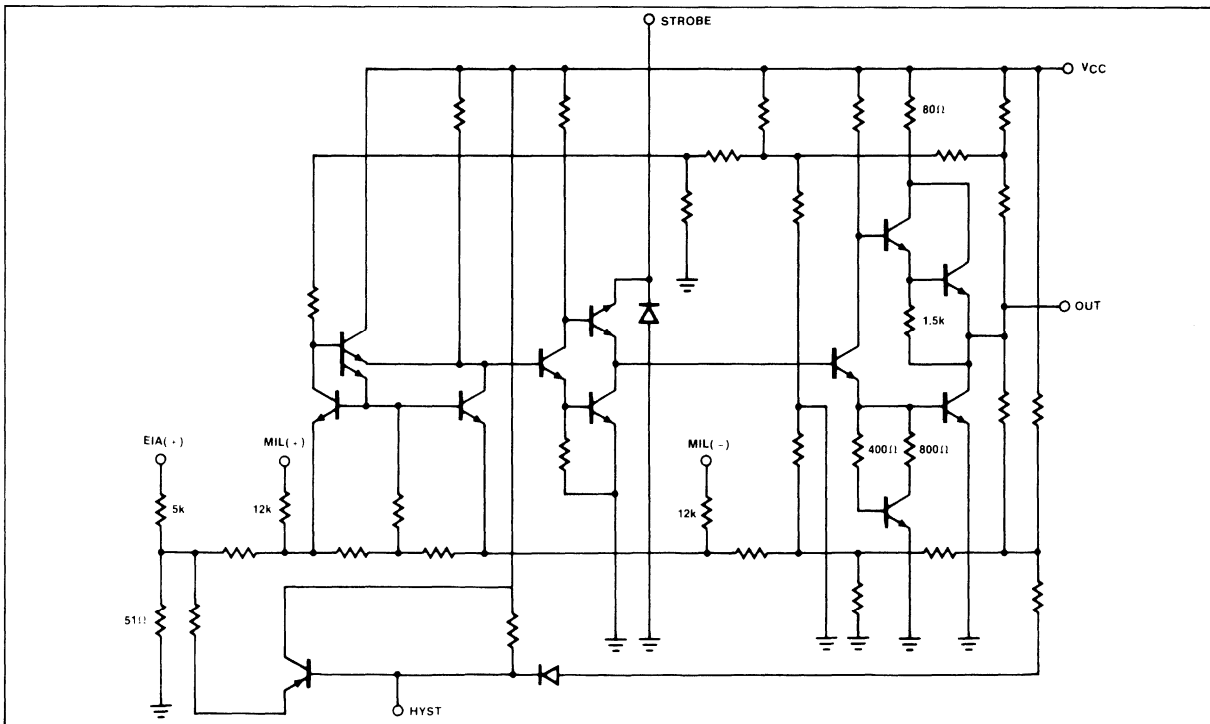
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	+7.0	V
V _{IN}	±25	V
T _{STG}	-65 to +175	°C
T _A	0 to +75	°C

SCHEMATIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

PARAMETER	TO	FROM	TEST CONDITIONS	8T16			UNIT
				Min	Typ	Max	
V _{OH} Output voltage (EIA) Hysteresis open ^{8,12}	Outputs -800μA	EIA, MIL(+), MIL(-), STROBE	EIA = 3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V	2.6	3.5		V
Hysteresis open	Outputs -800μA	EIA, MIL(+), MIL(-), STROBE	EIA = +1.2V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V	2.8	3.5		V
Hysteresis grounded ^{8,10}	Outputs -800μA	EIA, MIL(+), MIL(-), HYS, STROBE	EIA = +0.3V, MIL(+) = 0V, MIL(-) = HYS = 0V, STROBE = 2.0V	2.6	3.5		V
V _{OH} Output voltage (MIL) ^{8,11}	Outputs -800μA	MIL(+), MIL(-), STROBE	MIL(+) = -0.1mA, MIL(-) = 0V, STROBE = 2.0V	2.6	3.5		V
Output voltage (MIL) ^{8,11}	Outputs -800μA	MIL(+), MIL(-), STROBE	MIL(+) = -0.9V, MIL(-) = 0V STROBE = 2.0V	2.6	3.5		V
Output voltage (MIL) ^{8,13}	Outputs -800μA	MIL(+), MIL(-), STROBE	MIL(+) = +0.35V, MIL(-) = 0V, STROBE = 2.0V	2.8	3.5		V
V _{OH} Output voltage (STROBE) ⁸	Outputs -800μA	EIA, MIL(+), MIL(-), STROBE	EIA = +3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 0.8V	2.6	3.5		V
V _{OL} Output voltage (EIA)							
Hysteresis open ^{9,12}	Outputs 9.6mA	EIA, MIL(+), MIL(-), STROBE	EIA = +3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 0.8V			0.4	V
Hysteresis open ^{9,10}	Outputs 9.6mA	EIA, MIL(+), MIL(-), STROBE	EIA = -1.2V, MIL(+) = 0V MIL(-) = 0V, STROBE = 2.0V		0.2	0.4	V
Hysteresis grounded ^{9,12}	Outputs 9.6mA	EIA, MIL(+), MIL(-), HYS, STROBE	EIA = +3.0V, MIL(+) = 0V, MIL(-) = 0V, HYS = 0V, STROBE = 2.0V			0.4	V
Output voltage (MIL) ^{9,13}	Outputs 9.6mA	MIL(+), MIL(-), STROBE	MIL(+) = +0.1mA, MIL(-) = 0V, STROBE = 2.0V			0.4	V
Output voltage (MIL)	Outputs 9.6mA	MIL(+), MIL(-), STROBE	MIL(+) = +0.9V, MIL(-) = 0V, STROBE = 2.0V			0.4	V
Output voltage (MIL) ^{9,11}	Outputs 9.6mA	MIL(+), MIL(-), STROBE	MIL(+) = -0.35V, MIL(-) = 0V, STROBE = 2.0V		0.2	0.4	V
Input resistance (EIA)		EIA, MIL(+), MIL(-)	EIA = ±25V, MIL(+) = 0V, MIL(-) = 0V	3	5	7	kΩ
Input resistance (MIL)		EIA, MIL(+), MIL(-)	EIA = 0V, MIL(+) = ±25V, MIL(-) = 0V	7.5	11.4		kΩ
Power consumption (per receiver) ¹⁷		EIA, MIL(+), MIL(-)	EIA = 3.0V, MIL(+) = 0V, MIL(-) = 0V		44	75	mW
Output short circuit current ^{16,17}	Outputs 0V	EIA, MIL(+), MIL(-)	EIA = -3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 5.0V	-10		-70	mA
Propagation delay ^{14,15}		STROBE	STROBE = 5.0V		100	150	ns
Signal switching acceptance ¹⁵		STROBE	STROBE = 5.0V	20			kHz

NOTES

- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current is defined as into the terminal referenced.
- Positive logic definition:
"UP Level = H, "DOWN" Level = L.
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings.
- Manufacturer reserves the right to make design and process changes and improvements.
- This test guarantees operation free of latch-up over the specified input voltage range.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC}.
- Previous EIA input: +3V (See hysteresis curve).
- Previous MIL input: +0.9V (See hysteresis curve).
- Previous EIA input: -3.0V (See hysteresis curve).
- Previous MIL input: -0.9V (See hysteresis curve).
- Reference AC Test Figures.
- This test guarantees transfer of signals of up to 20kHz. Connect 1000pF between the output terminal and ground.
- Each receiver to be tested separately.
- V_{CC} = 5.25V.

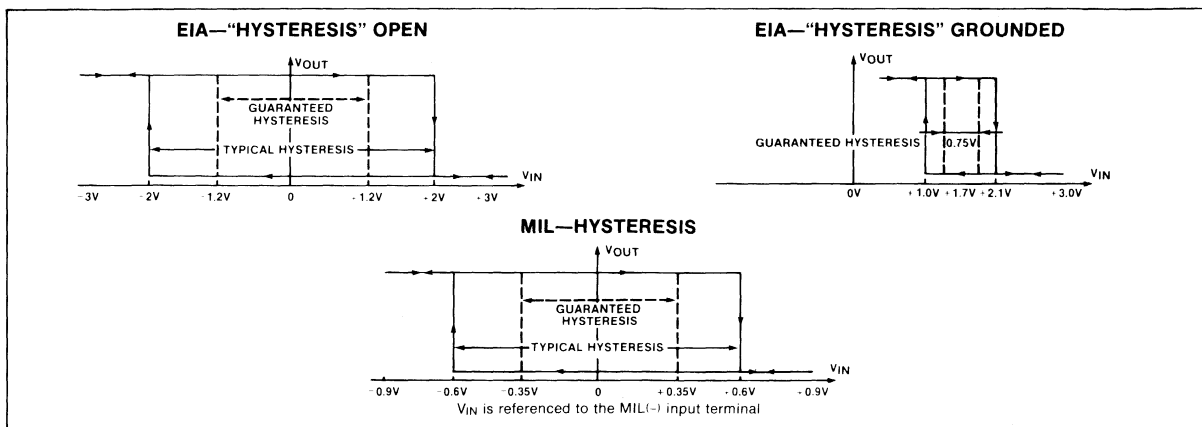
AC ELECTRICAL CHARACTERISTICS

PARAMETER	FROM	TEST CONDITIONS	8T16			UNIT
			Min	Typ	Max	
Input resistance EIA	EIA, MIL(+), MIL(-)	EIA = $\pm 25V$, MIL(+) = 0.0V, MIL(-) = 0.0V	3	5	7	k Ω
MIL	EIA, MIL(+), MIL(-)	EIA = 0.0V, MIL(+) = $\pm 25V$, MIL(-) = 0.0V	7.5	11.4		k Ω
Propagation delay	Strobe	Strobe = 5.00V		100	150	ns
Signal switching acceptance	Strobe	Strobe = 5.00V	20			kHz

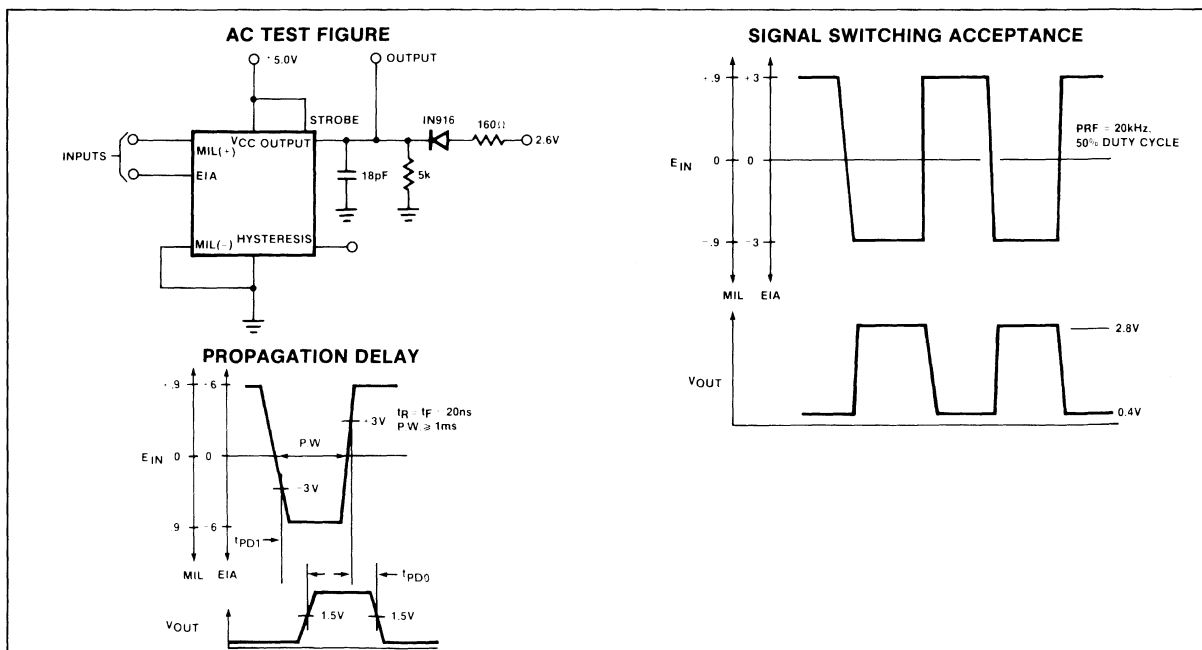
NOTE

This test guarantees transfer of signals of up to 20kHz. Correct 1000pF between the output terminal and ground.

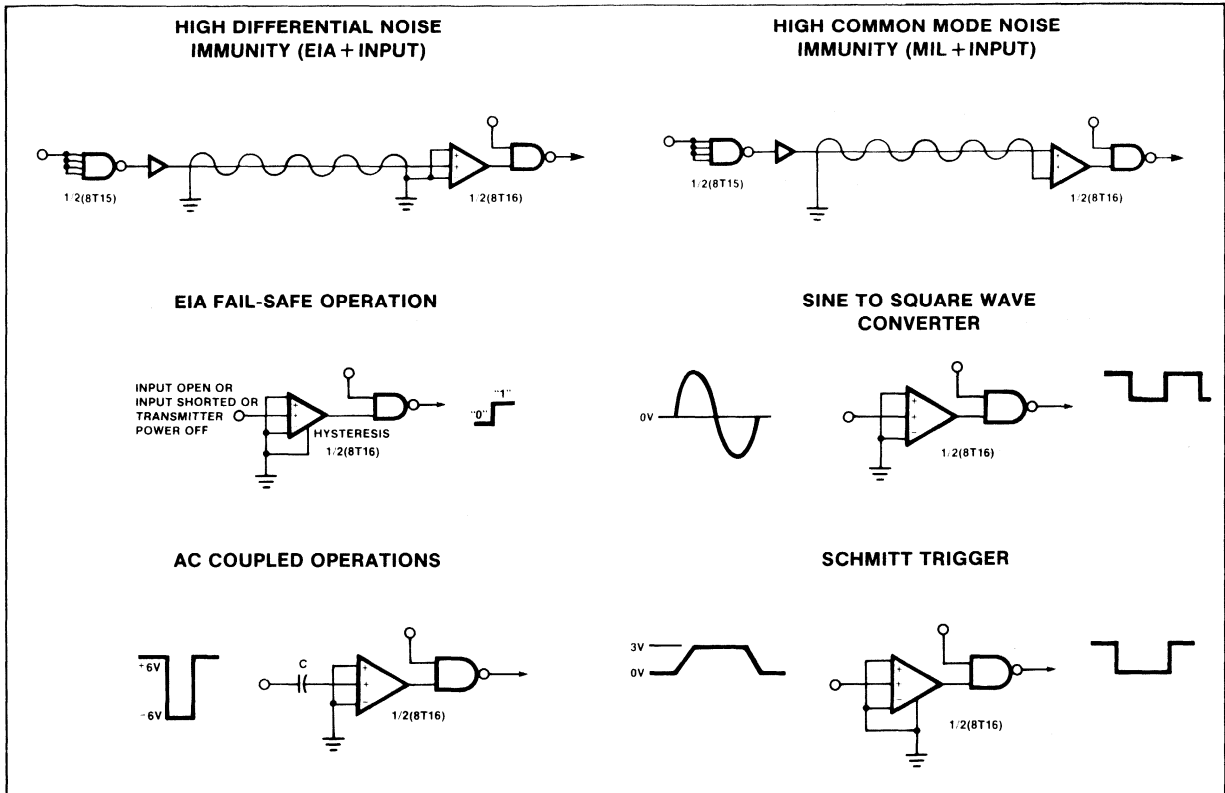
HYSTERESIS CURVES



AC TEST FIGURE AND WAVEFORMS



TYPICAL APPLICATIONS



DESCRIPTION

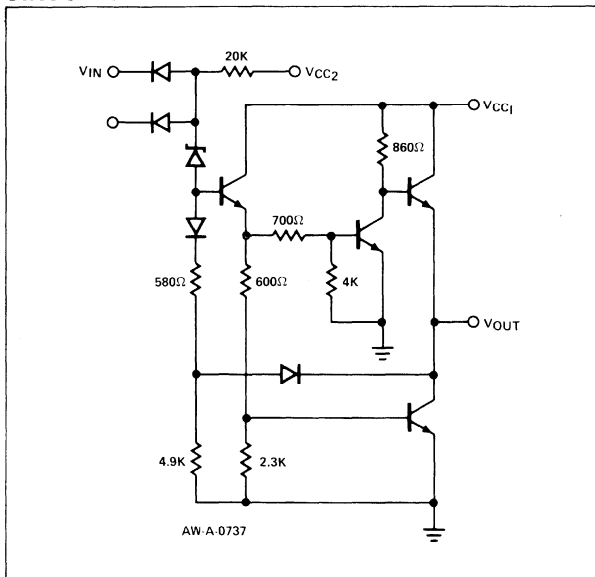
The 8T18 is a Dual 2-Input NAND Interface Gate. It is typically used as a high to low voltage translator which provides translation from up to 30-volt logic levels to standard logic levels of 5 volts.

The basic gate operates from two power supplies. The input structure functions from a high voltage supply V_{CC2} , between 20V and 30V and the second stage transistors and output structure operate from a standard 5V power supply, V_{CC1} .

The high "0" level input threshold (guaranteed at 6.5V) makes the 8T18 very attractive for noisy systems applications such as industrial interfaces.

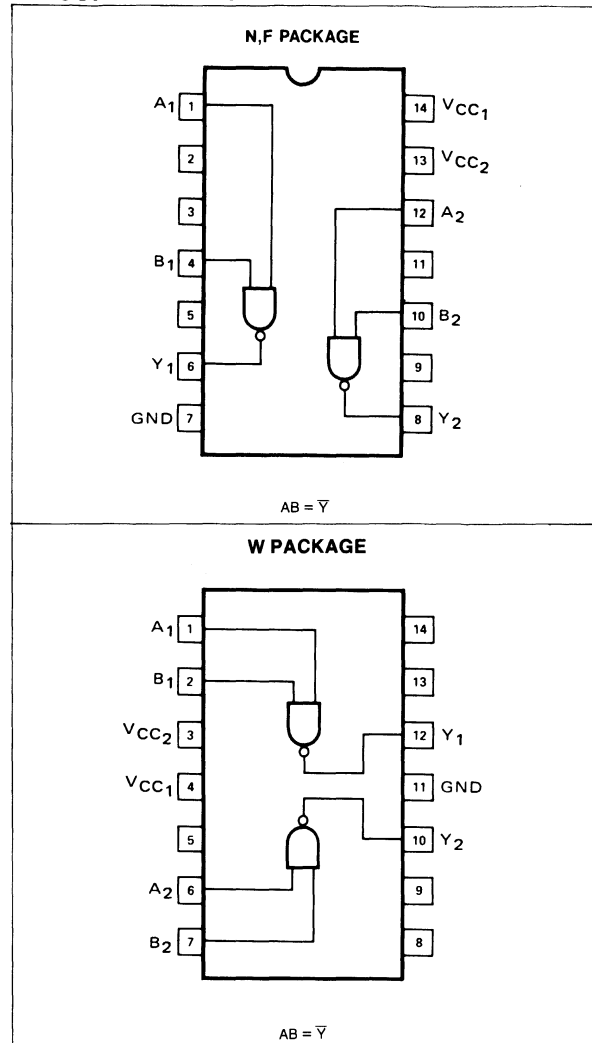
The output structure features active pull-up and pull-down, providing a low impedance driving source in both "1" and "0" output states. This configuration is particularly suited for driving the high capacitance loads encountered in high fan-out and line driving applications.

CIRCUIT SCHEMATIC

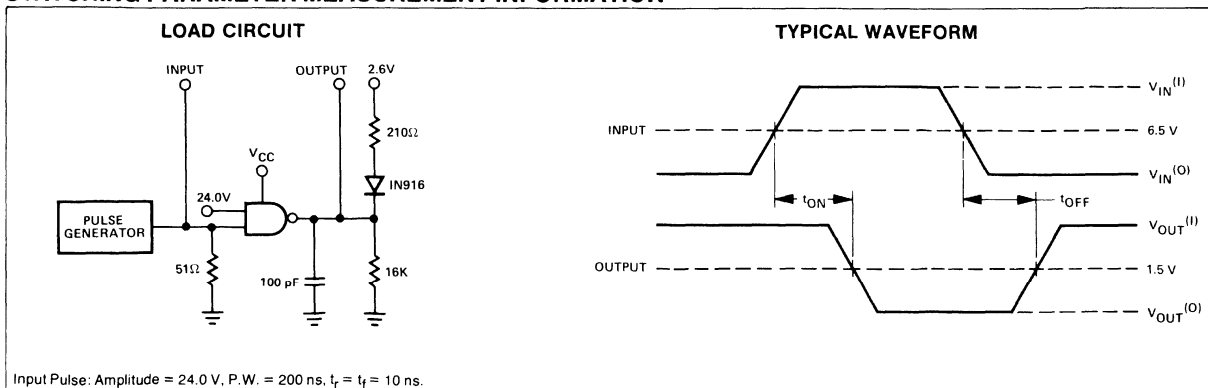


NOTE: 1/2 of unit shown. Component values are typical.

PIN CONFIGURATION



SWITCHING PARAMETER MEASUREMENT INFORMATION



Input Pulse: Amplitude = 24.0 V, P.W. = 200 ns, $t_r = t_f = 10$ ns.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC1} = 5.0\text{V}$, $V_{CC2} = 24.0\text{V}$

PARAMETER		TEST CONDITIONS ⁹	LIMITS			UNIT
			MIN	TYP	MAX	
t_{on}	Turn-On Delay	$R_L = 210\Omega$		27	40	ns
t_{off}	Turn-Off Delay	$C_L = 100\text{ pF}$		18	35	ns

DESCRIPTION

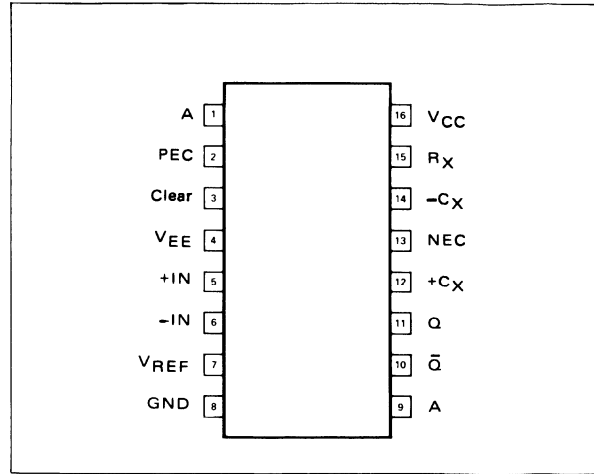
The Bidirectional One Shot is intended for applications where high speed low level signal processing is required.

The 8T20 is a Monolithic Building Block, consisting of a high speed analog comparator, digital control circuitry, and a precision monostable multivibrator. The differential input threshold voltage is between $\pm 4mV$ with respect to the input reference level which may range from $-3.2V$ to $+4.2V$. For input frequencies up to 8MHz, the device may be conditioned to act as a frequency doubler since it can trigger on both positive and negative input transitions.

Timing pins permit using this device in a variety of applications where external control over pulse width is desirable. Pulse width (t_w) is defined by the relationship $t_w = C_X R_X \text{Loge}2$. Pulse width stability is internally compensated and virtually independent of temperature and V_{CC} variations, thus only limited by the accuracy of external timing components.

An internal resistive divider is available on the chip to provide a voltage of 1.4V (typ.). This output can be connected directly to either of the comparator inputs as a reference voltage when interfacing with TTL outputs.

PIN CONFIGURATION



FEATURES

- DIFFERENTIAL INPUT THRESHOLD = $\pm 4mV$
- PULSE POSITION ERROR = TYPICALLY $< 3ns$
- MAX. INPUT FREQUENCY = 8 MHz
- TRIGGERS ON POSITIVE AND/OR TRANSITIONS

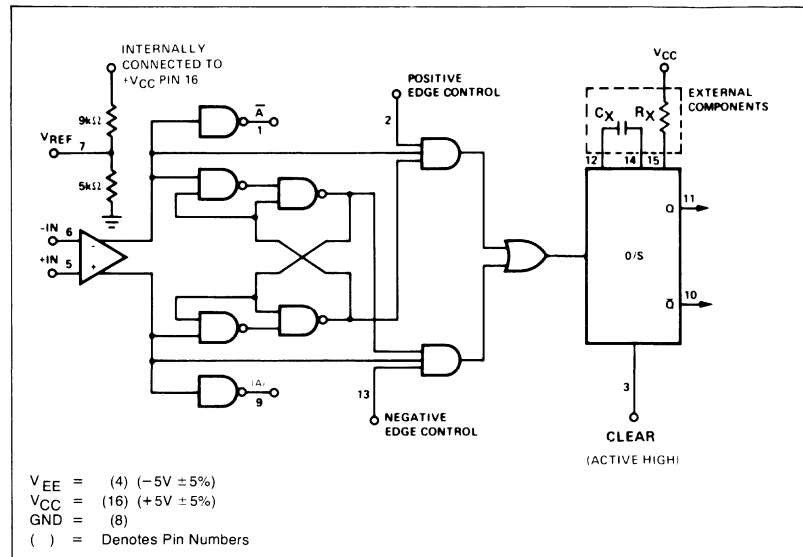
APPLICATIONS

- DISC, TAPE AND DRUM READERS
- DIGITAL COMMUNICATIONS RECEIVERS
- SIGNAL CONDITIONERS
- TRANSITION DETECTORS

ABSOLUTE MAX RATINGS

- Input Voltage
- V_{CC} : +7V
- V_{EE} : -7V
- MAX DIFF. INPUT VOLTAGE $\pm 5V$

LOGIC DIAGRAM



$T_A = 25^\circ C, V_{CC} = +5.00V, V_{EE} = -5.00V$

CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS
	MIN.	TYP.	MAX.		
Output Frequency	16			MHz	Fig. 1, $f_{in} = 8 \text{ MHz}$
Propagation Delay (t_{on}, t_{off})				ns	Fig. 2
Input to Q, Q		30	50	ns	Fig. 4
Input to A, A		30	50	ns	
Clear to Q, Q		20	30	ns	
Reference Voltage (V_{REF})	0.8	1.4	2.0	V	Pin 7 tied to Pin 6
Output Pulse Width, Fig. 1	10		40	ns	$R_x = 10K, C_x = \text{Open}$
Output Pulse Width, Fig. 3	600		800	ns	$R_x = 10K, C_x = 100pf$

AC TEST CIRCUITS

MINIMUM OUTPUT PULSE WIDTH ($C_X = \text{OPEN}$)

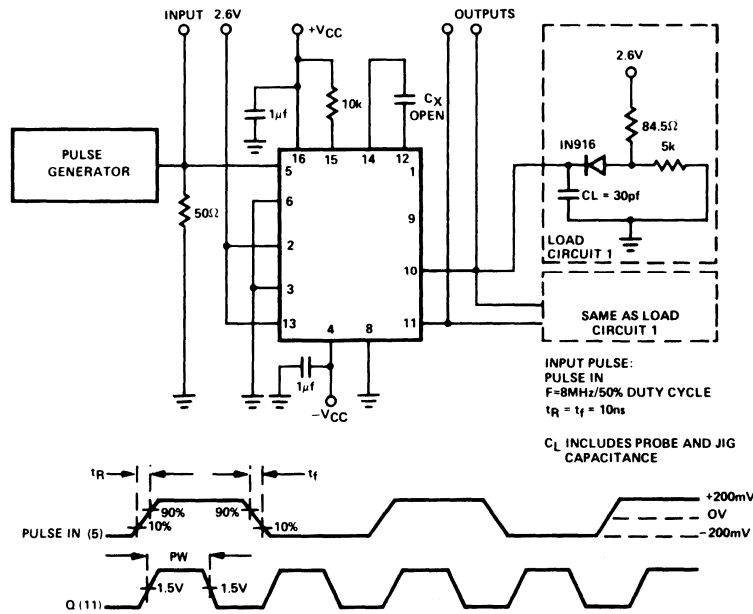


FIGURE 1

PROPAGATION DELAY (INPUT TO Q, \bar{Q} OUTPUTS)

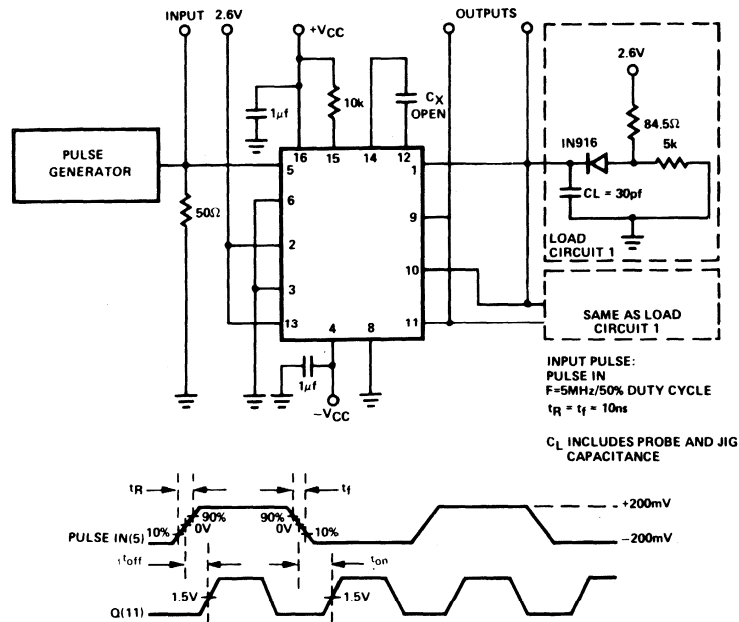


FIGURE 2

AC TEST CIRCUITS (Cont'd)

PROPAGATION DELAY (CLEAR TO Q, \bar{Q})

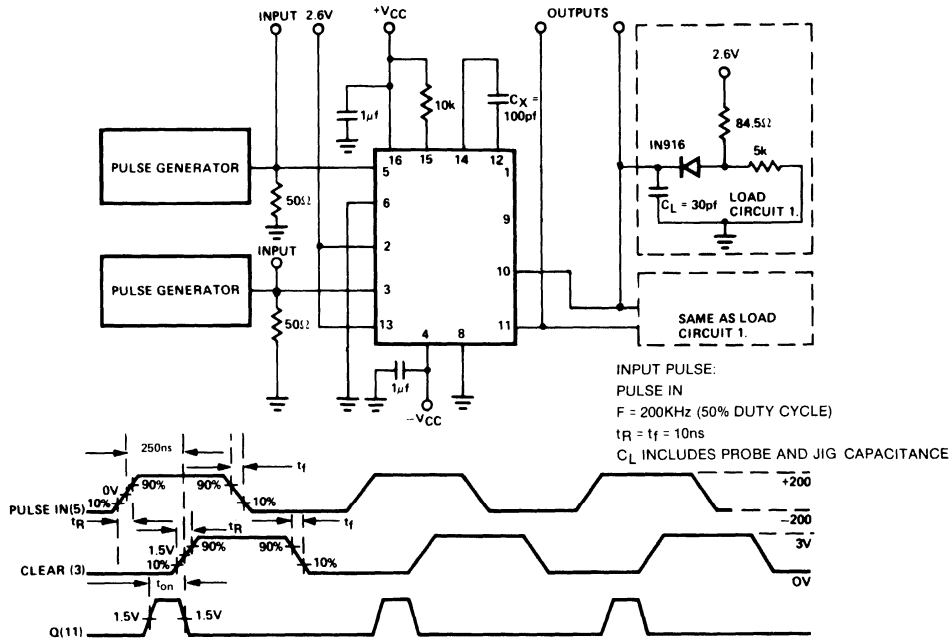


FIGURE 3

PROPAGATION DELAY (INPUT TO A, \bar{A} OUTPUTS)

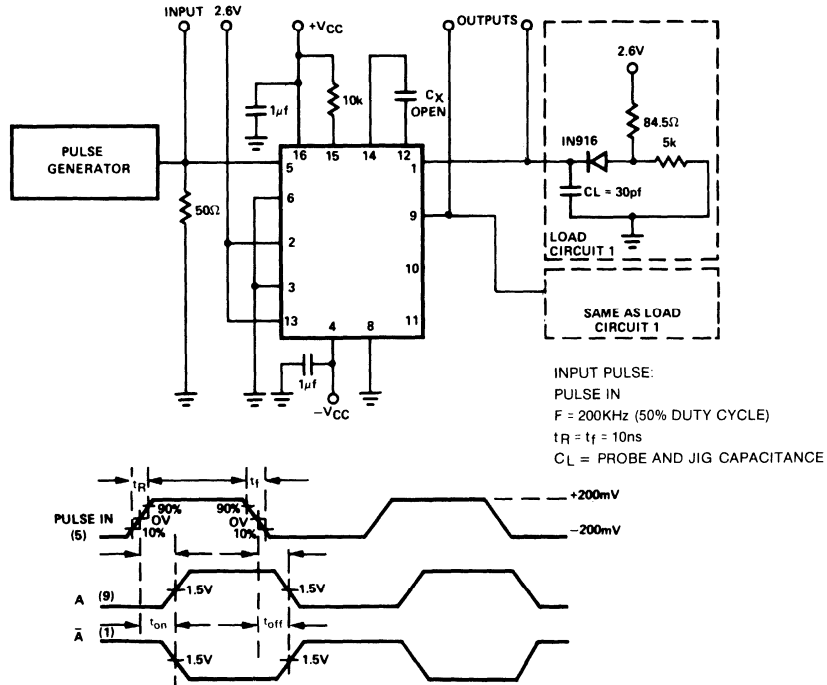
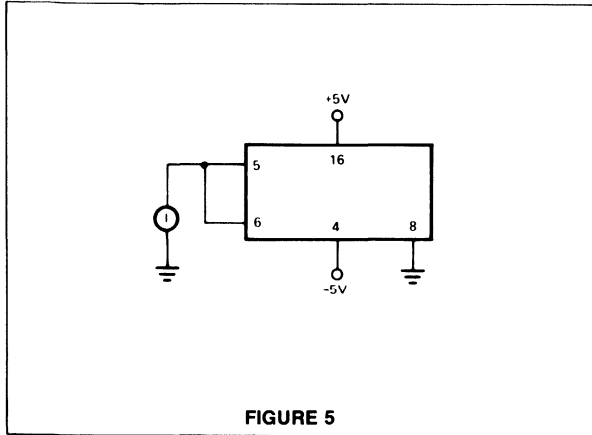
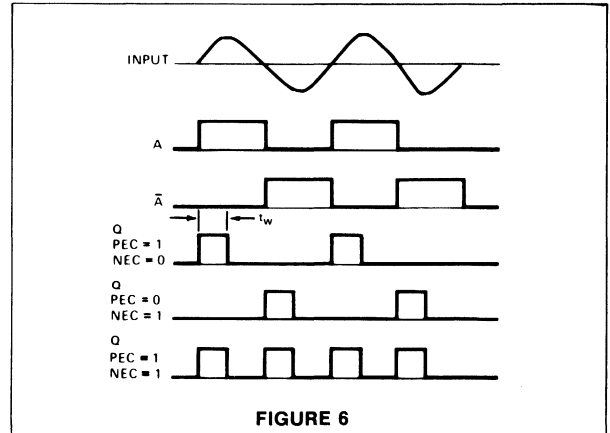


FIGURE 4

INPUT BIAS CURRENT TEST CIRCUIT



INPUT/OUTPUT WAVEFORMS



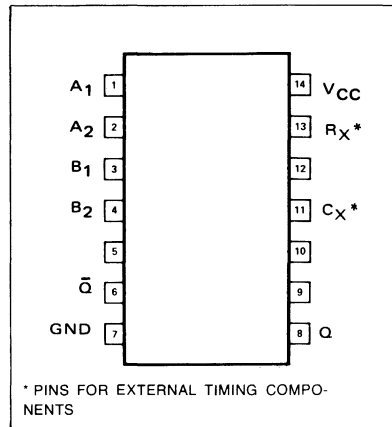
DESCRIPTION

The 8T22 is a direct pin-for-pin replacement for the 9601 retriggerable one-shot. Triggering can be performed on either the leading or falling edge of the input signal through selection of the proper input terminal.

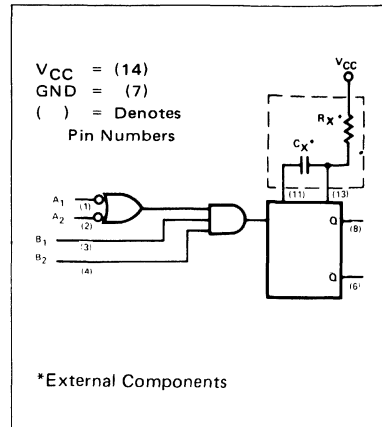
The inputs are level-sensitive making triggering independent of signal transition times. Output pulse width is determined by external timing components (R_X and C_X) with each trigger pulse initiating a complete new timing cycle.

For those applications where a dual retriggerable one-shot is required the Signetics 9602 should be considered.

PIN CONFIGURATION



LOGIC DIAGRAM



TRUTH TABLE

Pin Number			
1	2	3	4
H→L	H	H	H
H	H→L	H	H
L	X	L→H	H
X	L	L→H	H
L	X	H	L→H
X	L	H	L→H

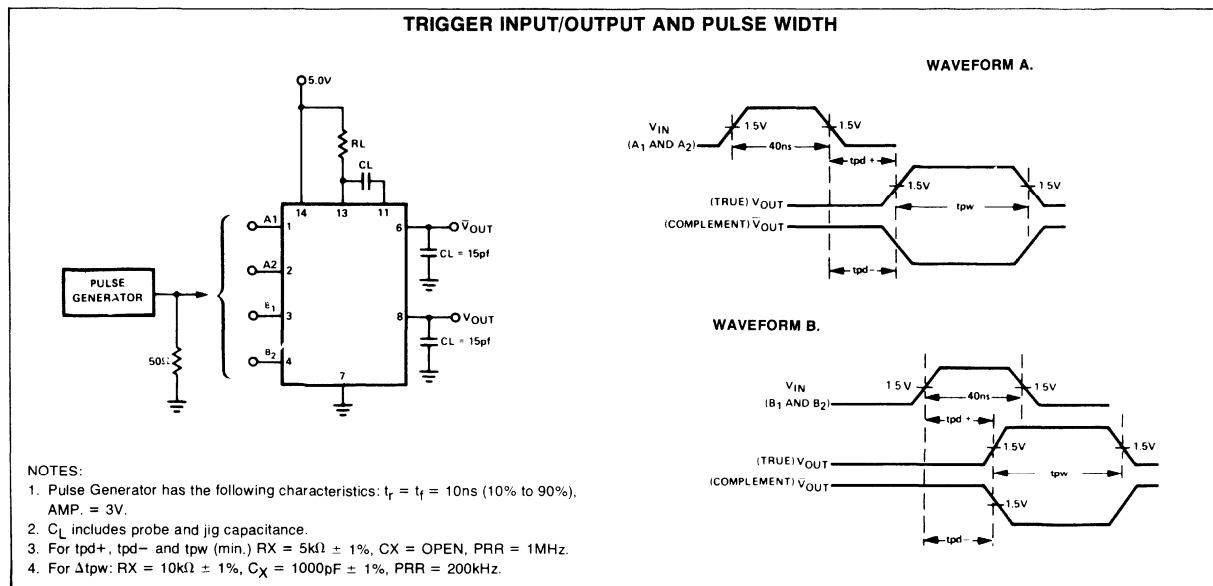
$T_A = 25^\circ C$ and $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Propagation Delay Negative Trigger Input to True Output (t_{pd+})	$R_X = 5.0k\Omega, C_X = 0$ $C_L = 15pF$		25	40	ns
Negative Trigger Input to False Output (t_{pd-})	$R_X = 5.0k\Omega, C_X = 0$ $C_L = 15pF$		25	40	ns
Min. True Output Pulse Width	$R_X = 5.0k\Omega, C_X = 0$ $C_L = 15pF$		45	65	ns
Pulse Width Variation	$R_X = 10k\Omega, C_X = 1000pF$	3.08	3.42	3.76	μs
Timing Resistor		5.0		50	$k\Omega$
CStray - Maximum allowable wiring capacitance	P13 to Ground			50	pF

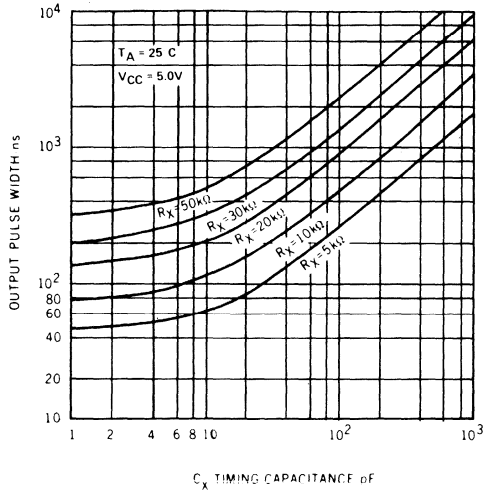
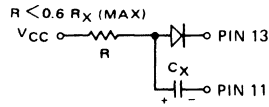
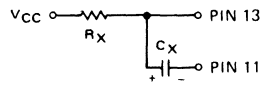
NOTES

1. Positive current is defined as into the pin referenced.
2. Unless otherwise noted, $10k\Omega$ resistor placed between Pin 13 and V_{CC} (R_X).

AC TEST FIGURE AND WAVEFORMS



OPERATION RULES



TYPICAL OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR C_X < 10³ pF IS SHOWN IN THE ABOVE GRAPH.

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 to 50 kΩ (0 to 75°).
3. C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. If electrolytic capacitors are to be used, the following configurations are recommended:
 - A. For use with low leakage electrolytic capacitors. The normal RC configuration can be used predicably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range, and Rule 3 above is satisfied.
 - B. Use with high inverse leakage current electrolytic capacitors. The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.

t ≈ 0.3 RC_X

The output pulse with (t) is defined as follows:

$$t = 0.32 R_X C_X \left[1 + \frac{0.7}{R_X} \right]$$

Where R_X is in kΩ, C_X is in pF, t is in ns; for C_X < 10³ pF.

DESCRIPTION

The 8T23 is a Dual Line Driver designed to meet all of the requirements of the IBM System/360, System/370 I/O interface specifications (IBM Specification GA 22-6974-0).

The low impedance emitter follower output will drive terminated lines such as coaxial cable or twisted pair. The output is protected against accidental shorting by an internal clamping network which turns on once the output voltage drops below approximately 1.5 volts. The uncommitted emitter output structure allows Dot-OR logic to be performed as in "Party-Line" operations.

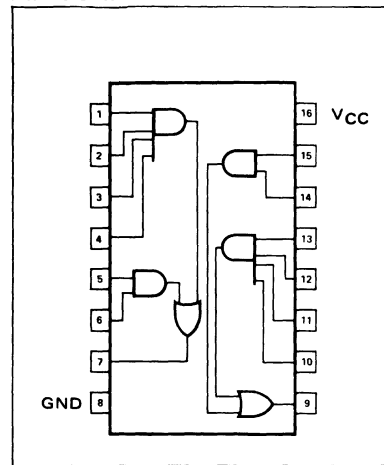
Multiple emitter inputs allow the 8T23 to interface with standard TTL or DTL systems and the circuit operates from a single +5 volt power supply.

Additional logic incorporated in the 8T23 Dual Line Driver can be used during the power-up and power-down sequence to ensure that no spurious noise is generated on the line.

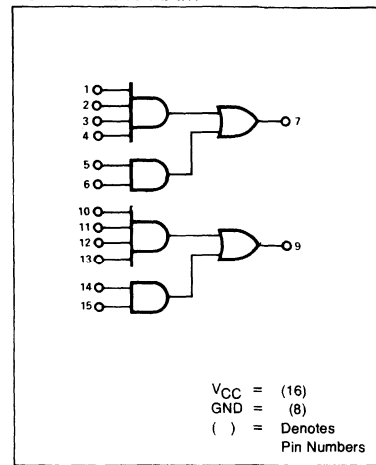
FEATURES

- IOUT = 59.3mA AT 3.11 VOLTS
- UNCOMMITTED EMITTER OUTPUT STRUCTURE
- FOR PARTY-LINE OPERATION
- SHORT-CIRCUIT PROTECTION
- SINGLE 5 VOLT POWER SUPPLY.
- AND-OR LOGIC CONFIGURATION

PIN CONFIGURATION



LOGIC DIAGRAM

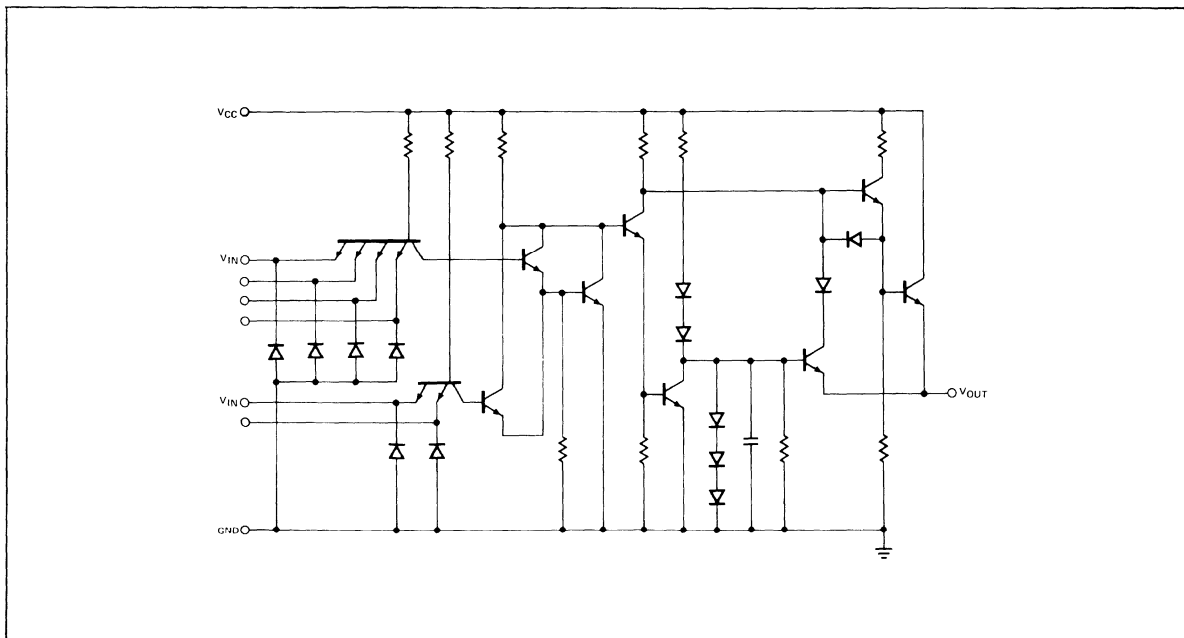


SWITCHING CHARACTERISTICS VCC = 5.0V, TA = 25° C^{1,2}

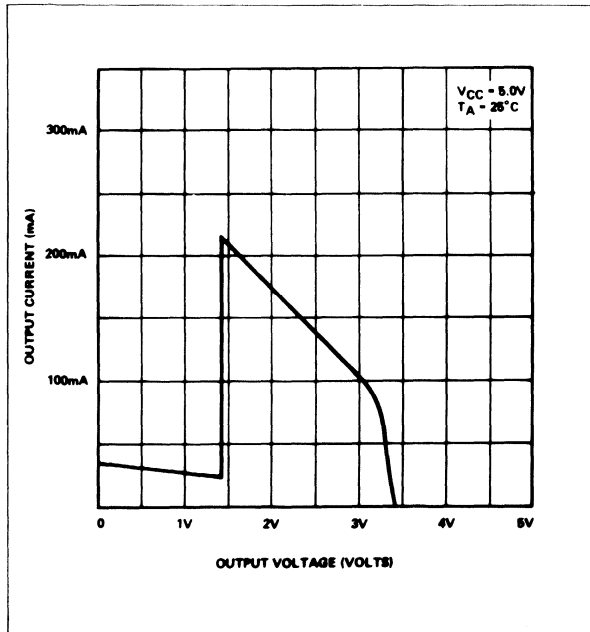
PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
t _{on} , Turn-On Delay		12	20	ns
		15	25	ns
t _{off} , Turn-Off Delay		12	20	ns
		20	35	ns

- NOTES:
1. RL = 50Ω to ground.
 2. Load is 50Ω in parallel with 100pF.
 3. Reference AC Test Circuit and Pulse Requirements

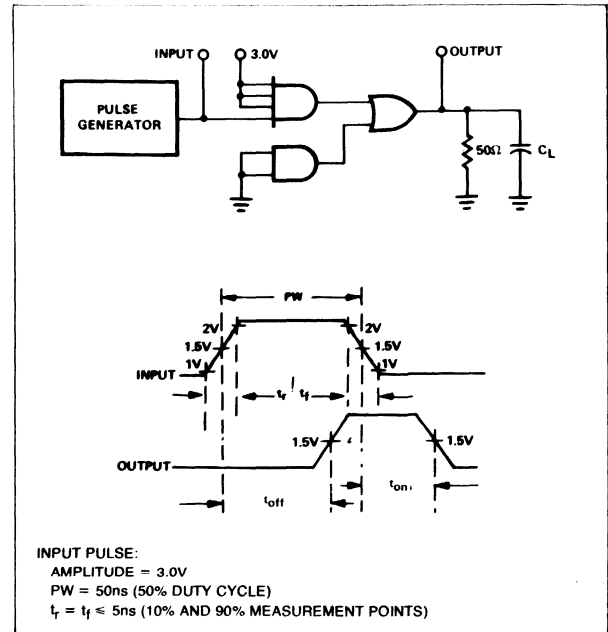
CIRCUIT SCHEMATIC



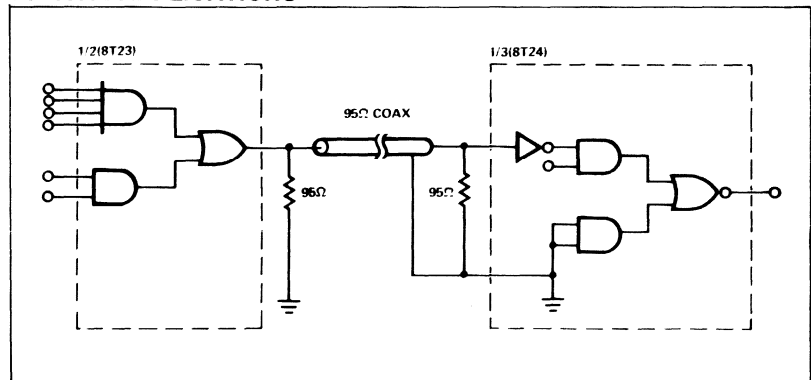
TYPICAL OUTPUT CHARACTERISTICS



AC TEST FIGURE AND WAVEFORMS



TYPICAL APPLICATIONS



DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System (360, System/370 I/O Interface Specification (IBM Specification GA 22-6974-0). Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of 0.70 volts or less is interpreted as a logical zero as is an open circuited input.

The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The 8T24 will also withstand an input of -0.15V with power on or off.

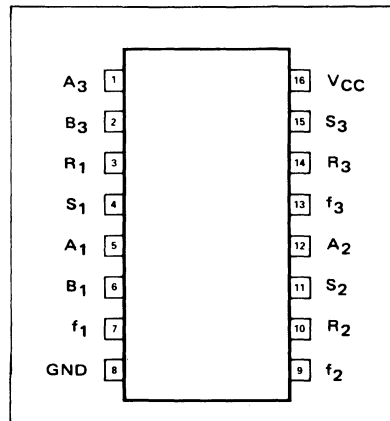
The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

FEATURES

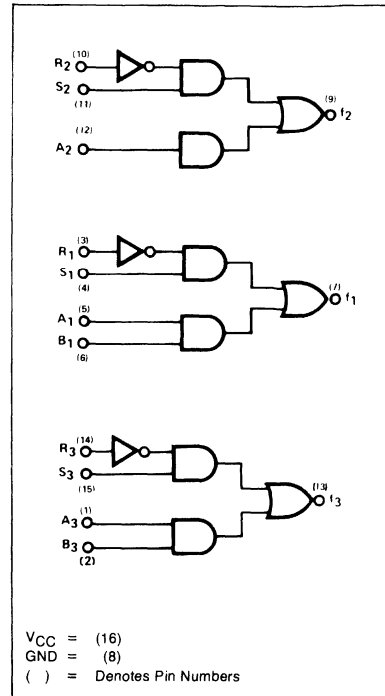
- BUILT-IN INPUT THRESHOLD HYSTERESIS*
- HIGH SPEED: TON = TOFF = 20ns (TYPICAL)
- EACH CHANNEL CAN BE STROBED INDEPENDENTLY
- FANOUT OF TEN (10) WITH STANDARD TTL INTEGRATED CIRCUITS
- INPUT GATING IS INCLUDED WITH EACH LINE RECEIVER FOR INCREASED APPLICATION FLEXIBILITY
- OPERATION FROM A SINGLE +5V POWER SUPPLY

* Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

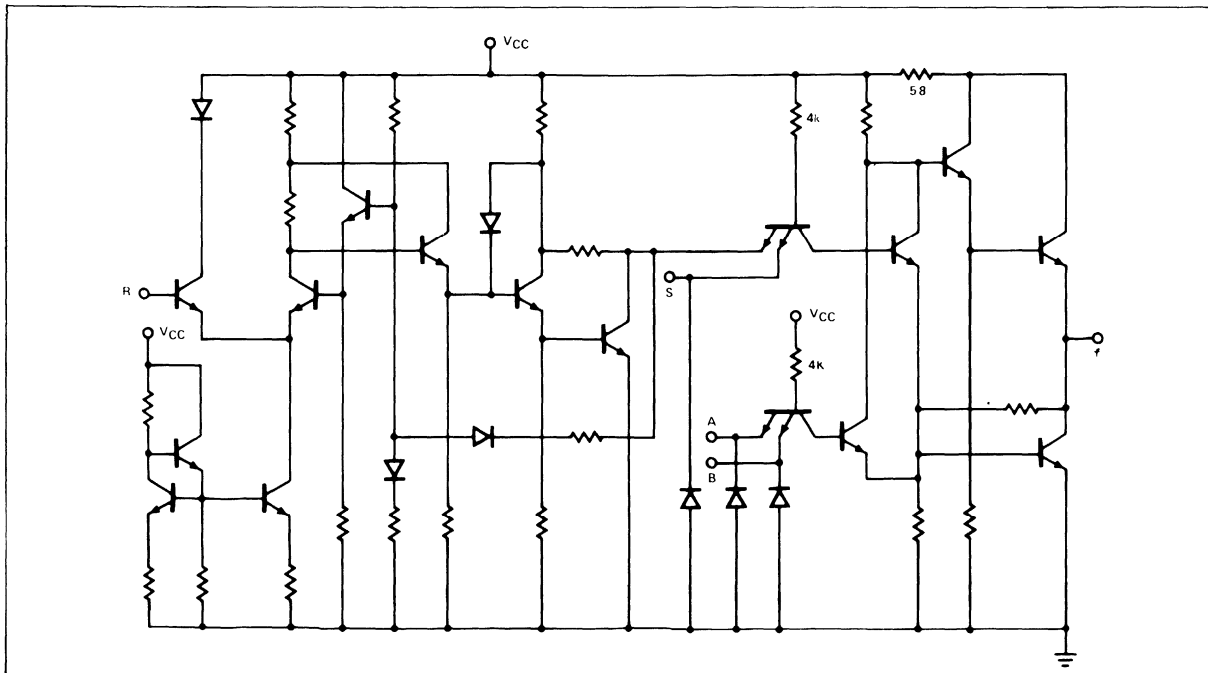
PIN CONFIGURATION



LOGICAL DIAGRAM WITH PIN LAYOUT



CIRCUIT SCHEMATIC



SWITCHING CHARACTERISTICS AT $V_{CC} = 5.0V$ AND $T_A = 25^\circ C$

1. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "0" to "1" state and the level at which the output begins to go from "1" to "0".

PARAMETER	TEST CONDITIONS				LIMITS			UNITS
	R	S	A	B	MIN	TYP	MAX	
t_{on} , Turn-On Delay						20	30	ns
t_{off} , Turn-Off Delay						20	30	ns
Hysteresis ¹		4.5V	0V	0V	0.2	0.4		V

AC TEST CIRCUIT AND WAVEFORMS

Input Pulse:
Amplitude = 2.6V
Pulse width = 200nS
(50% Duty Cycle)
 $t_r = t_f = 5nS$ (10% to 90%)

3 Receivers in the package.
Test each Receiver using switch positions as shown in Table 1.

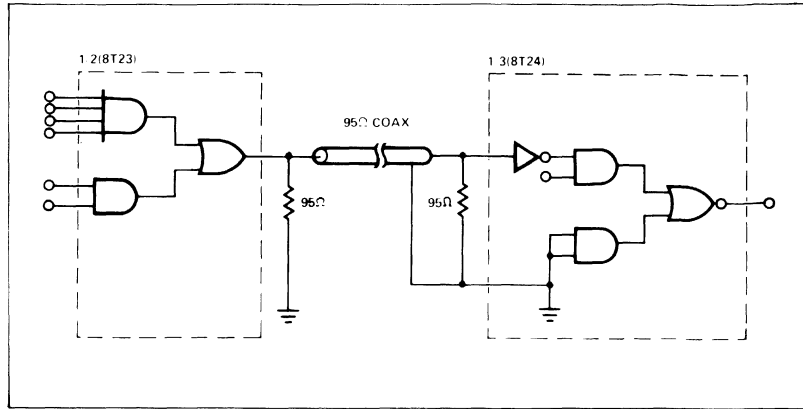
Receiver no.	POSITION	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

Verify in each of three (3) positions of S_1 (Figure 1) that the following occurs per Figure 2.

- V_1 and V_2 must be between 0.7V minimum and 1.7V maximum.
- Hysteresis = $V_1 - V_2$

TYPICAL APPLICATION



DESCRIPTION

The 8T25 is a Dual MOS-to-TTL interface element. The Sense Amplifier is designed to accept low level MOS signals from the output of Random Access Memories and the information is stored in a latch in response to an external Strobe signal. A tristate output buffer presents the data to the output using conventional TTL logic levels. The 8T25 operates from a single +5 volt supply.

CIRCUIT OPERATION

A logic "1" level on the PRESET/DISABLE line will disconnect the outputs of the Sense Amplifier from a common bus by turning both totem-pole transistors off. When the Preset/Disable line returns to a logic "0" level, the outputs will be preset to a logic "1" state. A low-going Strobe pulse will then transfer the data at Inputs A and B to their respective outputs non-inverted.

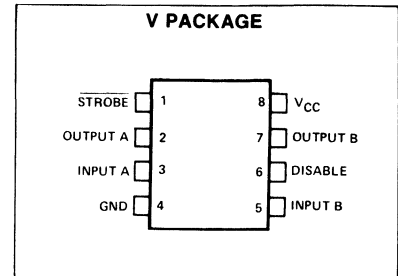
Due to the internal latch, output data will remain stable regardless of any change in input levels until a Disable signal again forces both outputs to the high impedance state.

If the STROBE is not used (STROBE = 0) the effect of the Preset/Disable line is to first disconnect the data from the tri-state bus (PRESET/DISABLE HIGH) and then transfer the input data to the output.

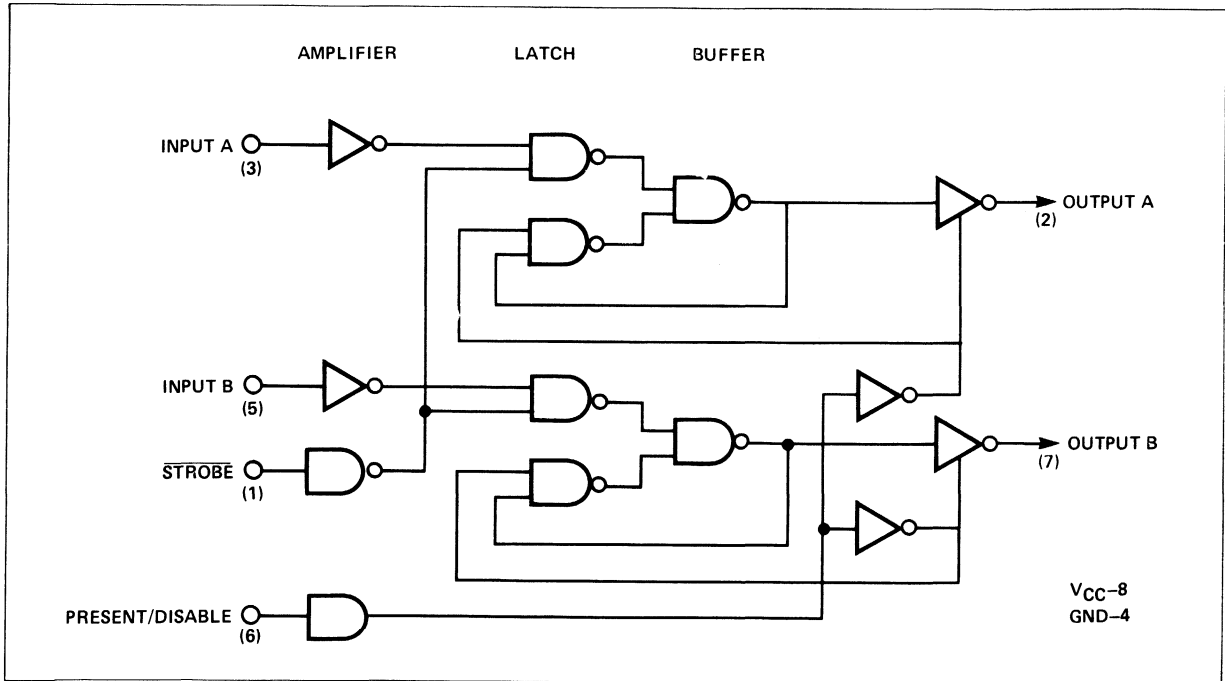
FEATURES

- MOS-TO-TTL CONVERTER
- INTERNAL LATCH
- TRISTATE OUTPUTS
- SINGLE +5V SUPPLY

PIN CONFIGURATION



LOGIC DIAGRAM

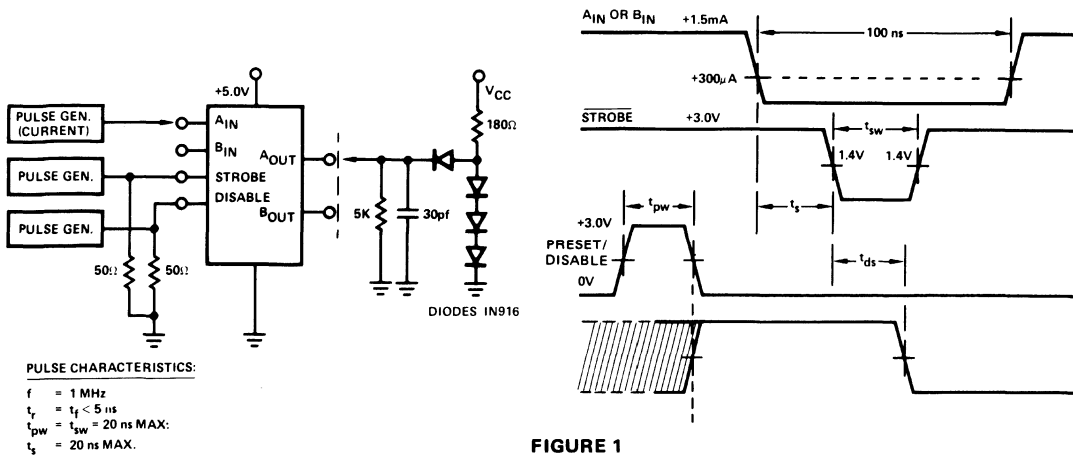


ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

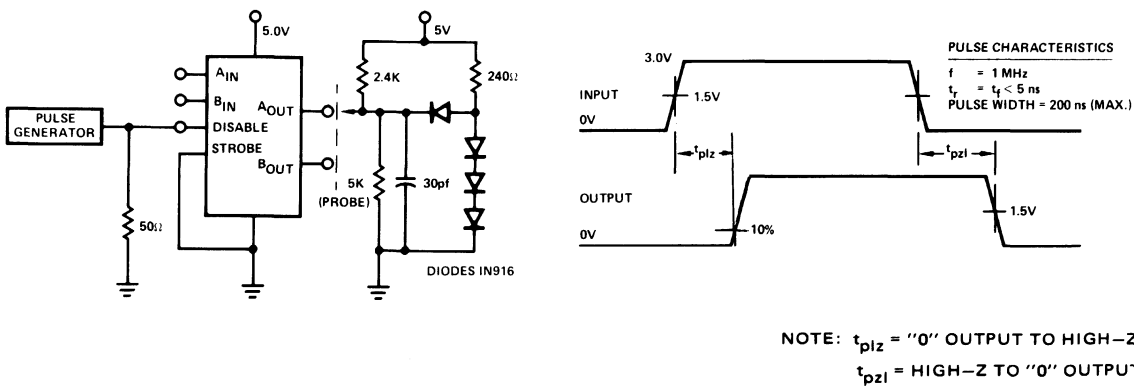
PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
Propagation Delay Strobe to Output (t_{ds})		15	25	ns
Disable to "0" Output (t_{pZL})		15	25	ns
"0" Output to Disable (t_{pLZ})		8	15	ns
Disable to "1" Output (t_{pZH})		15	25	ns
"1" Output to Disable (t_{pHZ})		9	20	ns

AC TEST CIRCUITS AND WAVEFORMS

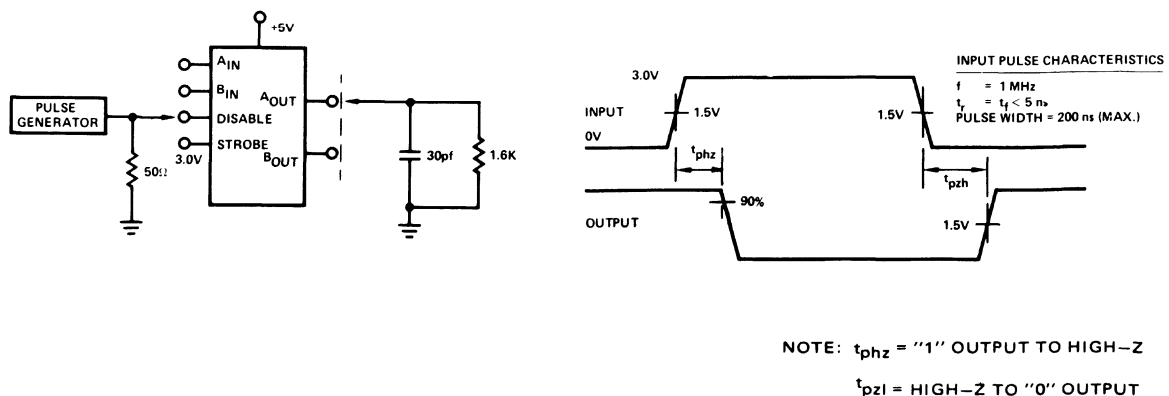
PROPAGATION DELAY (STROBE TO OUTPUT)



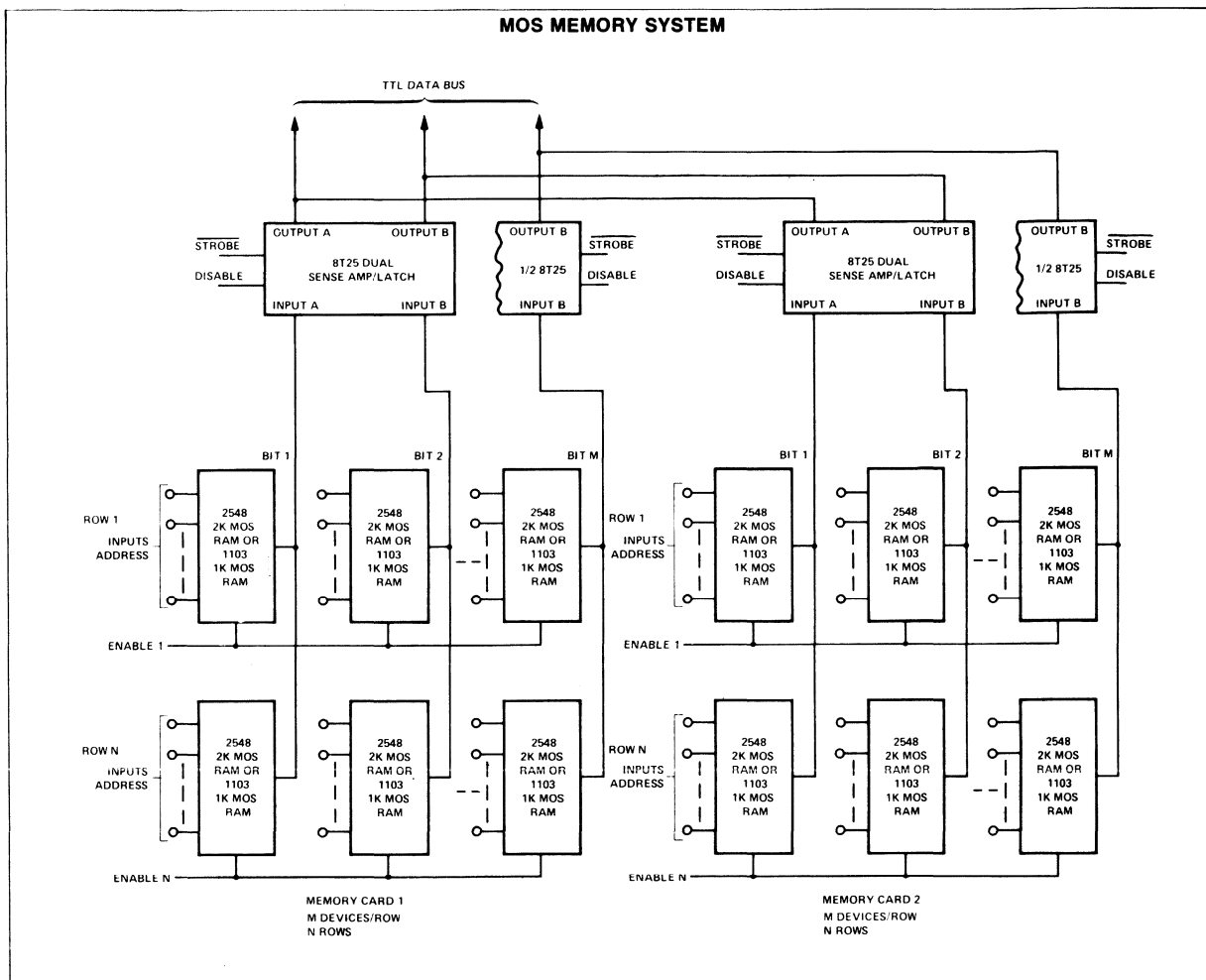
PROPAGATION DELAY (DISABLE TO OUTPUT)



PROPAGATION DELAY (DISABLE TO OUTPUT)

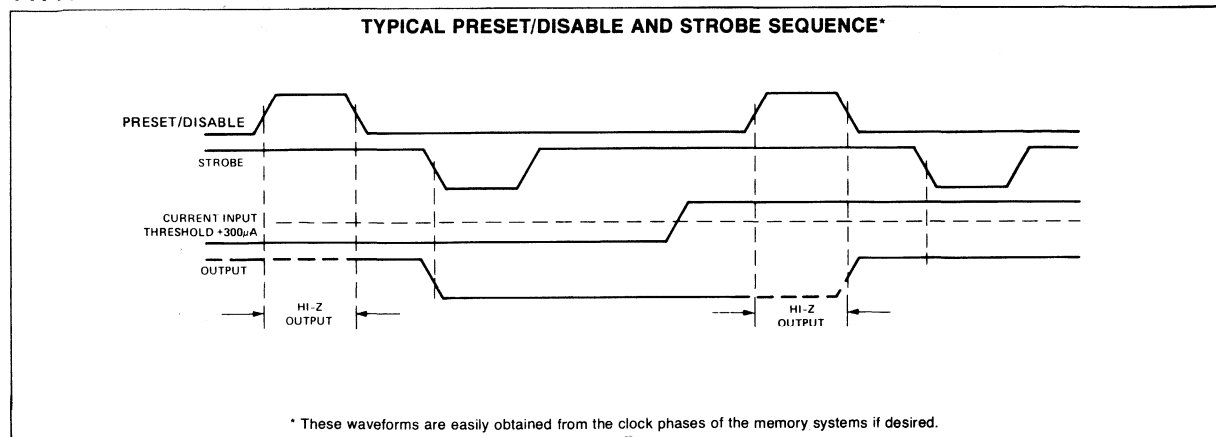


TYPICAL APPLICATION



NOTE: EACH MEMORY CARD IS AN
 N (2K) XM MEMORY FOR 2548 2K MOS RAM
 N(K) XM MEMORY FOR 1103 1K MOS RAM

TYPICAL WAVEFORMS



* These waveforms are easily obtained from the clock phases of the memory systems if desired.

DESCRIPTION

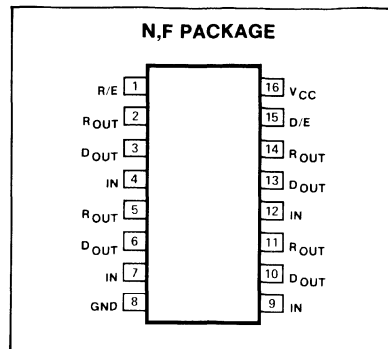
The 8T26A/28 consists of four pairs of 3-State logic elements configured as Quad Bus Drivers/Receivers along with separate buffered receiver enable and driver enable lines. This single IC Quad Transceiver design distinguishes the 8T26A/28 from conventional multi-IC implementations. In addition, the 8T26/28's ultra high speed while driving heavy bus capacitance (300pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

Both the Driver and Receiver gates have 3-State outputs and low-current PNP inputs. 3-State outputs provide the high switching speeds of totempole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200µA maximum.

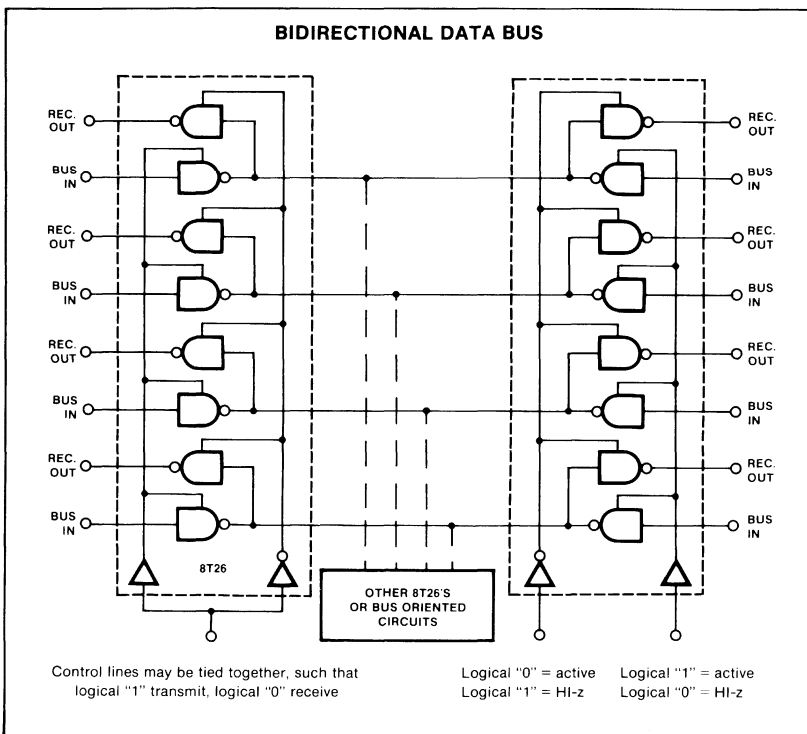
APPLICATIONS

- Half-duplex data transmission
- Memory interface buffers
- Data routing in bus oriented systems
- High current drivers
- MOS/CMOS-to-TTL interface

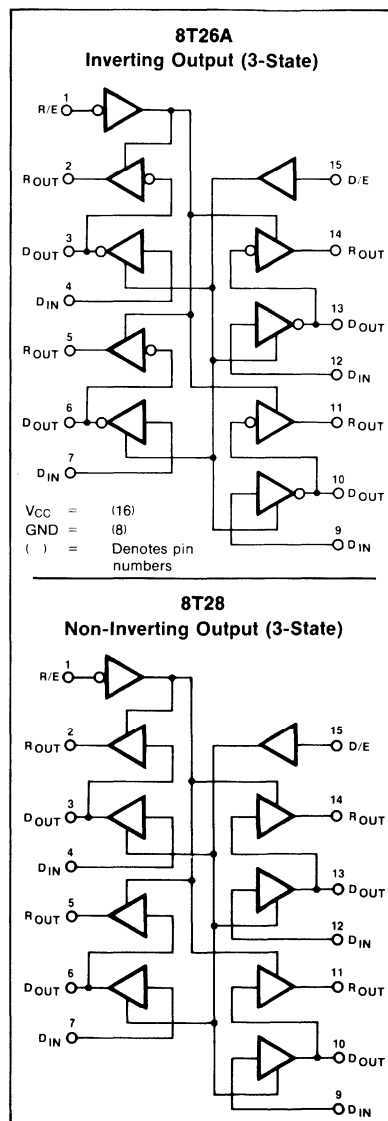
PIN CONFIGURATION



TYPICAL APPLICATION



LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS

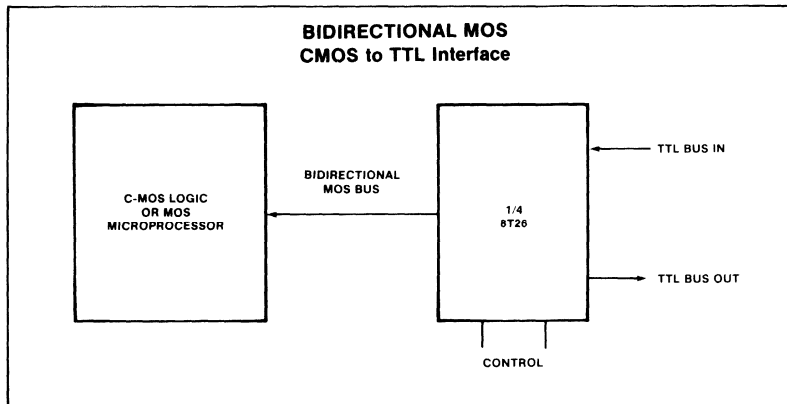
PARAMETER	TEST CONDITIONS	8T26A			8T28			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp V _{CC} = MIN, I _{IN} = -12mA		N/A N/A	-1.0		N/A N/A	-1.0	V
V _{OL}	Output voltage Low Drive Receive I _{OL} = 48mA I _{OL} = 20mA V _{CC} = MAX, V _{IN} = 0.4V			0.5 0.5			0.5 0.5	V V
I _{IL}	Input current Low Drive (low level) Disabled (low level) Receive			-200 -25 -200			-200 -25 -200	mA mA mA

NOTE
Output sink current is supplied through a resistor to ground.

AC ELECTRICAL CHARACTERISTICS

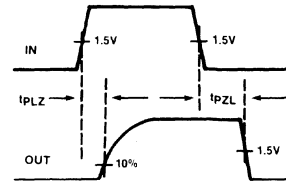
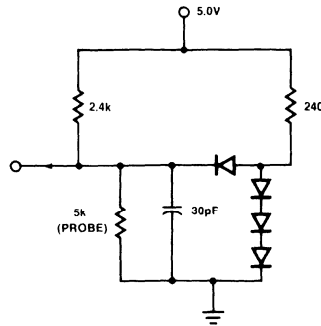
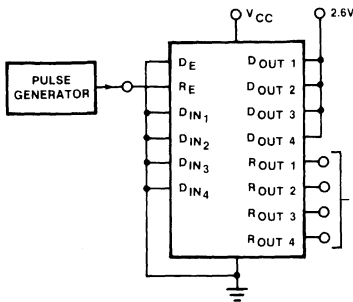
PARAMETER	TO	FROM	TEST CONDITIONS	8T26A			8T28			UNIT
				Min	Typ	Max	Min	Typ	Max	
t _{ON}	R _{OUT}	D _{OUT}	C _L = 30pF			14			17	ns
	D _{OUT}	D _{IN}	C _L = 300pF			14			17	ns
t _{OFF}	R _{OUT}	D _{OUT}	C _L = 30pF			14			17	ns
	D _{OUT}	D _{IN}	C _L = 300pF			14			17	ns
tp _{ZL}	0	High Z	C _L = 300pF			25			28	ns
tp _{ZL}	High Z	0				20			23	ns
tp _{ZL}	0	High Z	C _L = 30pF			20			23	ns
tp _{LZ}	High Z	0				15			18	ns

TYPICAL APPLICATION



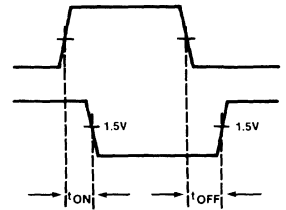
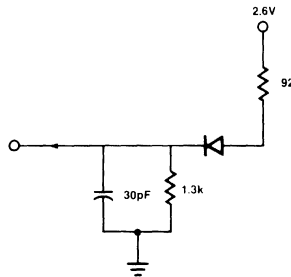
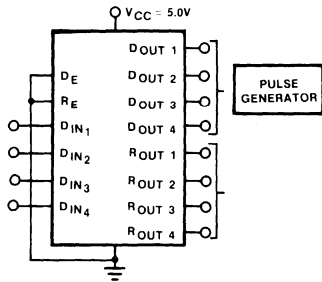
AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY
RECEIVE ENABLE TO RECEIVE OUTPUT



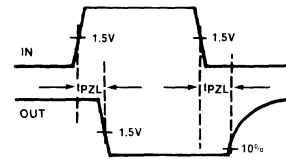
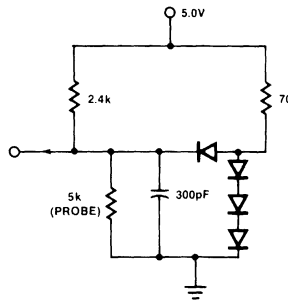
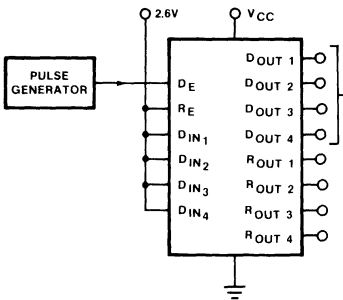
Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 freq = 5MHz (50% duty cycle)
 Amplitude = 2.6V

DOUT TO ROUT



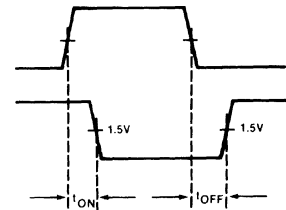
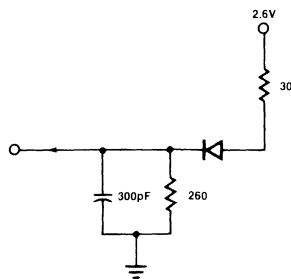
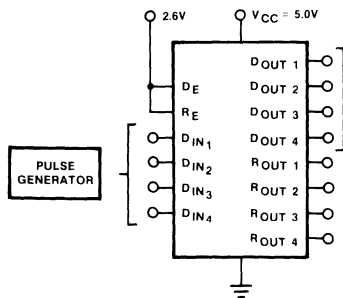
Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 freq = 10MHz (50% duty cycle)
 Amplitude = 2.6V

DATA ENABLE TO DATA OUTPUT



Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 freq = 10MHz (50% duty cycle)
 Amplitude = 2.6V

DIN TO DOUT



DESCRIPTION

The 8T30 is a dual bi-directional bus interchange element that interfaces MOS and TTL data busses. Data can be exchanged in a half-duplex transmission mode from a "party line" TTL/DTL bus to a MOS transceiver port and a TTL/DTL transceiver port. For maximum versatility the receive inputs and high current sink open collector transmit outputs are brought out separately.

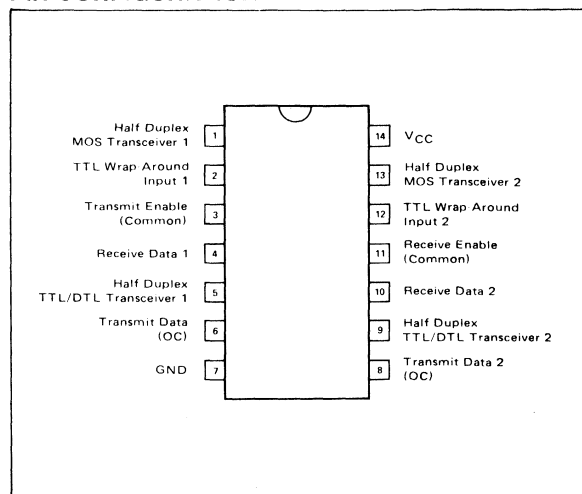
Common receive and transmit enable controls condition each half of the 8T30 for six valid modes of operation as tabulated in Table 1.

Pins 6 and 4 (8 and 10) are typically connected such that data from a common high performance "party line" bus can be routed to and from the TTL/DTL and MOS transceiver ports. In addition, wrap-around inputs are provided such that TTL/DTL data can be sent directly to the MOS transceiver port and the TTL/DTL "party line drivers" without using the TTL/DTL transceiver port.

A high performance emitter follower driver and a low current base input on the MOS transceiver port make the 8T30 a superior MOS bus interface element.

A power-down sequence (as V_{CC} is varied from 5.25V to 0V) of the 8T30 will have no effect on the transmit outputs i.e., the "party line" bus driving the port controller.

PIN CONFIGURATION



8T30 VALID OPERATING MODES

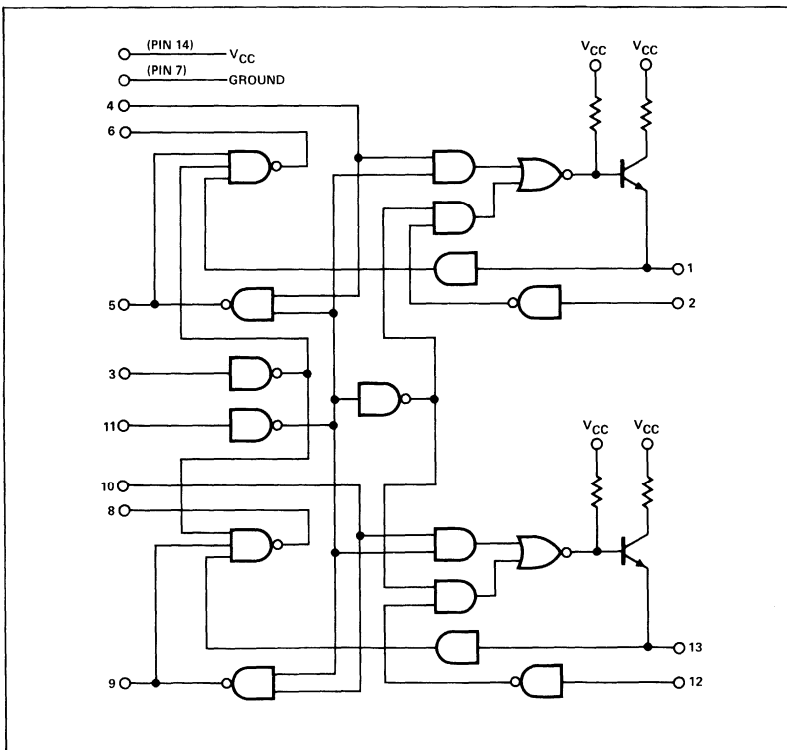
MODE OF OPERATION	PIN FUNCTIONS	PIN NUMBERS					
		6 & 4 (8 & 10)	2 (12)	5 (9)	3	11	1 (13)
Port Controller Receives Data From TTL/DTL System	Control Data In Data Out	Data	0	Data	1	0	Data
TTL/DTL Transceiver Sends Data to TTL/DTL System	Control Data In Data Out	Data	0	Data	0	1	1
MOS Transceiver Sends Data to TTL/DTL System	Control Data In Data Out	Data	0	1	0	1	Data
MOS Transceiver Receives Data from TTL/DTL Wrap-Around Input	Control Data In Data Out	X	Data	1	1	1	Data
TTL/DTL System Receives Data From TTL/DTL Wrap-Around Input	Control Data In Data Out	Data	Data	1	0	1	Data
Port Controller Idle (Random Activity on Pins 1(13), 2(12), and 5(9) Does Not Affect Bus on 6, 4 (8, 10))	Control Data In Data Out	X X	X	X	1	1	X

(X = Don't Care, 1 = Logic "1", 0 = Logic "0")

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Propagation Delays					
TTL/DTL Transceiver Inputs to Transmit Outputs	t_{on} Fig. 1, 2 $R_L = 220\Omega, C_L = 50pF$		14	25	ns
	t_{off}		14	20	ns
MOS Transceiver Inputs to Transmitter Outputs	t_{on} Fig. 2, 3 $R_L = 220\Omega, C_L = 50 pF$		23	70	ns
	t_{off}		23	50	ns
TTL Wraparound Inputs to Transmit Outputs	t_{on} Fig. 2, 4 $R_L = 220\Omega, C_L = 50 pF$		120	175	ns
	t_{off} $R_F = 11.2K, C_F = 30 pF$		36	75	ns
Receive Inputs to TTL/DTL Transceiver Outputs	t_{on} Fig. 2, 5 $R_L = 100\Omega, C_L = 30 pF$		42	60	ns
	t_{off} Fig. 2, 5 $R_L = 4K\Omega, C_L = 30 pF$		13	20	ns
Receive Inputs to MOS Transceiver Outputs	t_{on} Fig. 6, 7 $R_F = 11.2K, C_F = 30 pF$		14	35	ns
	t_{off}		106	135	ns
Transmit Enable to Transmit Outputs	t_{on} Fig. 8, 9 $R_L = 220\Omega, C_L = 50 pF$		19	40	ns
	t_{off}		19	40	ns
Receive Enable to TTL/DTL Transceiver Outputs	t_{on} Fig. 9, 10 $R_L = 400\Omega, C_L = 30 pF$		46	60	ns
	t_{off} Fig. 9, 10 $R_L = 4K\Omega, C_L = 30 pF$		19	35	ns
Receive Enable to MOS Transceiver Outputs	t_{on} Fig. 11, 12 $R_F = 11.2K, C_F = 30 pF$		20	50	ns
	t_{off}		115	155	ns

LOGIC DIAGRAM



AC TEST FIGURES AND WAVEFORMS

t_{on} , t_{off} TRANSCIVER INPUTS TO TRANSMIT OUTPUTS

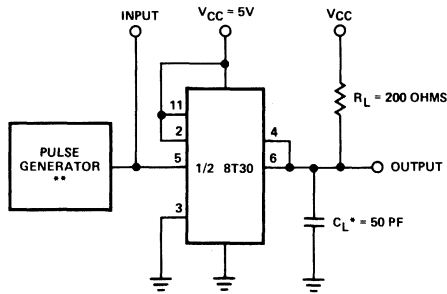
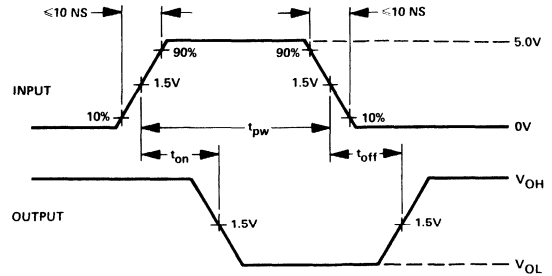


FIGURE 1

WAVEFORMS



* C_L INCLUDES STRAY AND PROBE CAPACITANCE
 ** $t_{pw} \cong 0.5 \mu\text{SEC}$, $\text{PRR} \cong 1 \text{ MHz}$, $R_{out} \cong 50 \text{ OHMS}$

FIGURE 2

t_{on} , t_{off} MOS TRANSCIVER TO TRANSMIT OUTPUTS

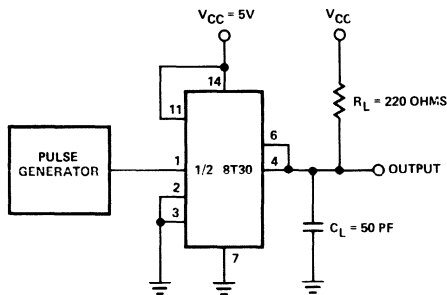
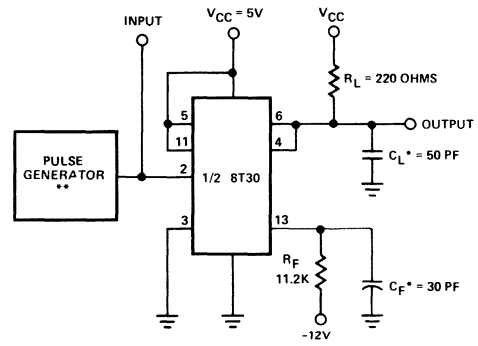


FIGURE 3

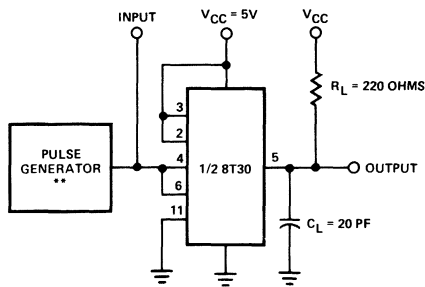
t_{on} , t_{off} TTL WRAPAROUND INPUTS TO TRANSMIT OUTPUTS



* C_F , C_L INCLUDES STRAY AND PROBE CAPACITANCE
 ** $t_{pw} \cong 0.5 \mu\text{SEC}$, $\text{PRR} \cong 1 \text{ MHz}$, $R_{out} \cong 50 \text{ OHMS}$
 SEE FIGURE 2 FOR WAVEFORMS

FIGURE 4

t_{on} , t_{off} RECEIVE INPUTS TO TTL/DTL TRANSCIVER OUTPUTS



* C_L INCLUDES STRAY AND PROBE CAPACITANCE
 ** $t_{pw} \cong 0.5 \mu\text{SEC}$, $\text{PRR} \cong 1 \text{ MHz}$, $R_{out} \cong 50 \text{ OHMS}$
 SEE FIGURE 2 FOR WAVEFORMS

FIGURE 5

t_{on} , t_{off} RECEIVE INPUTS TO MOS TRANSCIVER OUTPUTS

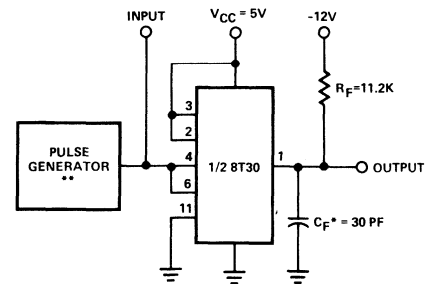


FIGURE 6

AC TEST FIGURES AND WAVEFORMS (Cont'd)

t_{on}, t_{off} WAVEFORMS

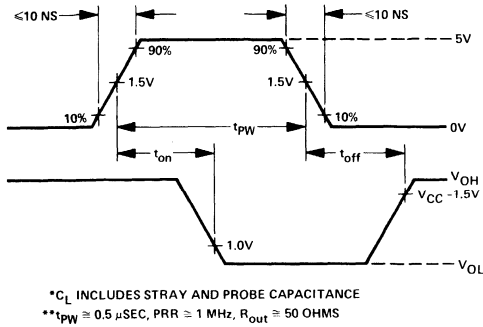


FIGURE 7

TRANSMIT ENABLE TO TRANSMIT OUTPUTS

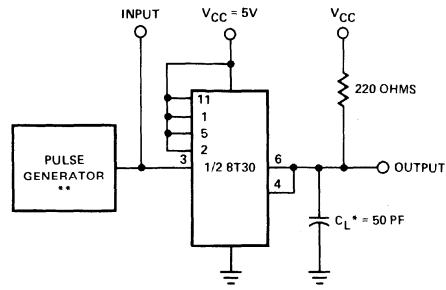


FIGURE 8

t_{on}, t_{off} WAVEFORMS

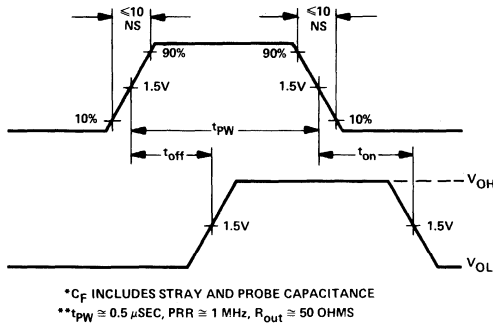
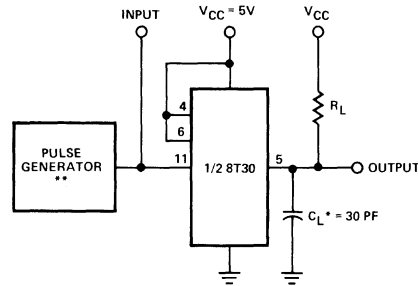


FIGURE 9

t_{on}, t_{off} RECEIVE ENABLE TO TTL/DTL TRANSCEIVER OUTPUTS



*C_F, C_L INCLUDES STRAY AND PROBE CAPACITANCE
 **t_{pw} ≅ 0.5 μSEC, PRR ≅ 1 MHz, R_{out} ≅ 50 OHMS
 SEE FIGURE 2 FOR WAVEFORMS

FIGURE 10

t_{on}, t_{off} RECEIVE ENABLE TO MOS TRANSCEIVER OUTPUTS

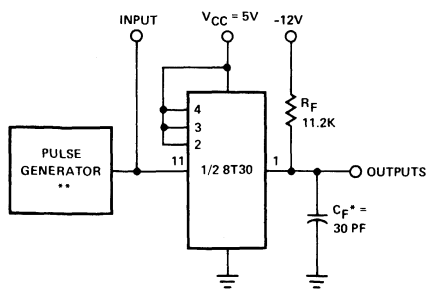


FIGURE 11

t_{on}, t_{off} WAVEFORMS

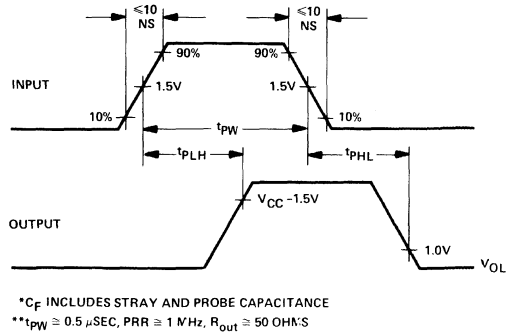
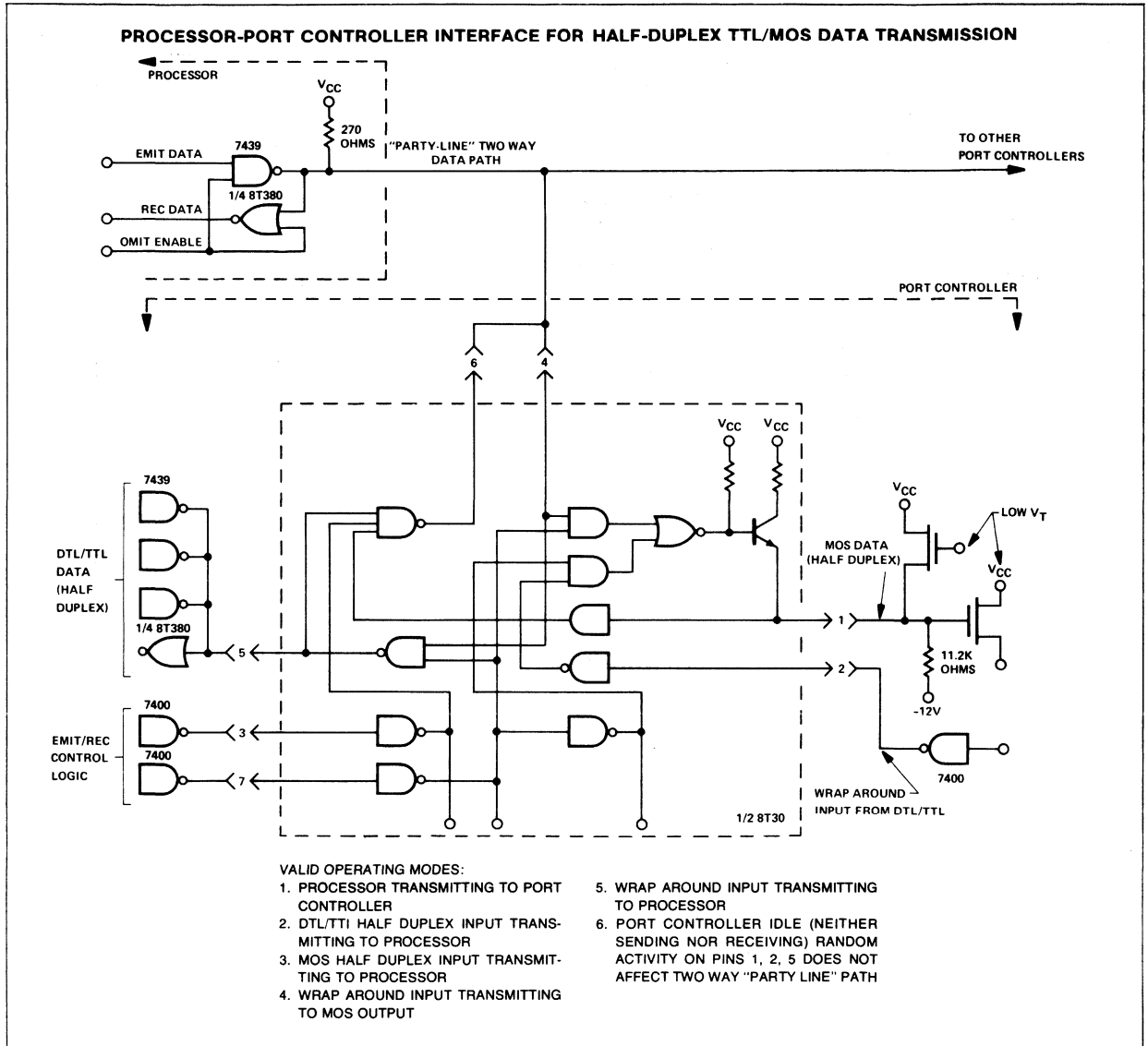


FIGURE 12

TYPICAL APPLICATION

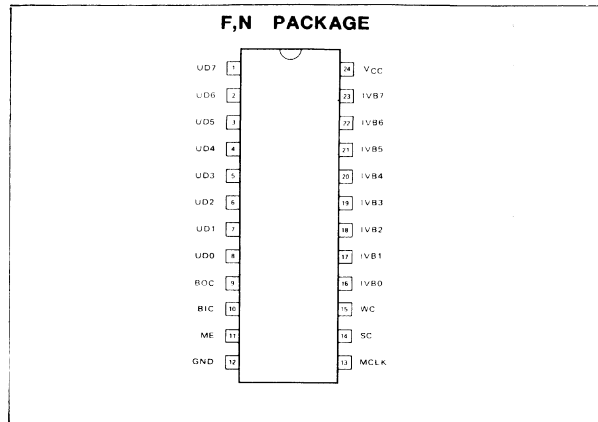


DESCRIPTION

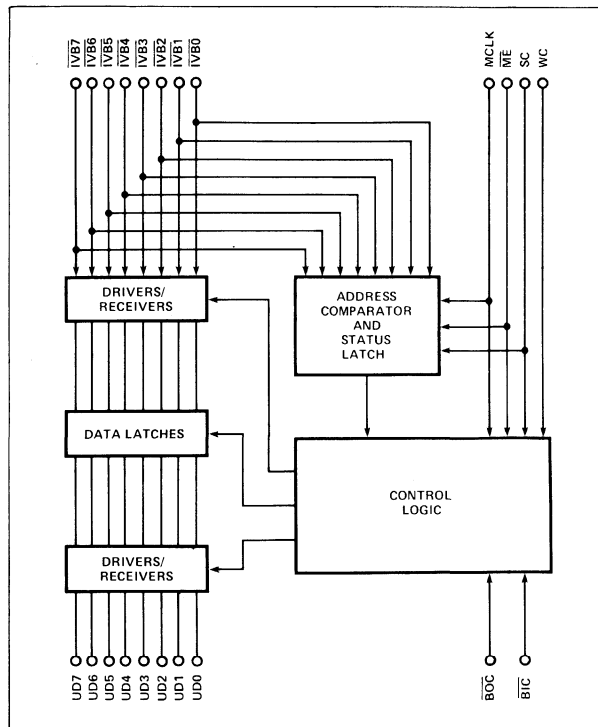
The Interface Vector (IV) Byte is an 8-bit bi-directional data register designed to function as an I/O interface element in microprocessor systems. It contains eight clocked data latches accessible from either a microprocessor (IV) port or a user port. Separate I/O control is provided for each port. The two ports operate independently, except when both are attempting to input data into the IV Byte. In this case, the user port has priority.

A unique feature of the IV Byte is the way in which it is addressed. Each IV Byte has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is high, data at the microprocessor port is treated as an address. If the address matches the IV Byte's internally programmed address, the microprocessor port is enabled, allowing data transfer through it. The port remains enabled until an address which does not match is presented, at which time the port is disabled (data transfer is inhibited). A Master Enable input (ME) can serve as a ninth address bit, allowing 512 IV Bytes to be individually selected on a bus, without decoding. The user port is accessible at all times, independent of whether or not the microprocessor port is selected.

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

USER DATA BUS CONTROL

The activity of the User Data Bus is controlled by the \overline{BIC} and \overline{BOC} inputs as shown in Table 1. (H represents high, L represents low.)

Table 1
BIC and BOC function Control

\overline{BIC}	\overline{BOC}	MCLK	USER DATA BUS
H	L	X	Output Data
L	X	H	Input Data
L	X	L	Inactive
H	H	X	Inactive

To avoid conflicts at the Data Latch, input from the microprocessor port is inhibited when \overline{BIC} indicates user data is being input. Under all other conditions, the two ports operate independently.

INTERFACE VECTOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port (IV Bus) is controlled by the \overline{ME} , SC, WC and \overline{BIC} inputs, as well as the state of an internal status latch. \overline{BIC} is included to show user port priority over the microprocessor port for data input.

TABLE 2
MICROPROCESSOR PORT FUNCTION CONTROL

ME	SC	WC	MCLK	\overline{BIC}	Status Latch	IVBX Function
L	L	L	X	X	SET	Output Data
L	L	H	H	H	SET	Input Data
L	H	L	H	X	X	Input Address
L	H	H	H	L	X	Input Address
L	H	H	H	H	X	Input Data and Address
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	not set	Inactive
H	X	X	X	X	X	Inactive

Each IV Byte's status latch stores the result of the most recent IV Byte select; it is set when the IV Byte's internal address matches the IV Bus. It is cleared when an address that differs from the internal address is presented on the IV Bus. In normal operation, the state of the status latch acts like a master enable; the microprocessor port can transfer data only when the status latch is set.

When SC and WC are both high, data on the IV Bus is accepted as data, whether or not the IV Byte was selected. The data is also interpreted as an address. The IV Byte sets its select status if its address matches the data read when SC and WC were both high; it resets its select status otherwise.

BUS OPERATION

Data written into the IV Byte from one port will appear inverted when read from the other port. Data written into the IV Byte from one port will not be inverted when read from the same port.

Figure 1 shows various ways to use the IV Byte in a system by controlling the states of the \overline{BIC} and \overline{BOC} lines. BYTE 1 is for input only, BYTE 2 is for output only, BYTE 3 is bidirectional under user control. BYTE 4 is output only (6 bits) with two bits reserved for system control of BYTE 5.

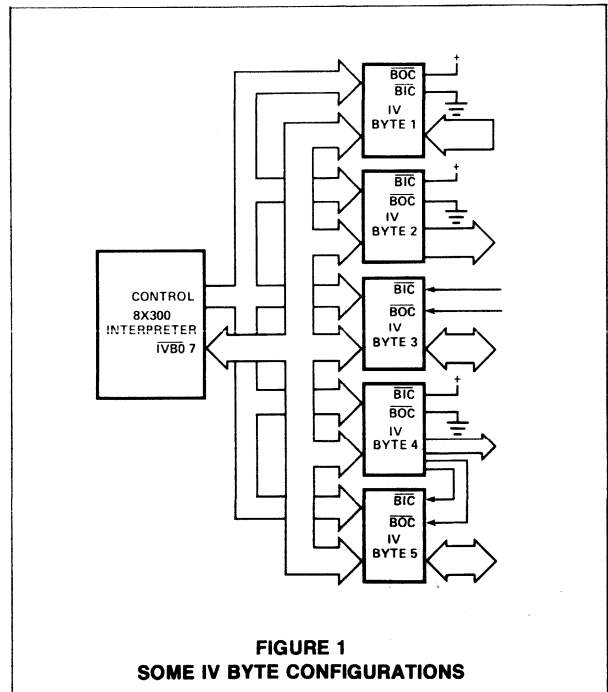
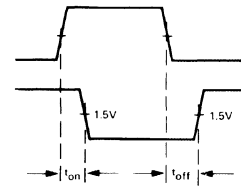
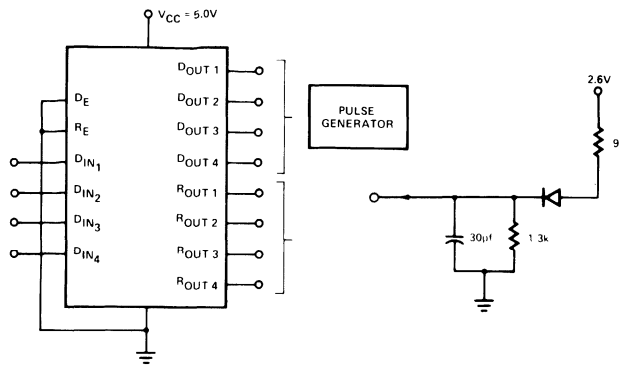


FIGURE 1
SOME IV BYTE CONFIGURATIONS

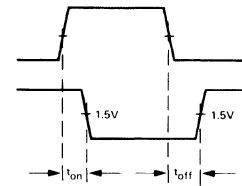
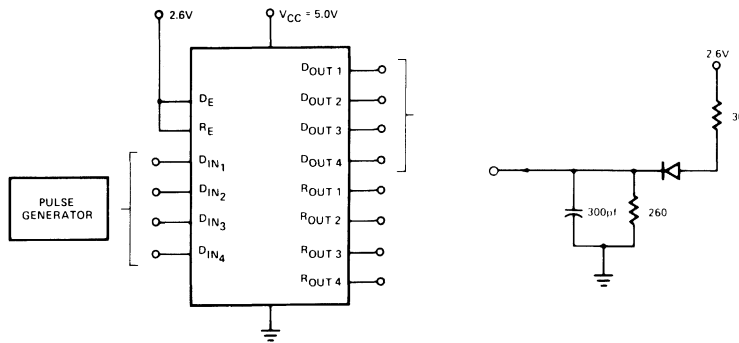
AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (D_{OUT} TO R_{OUT})



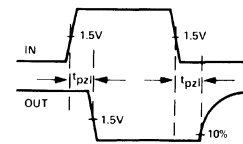
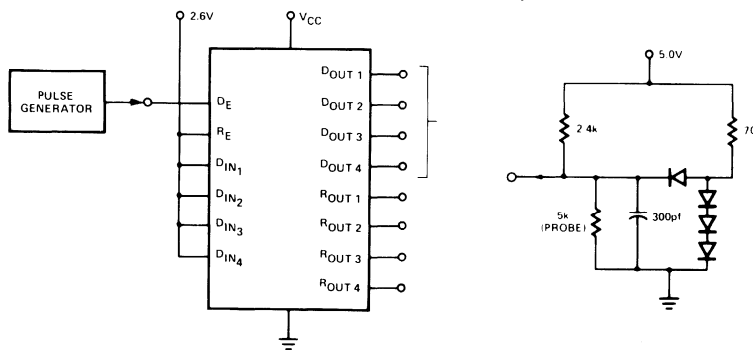
INPUT PULSE:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 freq = 10MHz (50% duty cycle)
 Amplitude = 2.6V

PROPAGATION DELAY (D_{IN} TO D_{OUT})



INPUT PULSE:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 freq = 10MHz (50% duty cycle)
 Amplitude = 2.6V

PROPAGATION DELAY (DATA ENABLE TO DATA OUTPUT)



INPUT PULSE:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 freq = 5MHz (50% duty cycle)
 Amplitude = 2.6V

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	$\overline{UD0} - \overline{UD7}$:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment. Either tri-state or open collector outputs are available.	ACTIVE HIGH
16-23	$\overline{IVB0} - \overline{IVB7}$:	Interface Vector Bus. Bidirectional tri-state data lines to communicate with controlling digital system (microprocessor).	ACTIVE LOW
10	\overline{BIC} :	Byte Input Control. User input to control writing into the IV Byte from the User Data Lines.	ACTIVE LOW
9	BOC:	Byte Output Control. User input to control reading from the IV Byte onto the User Data Lines.	ACTIVE LOW
14	SC:	Selected Command. When SC is high and WC is low, data on $\overline{IVB0} - \overline{IVB7}$ is interpreted as an address. IV Byte selects itself if its address is identical to IV bus data; it de-selects itself otherwise.	ACTIVE HIGH
15	\overline{WC} :	Write Command. When WC is high and SC is low, IV Byte, if selected, stores contents of $\overline{IVB0} - \overline{IVB7}$ as data.	ACTIVE HIGH
11	ME:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	ACTIVE LOW
13	MCLK:	Master Clock. Input to strobe data into the latches.	
24	VCC:	5 volt power connection.	
12	GND:	Ground.	

PARAMETER MEASUREMENT INFORMATION

Load Circuit for Open Collector Outputs

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

Load Circuit for Tristate Outputs

L	H	S1 OPEN
H	Z	S2 CLOSED
Z	H	
H	L	S1 CLOSED
L	Z	S2 OPEN
Z	L	

NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

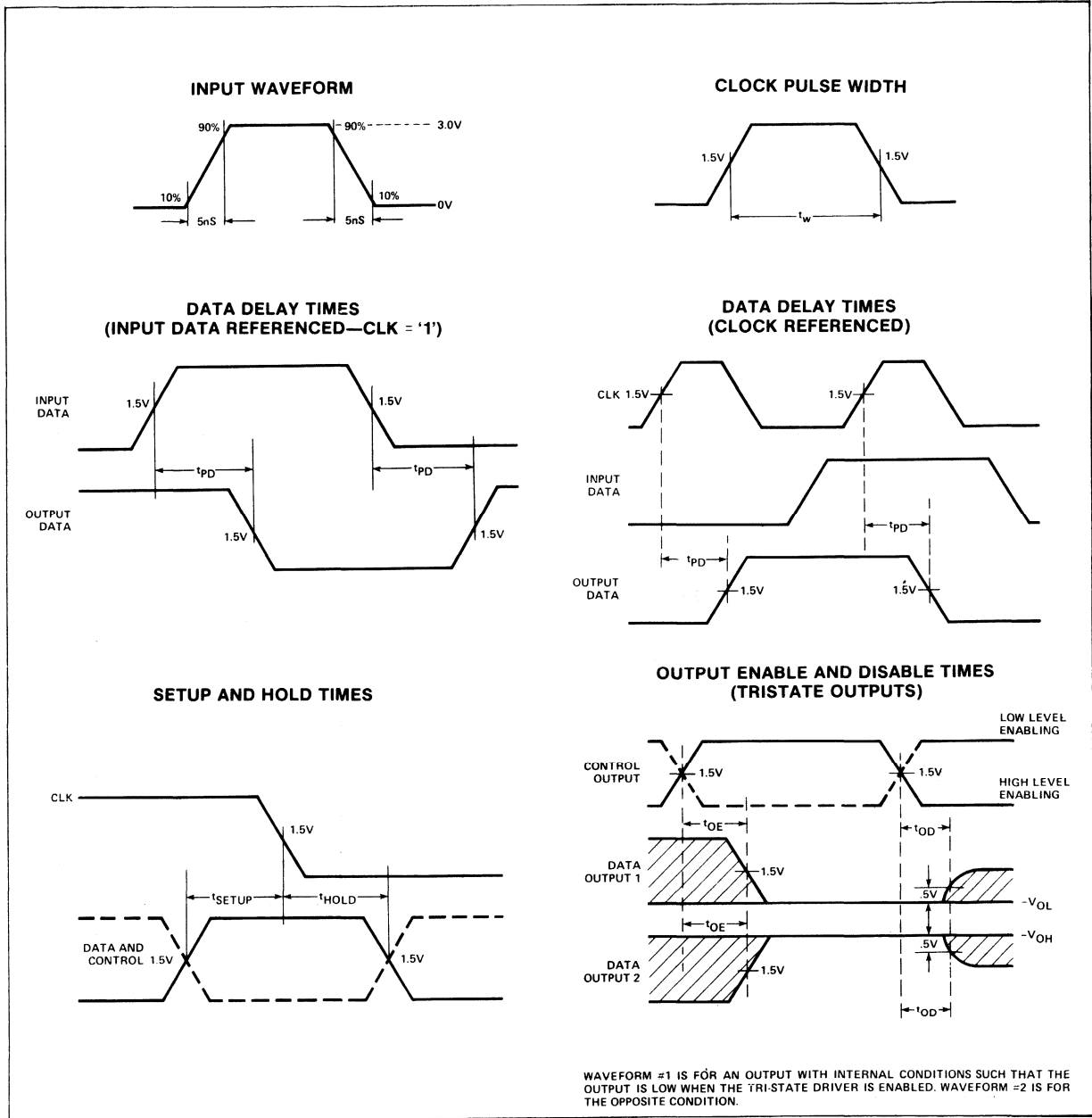
AC ELECTRICAL CHARACTERISTICS

(Limits apply for $V_{CC} = 5V \pm 5\%$ and $0^\circ C \leq T_A \leq 70^\circ C$ unless specified otherwise.)

Parameter	Symbol	Input	Output	Conditions	Limits			Units
					Min.	Typ.	Max.	
User Data Delay (Note 1)	t _{PD}	UDX MCLK	\overline{IVBX}	C _L = 30pF		19		ns
			IVBX	C _L = 30pF		36		ns
User Output Enable	t _{OE}	\overline{BIC}	UDX	C _L = 30pF		26		ns
		\overline{BOC}	UDX	C _L = 30pF		28		ns
User Output Disable	t _{OD}	\overline{BIC}	UDX	C _L = 30pF		22		ns
		\overline{BOC}	UDX	C _L = 30pF		13		ns
IV Data Delay (Note 1)	t _{PD}	\overline{IVBX} MCLK	UDX	C _L = 30pF		32		ns
			UDX	C _L = 30pF		40		ns
IV Output Enable	t _{OE}	\overline{ME}	\overline{IVBX}	C _L = 30pF		16		ns
		SC	IVBX	C _L = 30pF		16		ns
		WC	IVBX	C _L = 30pF		16		ns
IV Output Disable	t _{OD}	\overline{ME}	\overline{IVBX}	C _L = 30pF		15		ns
		SC	IVBX	C _L = 30pF		15		ns
		WC	IVBX	C _L = 30pF		15		ns
Clock Pulse Width	t _w	MCLK				20		ns
Setup Time (2)	t _{SETUP}	UDX				9		ns
		\overline{BIC}				22		ns
		\overline{IVBX}		(Note 5)		37		ns
		\overline{ME}		(Note 5)		23		ns
		SC		(Note 5)		23		ns
Hold Time (2)	t _{HOLD}	UDX		(Note 5)		16		ns
		\overline{BIC}		(Note 5)		3		ns
		\overline{IVBX}		(Note 5)		11		ns
		\overline{ME}		(Note 5)		0		ns
		SC		(Note 5)		0		ns
		WC		(Note 5)		4		ns

NOTES:

1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Setup and hold times given are for "normal" operation. \overline{BIC} setup and hold times are for a user write operation, SC setup and hold times are for an IV Byte select operation, WC setup and hold times are for an IV Bus write operation. ME setup and hold times are for both IV write and select operations.



ADDRESS PROGRAMMING

The IV Byte is manufactured such that an address of all high-levels (> 2V) on the IV Data Bus inputs matches the Byte's internal address. To program a bit so a low-level input (< 0.8V) matches, the following procedure should be used:

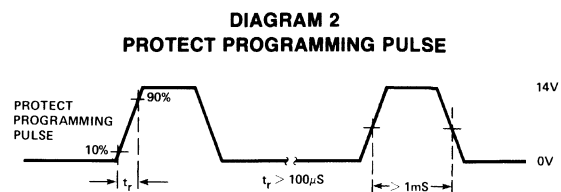
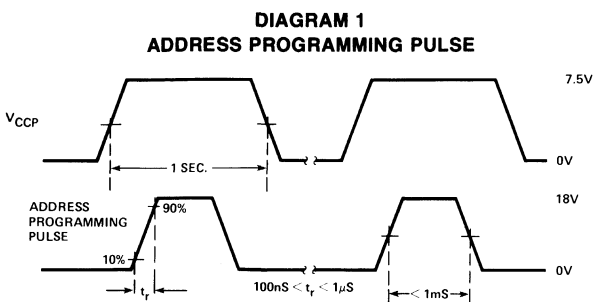
1. Set all control inputs to their inactive state (BIC = BOC = ME = V_{CC} ; SC = WC = MCLK = GND). Leave all IV Data Bus I/O pins open.

2. Raise V_{CC} to $7.75 V \pm .25V$.
3. After V_{CC} has stabilized, apply a programming pulse to the User Data Bus bit where a low-level match is desired. The voltage should be limited to 18V; the current should be limited to 75 mA. Apply the pulse as shown in Diagram 1.
4. Return V_{CC} to 0V (Note 6).

5. Repeat this procedure for each bit where a low-level match is desired.
6. Verify that the proper address is programmed by setting the Byte's status latch (IVB0 — IVB7 = desired address, ME = WC = L, SC = MCLK = H) and attempting to write through the IV Byte (BOC = SC = ME = L, BIC = WC = MCLK = H). If the proper address has been programmed, data presented at the IV Bus will appear inverted on the User Bus outputs. (Use normal V_{CC} and input voltages for verification.)

After the desired address has been programmed, a second procedure must be followed to isolate the address circuitry. The procedure is:

1. Set V_{CC} and all control inputs to 0V. (V_{CC} = BIC = BOC = ME = SC WC = MCLK = 0V). Leave all IV Data Bus I/O pins open.
2. Apply a protect programming pulse to every User Data Bus pin, one at a time. The voltage should be limited to 14V; the current should be limited to 150mA. Apply the pulse as shown in Diagram 2.
3. Verify that the address circuitry is isolated by applying 7V to each User Data Bus pin and measuring less than 1mA of input current. The conditions should be the same as in step 1 above. The rise time on the verification voltage must be slower than 100μs.



PROGRAMMING SPECIFICATIONS

Parameter	Symbol	Conditions	Limits			Units
			Min.	Typ.	Max.	
Programming Supply Voltage	V _{CCP}		7.5	0	8.0	V
Address						V
Protect						V
Programming Supply Current	I _{CCP}	V _{CCP} = 8.0V			250	mA
MAX TIME V _{CCP} > 5.25V					1.0	sec.
Programming Voltage						
Address			17.5		18.0	V
Protect			13.5		14.0	V
Programming Current						
Address					75	mA
Protect					150	mA
Programming Pulse Rise Time						
Address			.1		1	μsec
Protect			100			μsec
Programming Pulse Width			.5		1	mS

NOTES:

6. If all programming can be done in less than 1 second, V_{CC} may remain at 7.75V for the entire programming cycle.

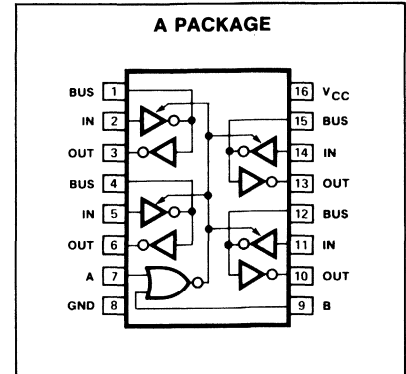
DESCRIPTION

The 8T34 is a quad transceiver with a common two input driver disable control. Tri-state driver outputs together with low input current requirements for the receivers offer extreme versatility in bus organized data transmission systems. The data busses may be terminated or unterminated.

Drivers in the third output state (Hi-Z) load

the bus only with negligible current. The receiver input current is low, allowing at least 100 driver/receiver pairs to utilize a single bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition the receiver does not load the bus with $V_{CC} = 0V$ as it may be the case when peripherals drive a common I/O bus and are shut off.

PIN CONFIGURATION



TRUTH TABLE

MODE	DISABLE	DISABLE	DRIVER IN	BUS RECEIVER		
	A	B		BUS		OUT
				IN	OUT	
Receive	H	X	X	H		L
Receive	X	H	X	L		H
Drive	L	L	H		L	H
Drive	L	L	L		H	L

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	8T34			UNIT		
		Min	Typ	Max			
V_{IL}	Input LOW voltage, Receiver	1.5		2.0	V		
V_{IH}	Input HIGH voltage, Receiver	0.8		1.5	V		
V_{IL}	Input LOW voltage, Driver			0.8	V		
V_{IH}	Input HIGH voltage, Driver	2.0			V		
V_{IC}	Clamp	$V_{CC} = \text{Min}, I_{IN} = -12\text{mA}$		-1.0	-1.5	V	
V_{OL}	Output LOW voltage Receive Bus	$V_{CC} = \text{Min}$ $I_{OL} = 16\text{mA}$ $I_{OL} = 50\text{mA}$		0.25	0.4	V	
					0.7	V	
V_{OH}	Output HIGH voltage Receive Bus	$V_{CC} = \text{Min}$ $I_{OL} = -400\mu\text{A}$ $I_{OL} = 10.4\mu\text{A}$		2.4		V	
				2.4		V	
I_{IL}	Input current LOW	$V_{CC} = \text{Max}, V_{IN} = 0.4V$			-1.6	mA	
I_{IH}	Input HIGH current Disable and driver Bus, power on Bus, power off	$V_{CC} = \text{Max}$ $V_{IN} = 2.4V$			50	μA	
		$V_{IN} = 4.0V$		20	100	μA	
		$V_{IN} = 4.0V$		20	100	μA	
I_{OS}	Short circuit output current Receive Driver	$V_{CC} = \text{Max}, V_{IN} = 0V, V_{OUT} = 0V$		-18	-33	-55	mA
				-60	-80	-105	mA
I_{CC}	Supply current	$V_{CC} = \text{Max}, V_{IN} = 2.0V$				60	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TO	FROM	TEST CONDITIONS	8T34			UNIT
				Min	Typ	Max	
t_{LZ} LOW	Bus	Disable	Load 1, $C_L = 15\text{pF}$; Waveform 3	3	9	30	ns
t_{HZ} HIGH	Bus	Disable	Load 1, $C_L = 15\text{pF}$; Waveform 4	8	15	30	ns
t_{ZL} LOW	Bus	Disable	Load 1, $C_L = 50\text{pF}$; Waveform 4	8	18	30	ns
t_{ZH} HIGH	Bus	Disable	Load 1, $C_L = 50\text{pF}$; Waveform 3	5	10	30	ns
t_{PLH}	Bus	Driver	Load 3, Waveform 5	3	6	15	ns
t_{PHL}	Bus	Driver	Load 3, Waveform 5	4	9	20	ns
t_{PLH}	Bus	Receiver	Load 2, Waveform 6	12	27	40	ns
t_{PHL}	Bus	Receiver	Load 2, Waveform 6	5	14	25	ns

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR TRI-STATE OUTPUTS

TEST POINT

FROM OUTPUT UNDER TEST

(SEE NOTE 1)

C_L

$1\text{k}\Omega$

V_{CC}

R_L

S1

(SEE NOTE 2)

S2

LOAD 1

VOLTAGE WAVEFORMS

OUTPUT CONTROL (LOW-LEVEL ENABLING)

1.5V

t_{LZ}

S1 CLOSED, S2 OPEN

$\approx 4.5\text{V}$

1.5V

t_{ZH}

S1 OPEN, S2 CLOSED

$\approx 0\text{V}$

WAVEFORM 3

3V

1.5V

t_{ZL}

S1 AND S2 CLOSED

$\approx 1.5\text{V}$

0V

t_{HZ}

0.5V

0.5V

V_{OH}

$\approx 1.5\text{V}$

$\approx 0\text{V}$

S1 AND S2 CLOSED

WAVEFORM 4

PROPAGATION DELAY TIMES

INPUT

3V

1.5V

t_{PHL}

1.5V

OUT-OF-PHASE OUTPUT

1.5V

t_{PLH}

V_{OH}

V_{OL}

WAVEFORM 5

3V

2.3V

t_{PHL}

1.5V

1.3V

t_{PLH}

1.5V

WAVEFORM 6

V_{CC}

$R_L = 390\Omega$

FROM OUTPUT UNDER TEST

TEST POINT

$C_L = 15\text{pF}$

LOAD 2

91Ω

FROM OUTPUT UNDER TEST

TEST POINT

200Ω

$C_L = 50\text{pF}$

LOAD 3

NOTES

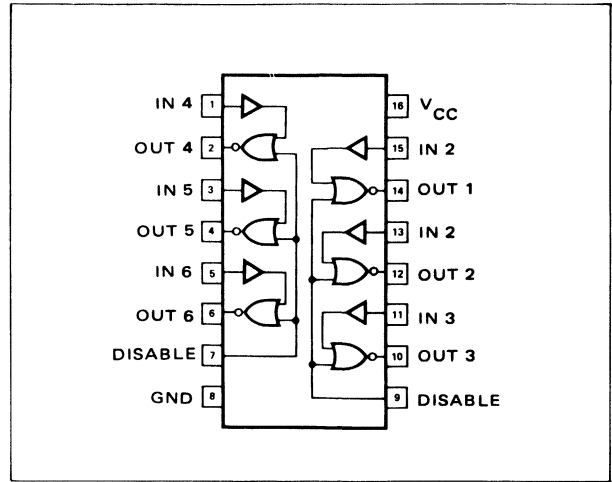
- C_L includes probe and jig capacitance
- Pin diodes are IN3064

DESCRIPTION

The 8T37 is a hex bus receiver with hysteresis organized as two triple receivers with separate disable lines for each group. Typically the devices may be used in bus organized data transmission systems interconnected by terminated lines. The low input current requirement allows several drivers and receivers to communicate over a common bus in "party line" fashion. A power-up or power-down sequence of the receiver will not affect the bus. Built in hysteresis provides maximum noise immunity and makes the 8T37 also an ideal Schmitt trigger in those applications where the non-linear input characteristics of standard TTL are undesirable.

Low input current requirements make the hex-inverter inputs compatible with MOS/CMOS in addition to DTL/TTL. All inputs have clamping diodes to simplify systems design. The receiver outputs as well as the disable inputs are TTL/DTL compatible.

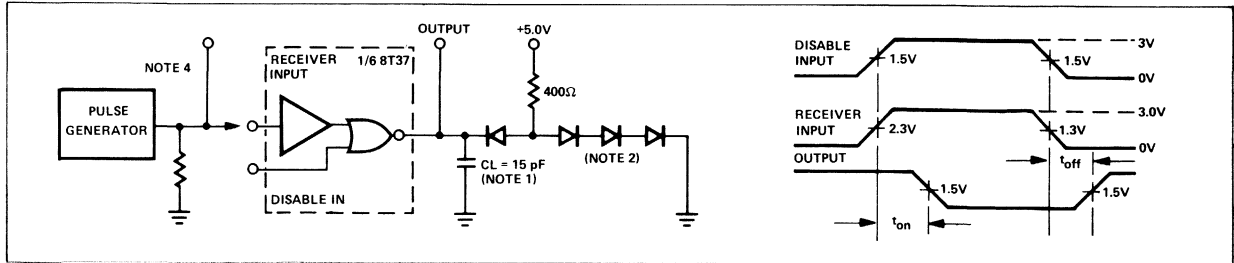
PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Propagation Delays (t_{on}, t_{off})					
Receiver t_{on}	$R_L = 400\Omega$ $C_L = 15pF$		10	30	ns
Receiver t_{off}			20	30	ns
Disable t_{on}			9	15	ns
Disable t_{off}			11	15	ns

AC TEST FIGURE AND WAVEFORMS



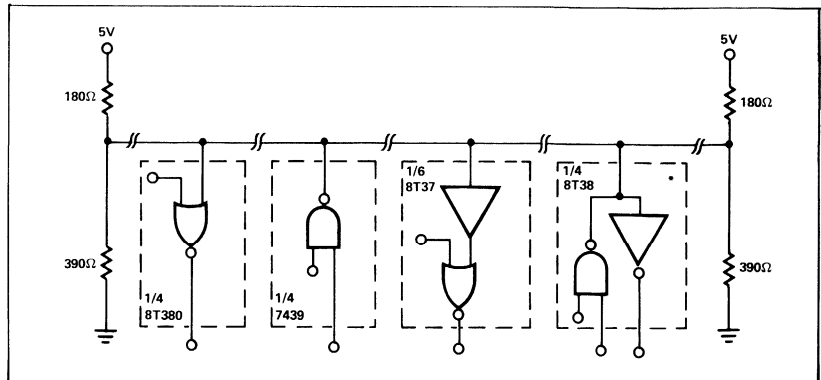
NOTES:

- Including probe and jig capacitance
- All diodes are 1N3064
- Pulse generator characteristics P.A. = 3.5V
 $Z_{OUT} = 50\Omega$
 $P_{RR} = 1MHz$
 $t_r = t_f \approx 10 ns$ (10% to 90%)
Duty Cycle = 50%
- When testing receiver, Disable = 0; when testing disable, Receiver = 0.

*** TO BE ANNOUNCED**

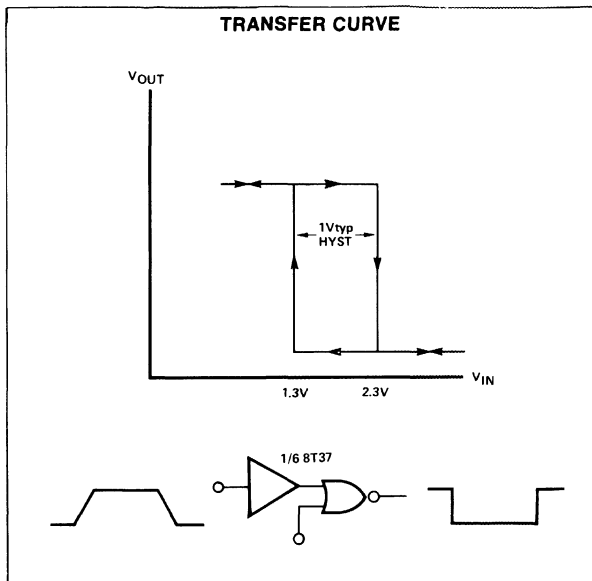
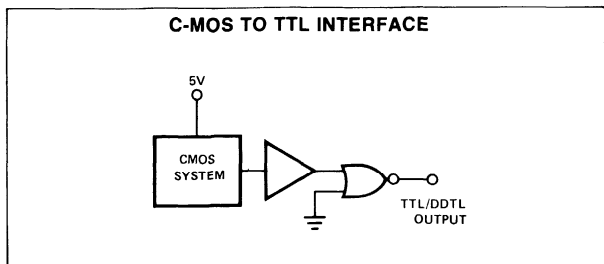
EACH TERMINATOR IS 120 OHMS THE VE-NIN'S EQUIVALENT CIRCUIT. USING FLAT RIBBON A MAXIMUM REASONABLE LENGTH IS 50 FT. FROM WHICH THE COMBINED LENGTH OF ALL TAPS OR STUBS SHOULD BE SUBTRACT. ED.

TYPICAL APPLICATION



SCHMITT TRIGGER

The receiver transfer curve shown makes the 8T37 ideal in a variety of Schmitt Trigger and waveshaping applications.



OBJECTIVE SPECIFICATION DESCRIPTION

The 8T38 is a quad bus transceiver with a common two input disable control for the drivers. Open collector driver outputs together with low input requirements for the receivers offer extreme versatility in low cost bus organized systems.

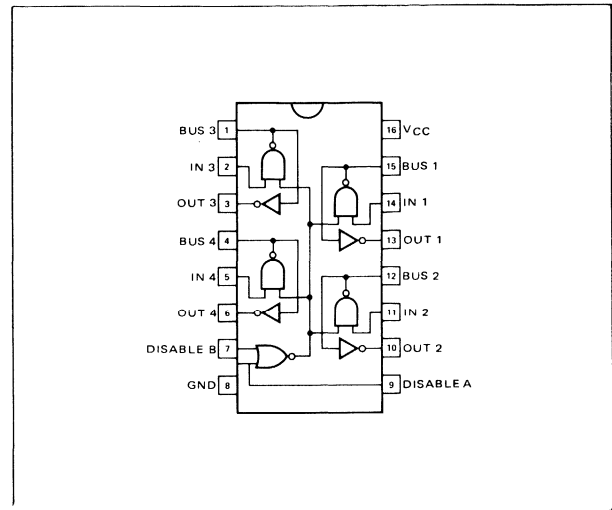
Busses may be terminated at both ends such that up to 100 driver/receiver pairs can utilize a common data bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition the receiver does not load the bus when $V_{CC} = 0$.

In those applications where only bus receiver are required the 8T380 quad bus receiver should be considered.

TRUTH TABLE

MODE	DISABLE	DISABLE	DRIVER	BUS	RECEIVER
	A	B	IN		OUT
RECEIVE	1	X	X	1	0
RECEIVE	X	1	X	0	1
DRIVE	0	0	1	0	1
DRIVE	0	0	0	1	0

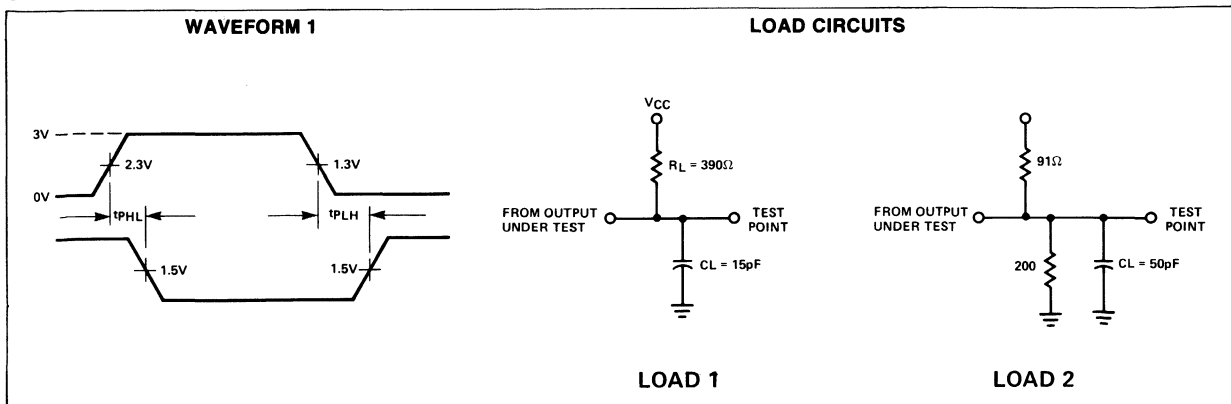
PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ C, V_{CC} = 5.0V$)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		MIN	TYP	MAX		
t_{PHL}	Disable to Bus	Load 2 $V_{in} = 0V$ to $3V$ Measured from $V_{in} = 1.5V$ to $V_{bus} = 1.5V$	11	19	30	ns
t_{PLH}	Disable to Bus		15	23	35	ns
t_{PHL}	Driver to Bus	Load 1 Waveform 1	5	12	20	ns
t_{PLH}	Driver to Bus		5	12	25	ns
t_{PHL}	Bus to Receiver		5	14	25	ns
t_{PLH}	Bus to Receiver		12	27	40	ns

SWITCHING PARAMETER MEASUREMENT INFORMATION



DESCRIPTION

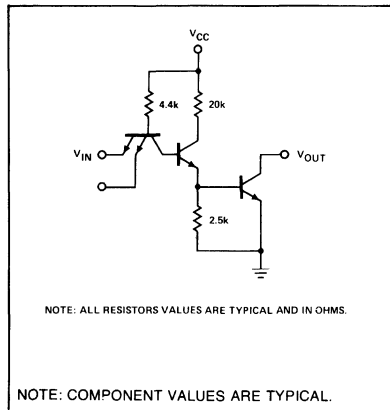
The 8T80 quad 2-input NAND interface gate and the 8T90 Hex inverter interface buffer are level translators that adapt standard 5V DTL/TTL logic to voltage levels of up to 30V.

The 8T80 performs the NAND function for positive logic (high level = logic "1") and the 8T90 performs the inverting function.

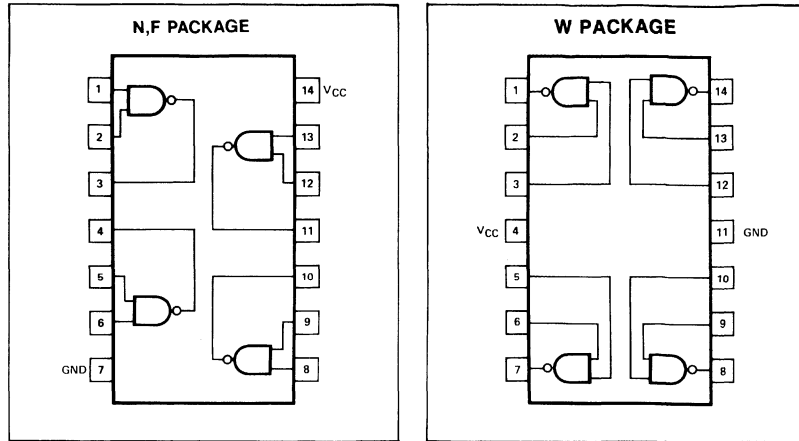
The output structure of the 8T80/90 is a high voltage transistor with uncommitted collector which allows logic swings up to 30 volts. The "bare" collector is useful for collector logic or wired-and connections.

Applications include TTL to MOS interface, lamp and relay driving as well as high level logic interfaces.

CIRCUIT SCHEMATIC



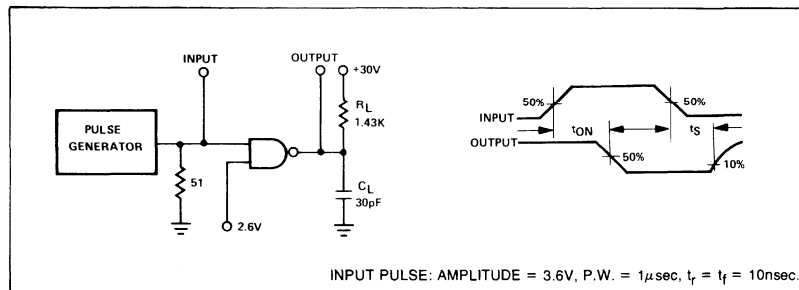
PIN CONFIGURATIONS



AC CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Turn-on Delay Storage Time	$R_L = 1.43K$ $C_L = 30pF$		35	55	ns
			40	95	ns

AC TEST AND WAVEFORMS



DESCRIPTION

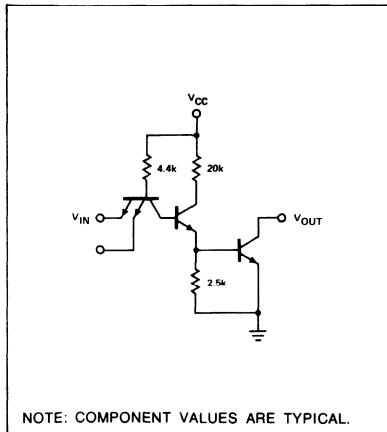
The 8T80 quad 2-input NAND interface gate and the 8T90 Hex inverter interface buffer are level translators that adapt standard 5V DTL/TTL logic to voltage levels of up to 30V.

The 8T80 performs the NAND function for positive logic (high level = logic "1" and the 8T90 performs the inverting function.

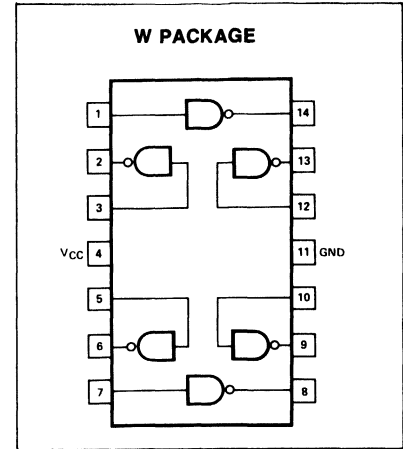
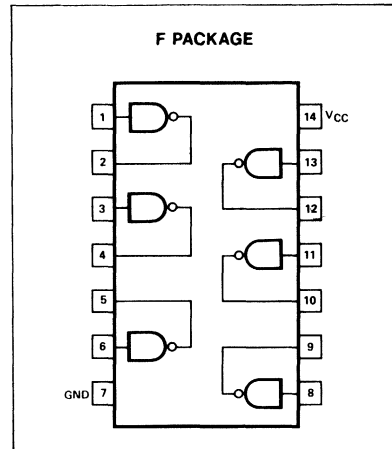
The output structure of the 8T80/90 is a high voltage transistor with uncommitted collector which allows logic swings up to 30 volts. The "bare" collector is useful for collector logic or wired-and connections.

Applications include TTL to MOS interface, lamp and relay driving as well as high level logic interfaces.

CIRCUIT SCHEMATIC



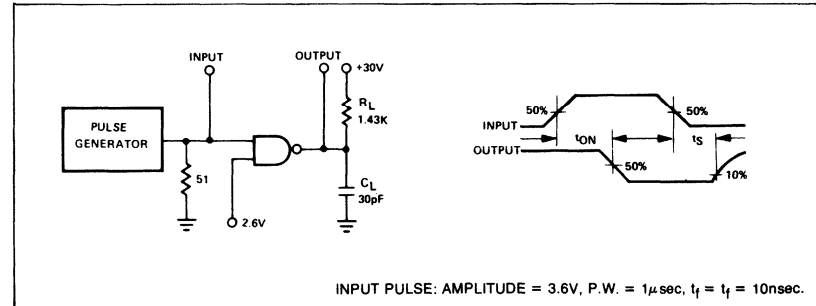
PIN CONFIGURATIONS



AC CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

CHARACTERISTIC	LIMITS			UNITS	TEST CONDITIONS
	MIN.	TYP.	MAX.		
Turn-on Delay		35	55	ns	$R_L = 1.43K$
Storage Time		40	95	ns	$C_L = 30pF$

AC TEST FIGURE AND WAVEFORMS



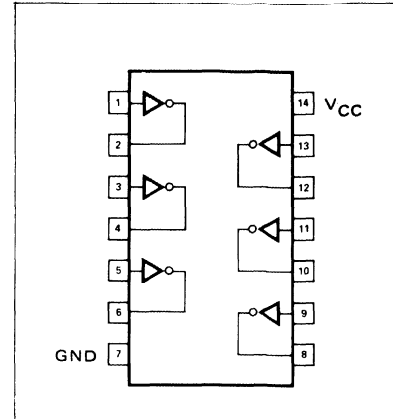
OBJECTIVE SPECIFICATION DESCRIPTION

The 8T93 Hex Inverter interface elements have been designed with Schottky TTL technology. This makes it possible to combine ultra-high speed with a low current PNP input structure. Because of its low input current requirements the 8T93 is ideal in applications such as bus receivers, low power TTL interfaces as well as MOS and C-MOS to TTL buffers. The 8T93 has active pullups.

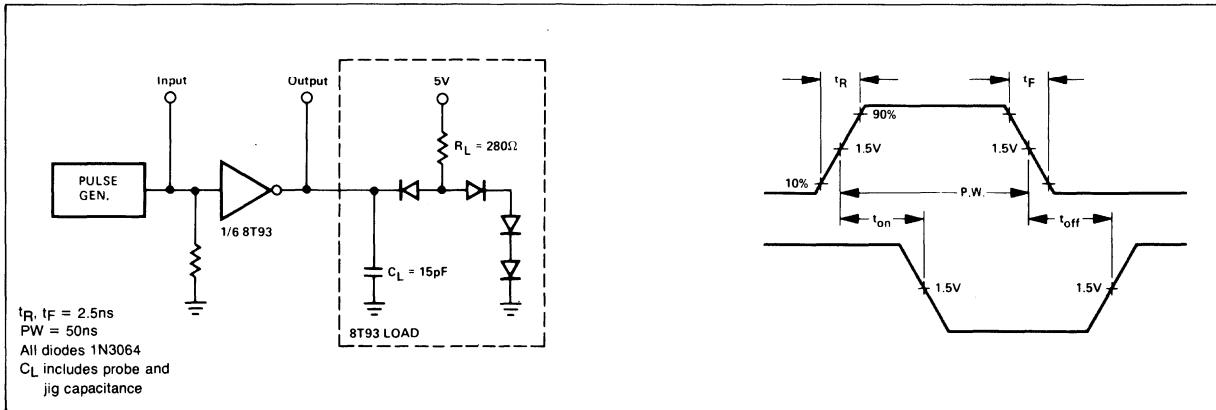
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5V$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Propagation Delay t_{on}, t_{off}	$R_L = 280$ $C_L = 15 \text{ pF}$		5		ns

PIN CONFIGURATION



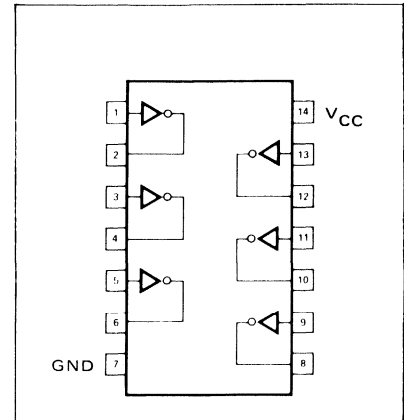
AC TEST FIGURE AND WAVEFORMS



OBJECTIVE SPECIFICATION DESCRIPTION

The 8T94 Hex Inverter interface elements have been designed with Schottky TTL technology. This makes it possible to combine ultra-high speed with a low current PNP input structure. Because of its low input current requirements the 8T94 is ideal in applications such as bus receivers, low power TTL interfaces as well as MOS and C-MOS to TTL buffers.

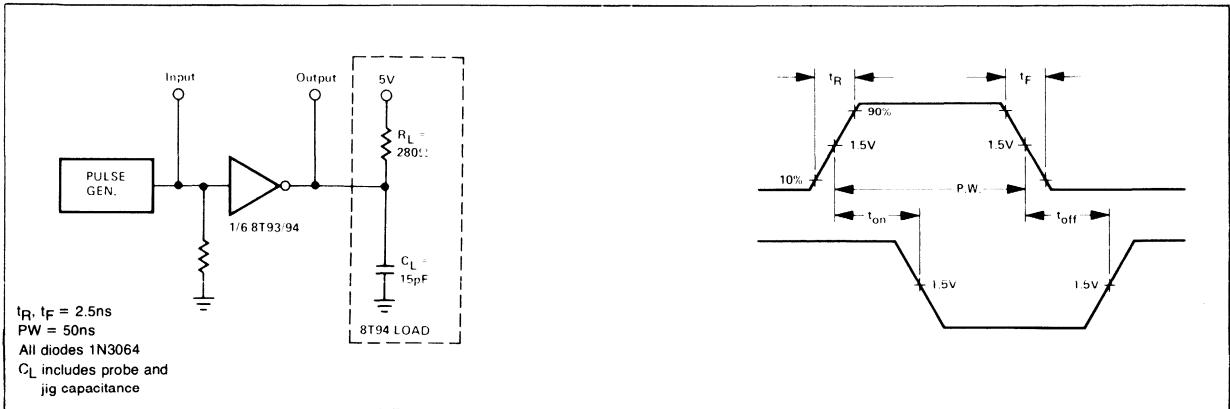
PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5V$

PARAMETER	TEST CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay t_{on}, t_{off}	$R_L = 280$ $C_L = 15 \text{ pF}$		6		ns

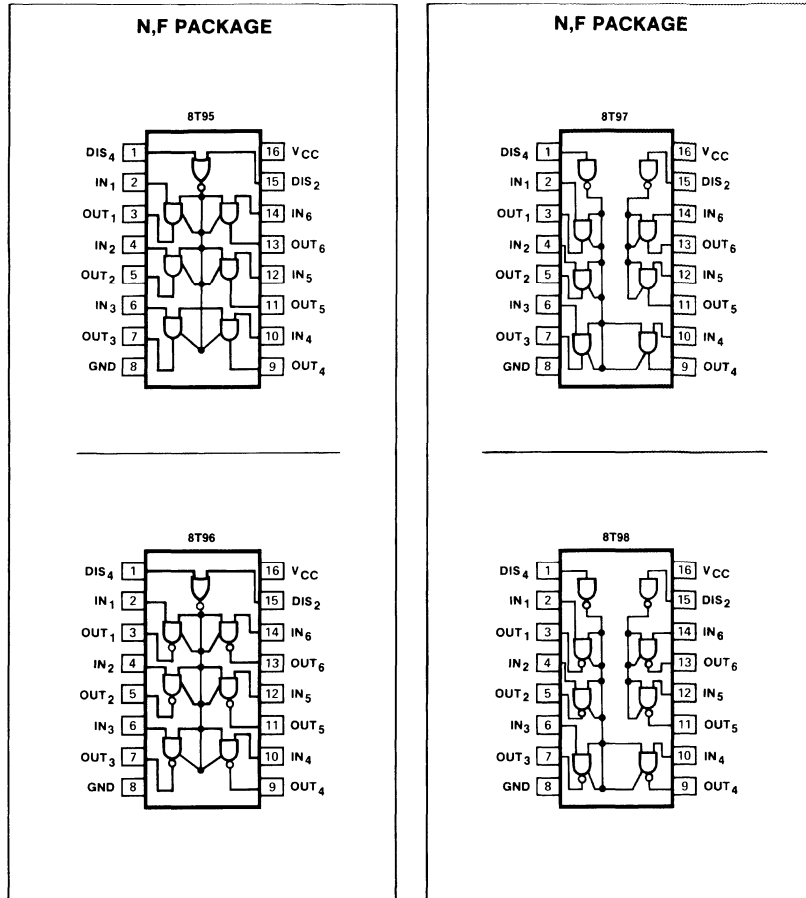
AC TEST FIGURE AND WAVEFORMS



DESCRIPTION

Each of the 3-State Bus Interface Elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to 3-state TTL Bus levels. For maximum systems flexibility the 8T95 and 8T97 do so without logic inversion, whereas, the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas, the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

PIN CONFIGURATIONS



TRUTH TABLE

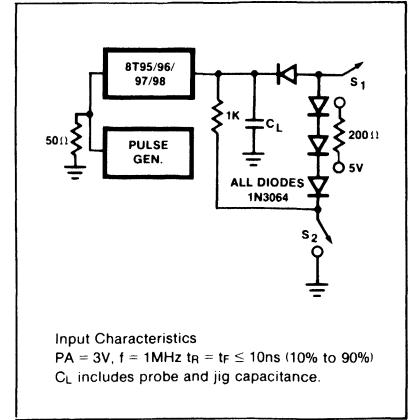
DEVICE	DISABLE DIS ₁	DISABLE DIS ₄	INPUT DIS ₂	INPUT	OUTPUT
8T95	0	—	0	0	0
	0	—	0	1	1
	0	—	0	x	H-z
	1	—	0	x	H-z
8T96	0	—	0	0	1
	0	—	0	1	0
	0	—	1	x	H-z
	1	—	0	x	H-z
8T97	—	0	0	0	0
	—	0	0	1	1
	—	x	1	x	H-z*
	—	1	x	x	H-z**
8T98	—	0	0	0	1
	—	0	0	1	0
	—	x	1	x	H-z*
	—	1	x	x	H-z**

*Output 5-6 only **Output 1-4 only x = irrelevant

DC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage					
V _{IL} Low		2.0		0.8	V
V _{IH} High					V
V _{IC} Clamp	V _{CC} = MIN, I _{IN} = -12mA				V
Input				-1.5	V
Output to ground				-1.5	V
Output voltage					V
V _{OL}	V _{CC} = MIN I _{OL} = 48mA			0.5	V
V _{OH}	I _{OH} = 5.2mA	2.4			V
Input current	V _{CC} = MAX, V _{IN} = 0.5V				μA
I _{IL} Low	D _{IS} = 0.5V			-400	μA
	D _{IS} = 2.0V (third state)			-40	μA
I _{IH} High	V _{IN} = 2.4V			40	μA
I _{OS} Short circuit output current	V _{CC} = MAX, V _{IN} = 0V, V _{OUT} = 0V	-40	-80	-115	μA

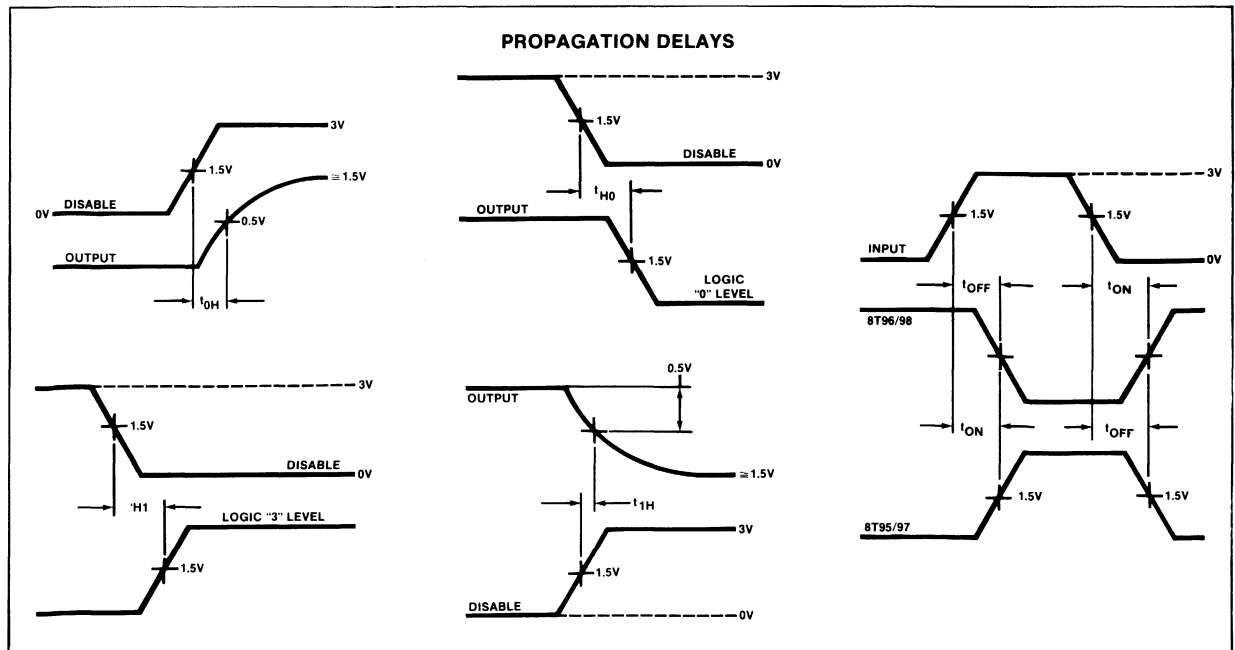
AC TEST CIRCUIT



AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TO	FROM	TEST CONDITIONS	8T95/97			8T96/98			UNIT
				Min	Typ	Max	Min	Typ	Max	
Propagation delay										
t _{ON}	Outputs	Inputs		3	9	13	3	6	10	ns
t _{OFF}	Outputs	Inputs		3	7	12	4	7	11	ns
Disable to Outputs										
t _{POH}	High Z	Low	S ₁ , S ₂ are closed, C _L = 5pF	3	6	12	5	10	16	ns
t _{PLH}	High Z	High	S ₁ , S ₂ are closed, C _L = 5pF	3	5	10	3	6	10	ns
t _{PHO}	Low	High Z	S ₁ is closed, S ₂ is open; C _L = 50pF	12	14	25	11	18	24	ns
t _{PHL}	High	High Z	S ₁ is open, S ₂ is closed; C _L = 50pF	8	19	25	7	15	22	ns

PARAMETER MEASUREMENT INFORMATION



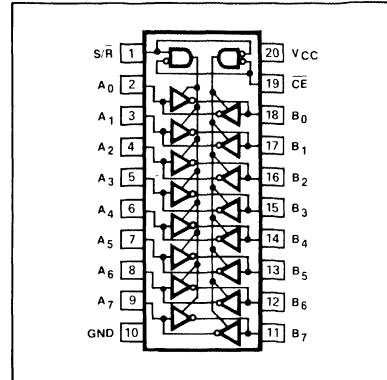
DESCRIPTION

The 8T125 is an Octal Transceiver featuring inverting 3-state bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA producing very good capacitive drive characteristics. The device features a Chip Enable input for easy cascading and a Send/Receive input for direction control. All inputs have hysteresis built in to minimize ac noise effects.

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all inputs
- Pin compatible with 54LS/74LS245

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^{\circ}C$ to $+70^{\circ}C$	MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N8T125N	
Ceramic DIP	N8T125F	S8T125F
Flatpak		

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/ \overline{R}	A_n	B_n
L	L	$A = \overline{B}$	INPUTS
L	H	INPUT	$B = \overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance "off" state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		LIMITS
\overline{CE}	Chip Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)	20 -0.2
S/ \overline{R}	Send/Receive control input	I_{IH} (μA) I_{IL} (mA)	20 -0.2
A_0 - A_7	A inputs	I_{IH} (μA) I_{IL} (mA)	20 -0.2
B_0 - B_7	B inputs	I_{IH} (μA) I_{IL} (mA)	20 -0.2
A_0 - A_7	3-State outputs	I_{OH} (mA) I_{OL} (mA)	-2 / -5.2 ^(a) 12 / 24 ^(a)
B_0 - B_7	3-State outputs	I_{OH} (mA) I_{OL} (mA)	-2 / -5.2 ^(a) 12 / 24 ^(a)

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	LIMITS		UNIT	
			Min	Max		
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		V	
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		0.8	V	
V _{CD}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-1.5	V	
V _{OH}	Output HIGH voltage	V _{CC} = Min,	I _{OH} = -2.0mA Mil	2.4	V	
			I _{OH} = -5.2mA Com	2.4	V	
			I _{OH} = -12mA Mil	2.0	V	
			I _{OH} = -15mA Com	2.0	V	
V _{OL}	Output LOW voltage	V _{CC} = Min,	I _{OL} = 12mA Mil & Com		0.4	V
			I _{OL} = 24mA Com		0.5	V
I _{OZH}	Output "off" current HIGH	V _{CC} = Max, V _{OUT} = 2.4V		20	μA	
I _{OZL}	Output "off" current LOW	V _{CC} = Max, V _{OUT} = 0.4V		-200	μA	
I _{IH}	Input HIGH current	V _{CC} = Max, V _{IN} = 2.4V		20	μA	
I _I	Input breakdown current	V _{CC} = Max, V _{IN} = 5.5V		100	μA	
I _{IL}	Input LOW current	V _{CC} = Max, V _{IN} = 0.4V		-200	μA	
I _{OS}	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-40	-120	mA	
I _{CCH}	Supply current HIGH	V _{CC} = Max, outputs HIGH		70	mA	
I _{CCL}	Supply current LOW	V _{CC} = Max, outputs LOW		90	mA	
I _{CCZ}	Supply current "off"	V _{CC} = Max, outputs "off"		95	mA	

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t _{PLH}	Propagation delay	Waveform 1 C _L = 45pF, R _L = 667Ω		12	ns
t _{PHL}	Input to output			12	ns
t _{PZH}	Enable to HIGH	Waveform 6 C _L = 45pF, R _L = 667Ω		40	ns
t _{PZL}	Enable to LOW	Waveform 7 C _L = 45pF, R _L = 667Ω		40	ns
t _{PHZ}	Disable from HIGH	Waveform 6 R _L = 667Ω	C _L = 45pF	35	ns
			C _L = 5pF(b)	18	ns
t _{PLZ}	Disable from LOW	Waveform 7 R _L = 667Ω	C _L = 45pF	30	ns
			C _L = 5pF(b)	25	ns

NOTE

b. These tests are for reference only. They represent the delay time to guarantee that a device is disabled and can no longer drive the bus.

DESCRIPTION

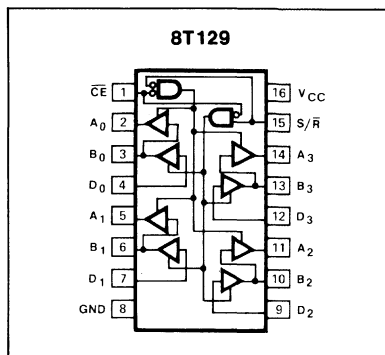
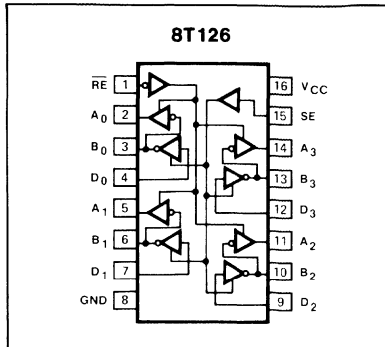
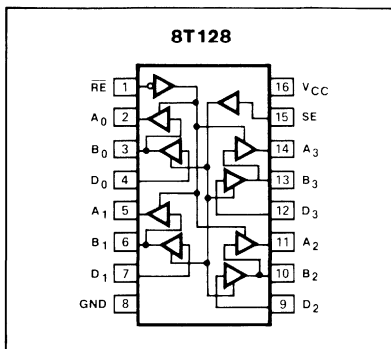
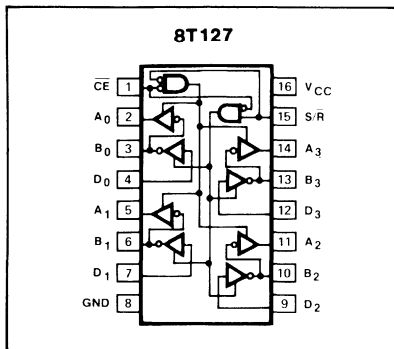
The 8T126 thru 8T129 are quad transceivers designed to handle many bus interface applications. The devices feature 3-state outputs on both send and receive buffers, and pnp transistors on all inputs to reduced input LOW loading requirements.

The 8T126 and 8T128 feature a 3.4V minimum V_{OH} level on the receiver for MOS in-

terface applications. The send and receive buffers have separate enable inputs for independent control.

The 8T127 and 8T129 feature full 24mA drive in both send and receive buffers. These devices have a common Chip Enable input for easy cascading, and a Send/Receive input for direction control.

PIN CONFIGURATIONS



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%$; $T_A=0^\circ C$ to $+70^\circ C$		MILITARY RANGES $V_{CC}=5V \pm 10\%$; $T_A=-55^\circ C$ to $+125^\circ C$	
	Plastic DIP	N8T126N	• N8T127N	
	N8T128N	• N8T129N		
Ceramic DIP	N8T126F	• N8T127F	S8T126F	• S8T127F
	N8T128F	• N8T129F	S8T128F	• S8T129F
Flatpak			S8T126W	• S8T127W
			S8T128W	• S8T129W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE^(a)

PINS	DESCRIPTION		8T126	8T127	8T128	8T129
\overline{RE}	Receive Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)	20 -0.1		20 -0.1	
SE	Send Enable (active HIGH) input	I_{IH} (μA) I_{IL} (mA)	20 -0.1		20 -0.1	
\overline{CE}	Chip Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)		20 -0.2		20 -0.2
S/\overline{R}	Send/Receive control input	I_{IH} (μA) I_{IL} (mA)		20 -0.2		20 -0.2
D_0 - D_3	Data inputs	I_{IH} (μA) I_{IL} (mA)	20 -0.1	20 -0.2	20 -0.1	20 -0.2
B_0 - B_3	Bus inputs	I_{IH} (μA) I_{IL} (mA)	20 -0.1	20 -0.2	20 -0.1	20 -0.2
B_0 - B_3	3-State bus outputs	I_{OH} (mA) I_{OL} (mA)	-2/-5.2(a) 12/24(a)	-2/-5.2(a) 12/24(a)	-2/-5.2(a) 12/24(a)	-2/-5.2(a) 12/24(a)
A_0 - A_3	3-State receiver outputs	I_{OH} (mA) I_{OL} (mA)	-1/-2.6(a) 6/12(a)	-2/-5.2(a) 12/24(a)	-1/-5/2(a) 6/12(a)	-2/-5.2(a) 12/24(a)

NOTE

a. The slashed numbers indicate different parametric values for Military Commercial temperature ranges respectively.

FUNCTION TABLE (8T126)

INPUTS			RECVR. OUT	BUS I/O
SE	RE	D _n	A _n	B _n
L	L	X	A = \bar{B}	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	H
H	H	H	(Z)	L
H	L	L	L	H
H	L	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance "off" stage

FUNCTION TABLE (8T128)

INPUTS			RECVR. OUT	BUS I/O
SE	RE	D _n	A _n	B _n
L	L	X	A = B	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	L
H	H	H	(Z)	H
H	L	L	L	L
H	L	H	H	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance "off" stage

FUNCTION TABLE (8T127)

INPUTS			RECVR. OUT	BUS I/O
CE	S/R	D _n	A _n	B _n
L	L	X	A = \bar{B}	INPUTS
L	H	L	(Z)	H
L	H	H	(Z)	L
H	X	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance "off" stage

FUNCTION TABLE (8T129)

INPUTS			RECVR. OUT	BUS I/O
CE	S/R	D _n	A _n	B _n
L	L	X	A = B	INPUTS
L	H	L	(Z)	L
L	H	H	(Z)	H
H	X	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = High impedance "off" stage

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	8T126/8T128		8T127/8T129		UNIT
		Min	Max	Min	Max	
t _{PLH}	Propagation delay		20		20	ns
t _{PHL}	Data to bus output		30		30	ns
t _{PLH}	Propagation delay bus to receiver output		20		20	ns
t _{PHL}			30		25	ns
t _{PZH}	Enable to HIGH for bus output		30		35	ns
t _{PZH}	Enable to HIGH for receiver output		25		30	ns
t _{PZL}	Enable to LOW for bus output		35		35	ns
t _{PZL}	Enable to LOW for receiver output		30		30	ns
t _{PHZ}	Disable from HIGH		25		25	ns
t _{PLZ}	Disable from LOW		25		25	ns

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	8T126/8T128		8T127/8T129		UNIT		
		Min	Max	Min	Max			
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		2.0	V	
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		Mil		0.7	V	
				Com		0.8	0.8	V
V _{CD}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA			-1.5		-1.5	V
V _{OH}	Output HIGH voltage for Bus outputs	V _{CC} = Min,	I _{OH} = -2.0mA Mil	2.4		2.4	V	
			I _{OH} = -5.2mA Com	2.4		2.4	V	
V _{OH}	Output HIGH voltage Receiver outputs	V _{CC} = Min, V _{IN} = V _{IL} or V _{IH} per Truth Table	I _{OH} = -100μA Mil	3.1			V	
			I _{OH} = -100μA Com	3.4			V	
			I _{OH} = -1.0mA Mil	2.4			V	
			I _{OH} = -2.0mA Mil			2.4	V	
			I _{OH} = -2.5mA Com	2.4			V	
			I _{OH} = -5.2mA Com			2.4	V	
V _{OL}	Output LOW voltage for Bus outputs	V _{CC} = Min,	I _{OL} = 12mA Mil & Com		0.4		0.4	V
			I _{OL} = 24mA Com		0.5		0.5	V
V _{OL}	Output LOW voltage for Receiver outputs	V _{CC} = Min,	I _{OL} = 6mA Mil & Com		0.4		V	
			I _{OL} = 12mA Mil & Com			0.4	V	
			I _{OL} = 12mA Com		0.5		V	
			I _{OL} = 24mA Com			0.5	V	
I _{OZH}	Output "off" current HIGH	V _{CC} = Max, V _{OUT} = 2.4V			20		20	μA
I _{OZL}	Receiver "off" current LOW	V _{CC} = Max, V _{OUT} = 0.4V			-20		-20	μA
I _{OZL}	Bus "off" current LOW	V _{CC} = Max, V _{OUT} = 0.4V			-100		-200	μA
I _{IH}	Input HIGH current	V _{CC} = Max, V _{IN} = 2.7V			20		20	μA
I _I	Input breakdown current	V _{CC} = Max,	Bus inputs V _{IN} = 5.5V		100		100	μA
			others V _{IN} = 10V		100		100	μA
I _{IL}	Input LOW current	V _{CC} = Max, V _{IN} = 0.4V			-100		-200	μA
I _{OS}	Output short circuit current	V _{CC} = Max, V _{OUT} = 0V		-40	-120	-40	-120	mA
I _{CCH}	Supply current HIGH	V _{CC} = Max, outputs HIGH			26		36	mA
I _{CCL}	Supply current LOW	V _{CC} = Max, outputs LOW			30		42	mA
I _{CCZ}	Supply current "off"	V _{CC} = Max, outputs "off"			36		44	mA

DESCRIPTION

The 8T363 Dual Zero Crossing Detector is an interface circuit incorporating a differential amplifier input and logic gate output. The input amplifier is referenced to zero volts and employs temperature compensation to ensure stable thresholds. The output structure of the 8T363 is compatible with DTL and TTL circuits.

APPLICATIONS

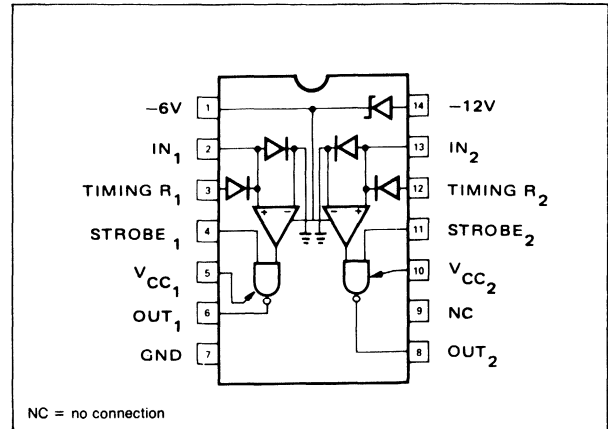
- Zero-Crossing Detector
- High Stability One-Shot
- Bi-Directional One-Shot
- Frequency Doubler
- Stable-Low Frequency Oscillator
- Linear Amplifier
- Frequency to Voltage Converter

ABSOLUTE MAXIMUM RATINGS

Input Voltage	+7.0V
Output Voltage	+6.0V
V _{CC}	+6.0V
Input Current	± 10mA
Output Current	+30, -10mA
Storage Temperature	-65° C to +175° C
Operating Temperature	0° C to +75° C
V ⁻	-7V or -13.5V

Maximum ratings are limiting values above which serviceability may be impaired.

PIN CONFIGURATION



AC ELECTRICAL CHARACTERISTICS T_A = 25° C, V_{CC} = 5.0V, V⁻ = -6V

PARAMETER	TEST CONDITIONS	MAX	UNITS
Turn on Delay Detector Strobe to Output	See Test Figure 1, T _A = 25° C	85	ns
	See Test Figure 2, V signal = V _{CC} through 10KΩ resistor, T _A = 25° C	50	ns
Turn off Delay Detector Strobe to Output	See Test Figure 1, T _A = 25° C	65	ns
	See Test Figure 2, V signal = V _{CC} through 10KΩ resistor, T _A = 25° C	50	ns
Input Voltage (Timing R V _F Diode)	V ₇ = V ₂ = V ₁₃ , I ₃ = 1mA, I ₁₂ = 1mA	1	V
Uncertainty Region-Signal		±30	mV
I _{cc} /Detector	V ₇ = V ₃ = V ₁₂ , Note 9, T _A = 25° C	6.5	mA
I _{EE}		-13.0	mA

CIRCUIT SCHEMATIC

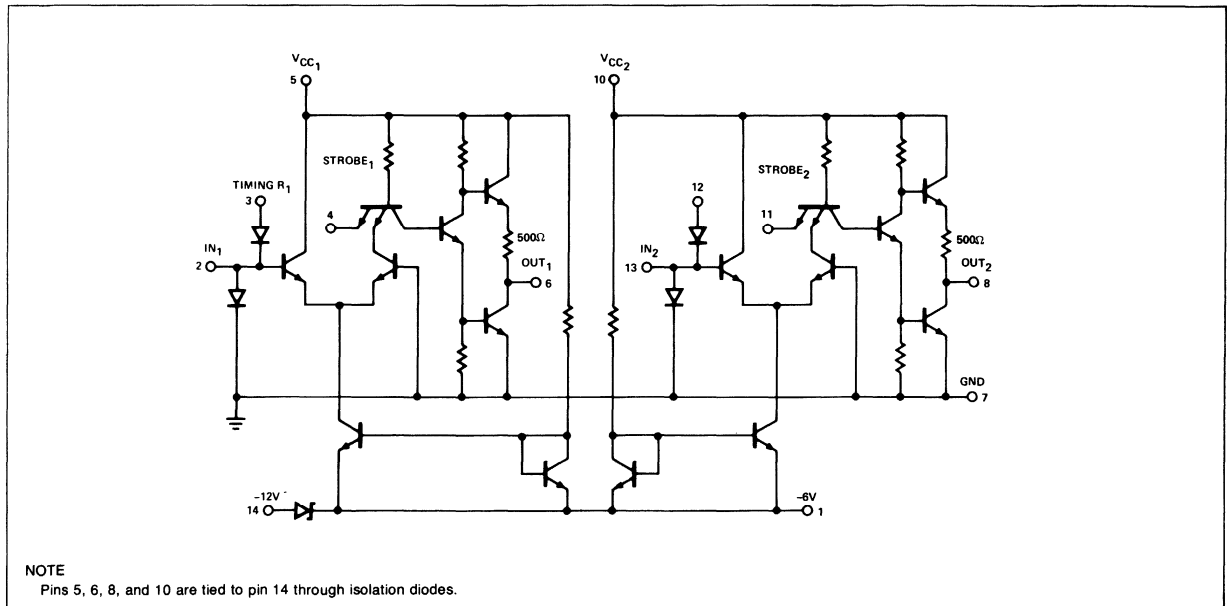
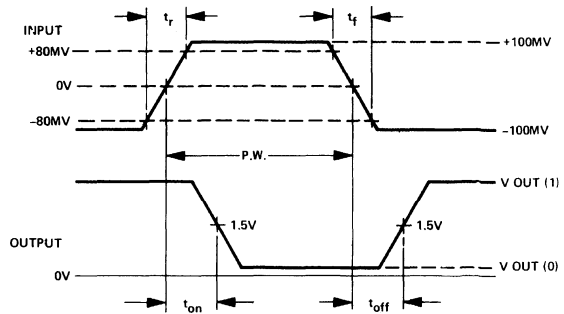
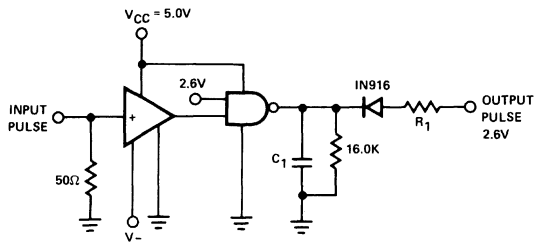


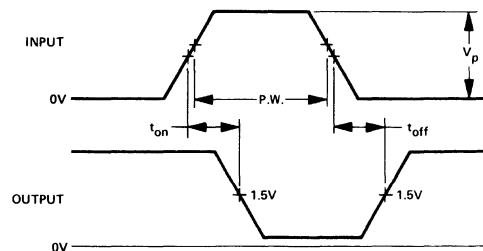
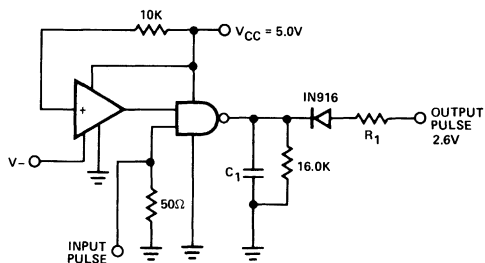
FIGURE 1 – t_{on} , t_{off} DETECTOR INPUTS



t_{on}	t_{off}
$C_1 = 27\text{pF}$	18pF
$R_1 = 210\Omega$	$1.91\text{k}\Omega$

Input Pulse: V_{in}
 Pulse Width = 350ns at 50% Points
 $t_r = t_f = 10\text{ns}$
 Amplitude = $\pm 100\text{mV}$

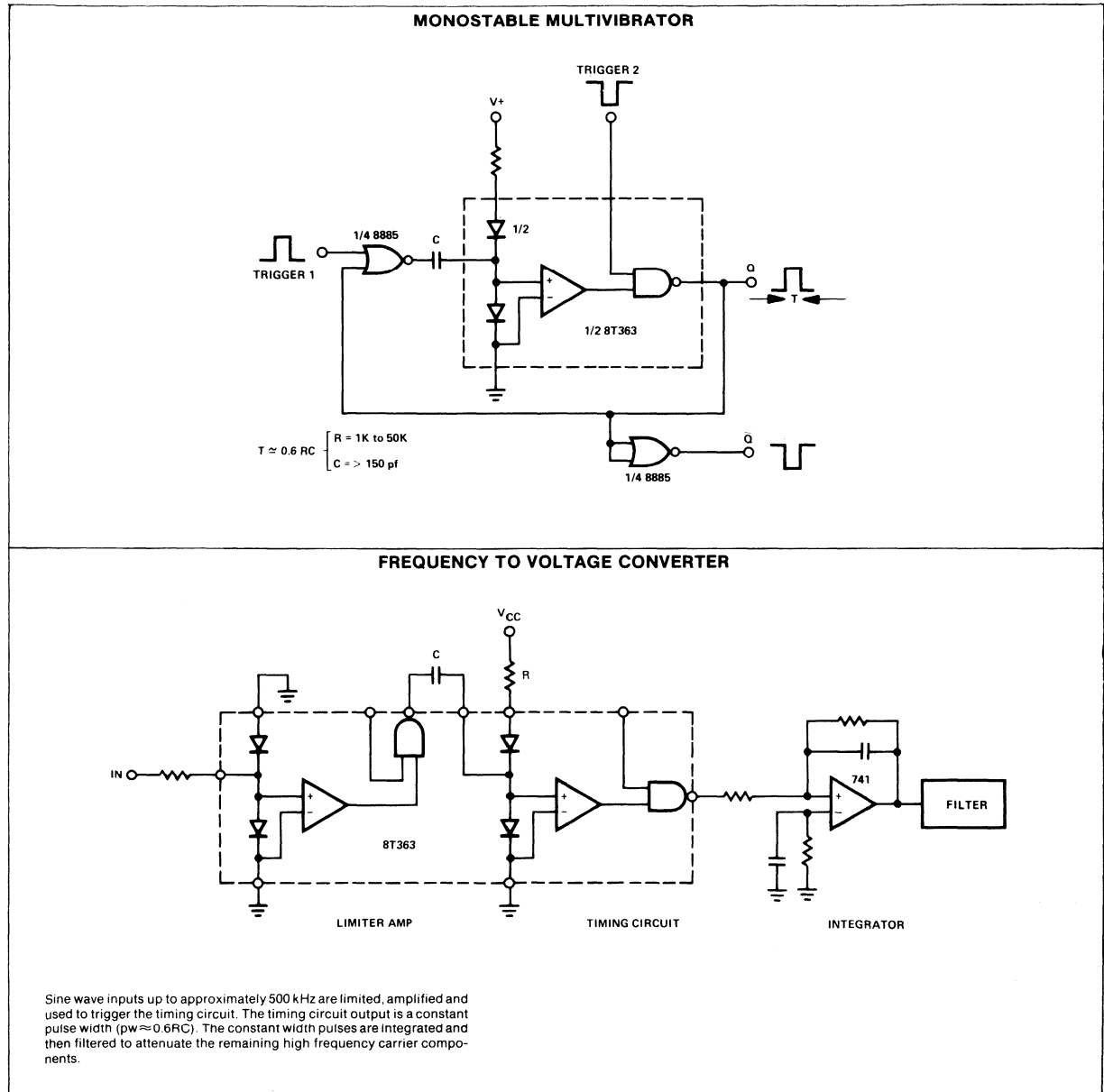
FIGURE 2 – t_{on} , t_{off} STROBE TO OUTPUT



t_{on}	t_{off}
$C_1 = 27\text{pF}$	18pF
$R_1 = 210\Omega$	$1.91\text{k}\Omega$

Input Pulse: V_{in}
 Pulse width = 200ns at 50% Points
 $t_r = t_f$ (10%-90%) = 10ns
 Amplitude $V_p = 4.0\text{V}$

TYPICAL APPLICATIONS

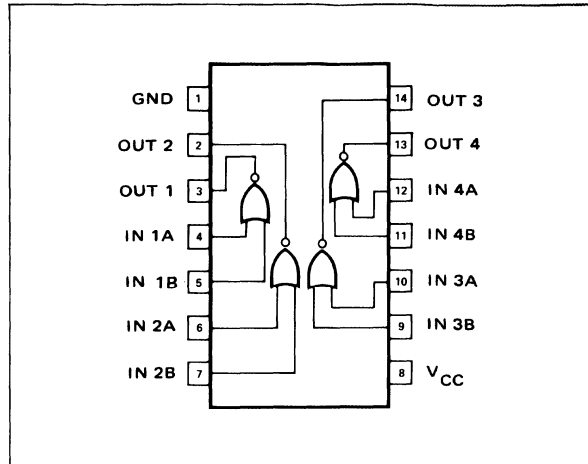


DESCRIPTION

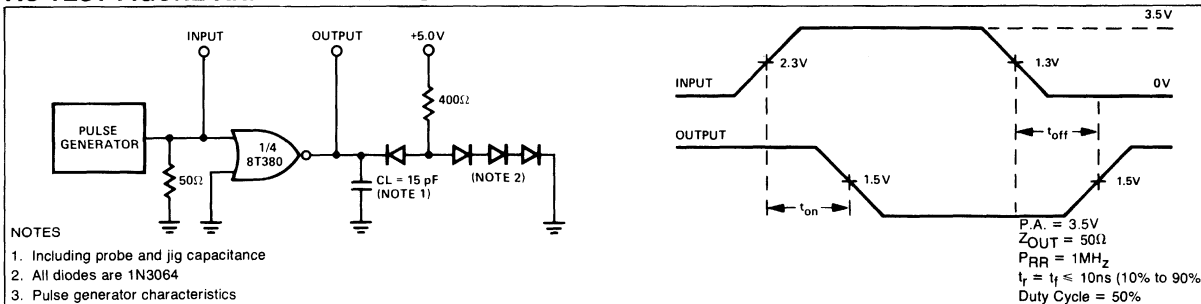
The 8T380 is a quad 2-input bus receiver with hysteresis for use in I/O, data, and memory busses. Built in hysteresis provides maximum noise immunity and a power-up or power-down sequence on the receiver will not affect the bus. Low input current allows several drivers and receivers to communicate over a common bus in "Party Line" fashion. The receiver has been designed to be pincompatible with the Signetics Utilogic II SP 380 gate and provides increased noise immunity as well as lower input current. The 8T 380 is ideal as a Schmitt Trigger in analog interfaces that cannot tolerate the non-linear input impedance characteristics of standard TTL. Further, the low input requirements allow the 8T380 to be used as a CMOS to TTL interface. All inputs have clamping diodes to simplify systems design.

AC ELECTRICAL CHARACTERISTICS
 $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
t_{on} , Turn-on Delay		16	35	ns
t_{off} , Turn-off Delay		20	35	ns



AC TEST FIGURE AND WAVEFORMS



- NOTES
1. Including probe and jig capacitance
 2. All diodes are 1N3064
 3. Pulse generator characteristics

TYPICAL APPLICATIONS

A generalized "Party Line" bus interface is shown in Figure 1. Each driver/receiver combination can communicate with any other pair or all. Open collector Nand Gates such as the Signetics 7439 have adequate drive capability for the bus terminations as well as 20 driver/receiver pairs. In addition the bussing scheme is non-inverting as shown and bus drivers are activated by a logic "1" whereas bus receivers are activated by a Logic "0".

Each terminator consisting of a 180 ohm resistor to ground is a 120 ohm. Thevenin's equivalent circuit. The maximum length of cable that can be driven is a complex relationship involving the type of cable used as well as the distribution of drivers and receivers on the buss. Using flat ribbon cable, a maximum reasonable length is 50 ft. minus the combined length of all taps or stubs.

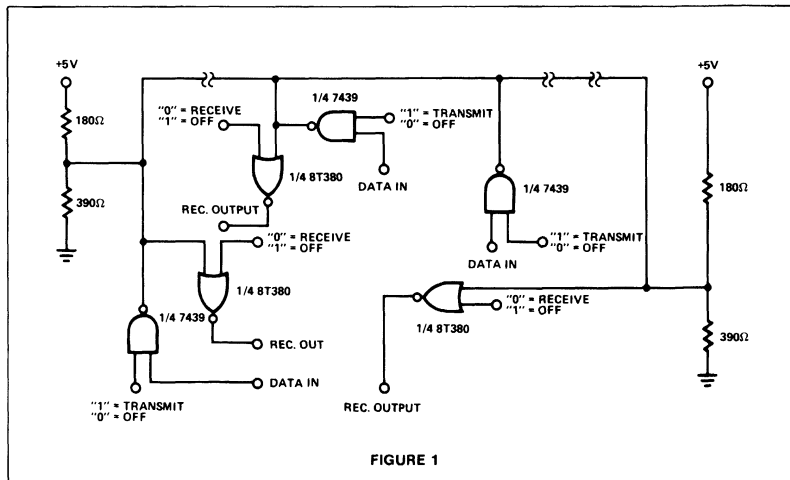


FIGURE 1

SCHMITT TRIGGER

The receiver transfer curve shown in Figure 2a makes the 8T380 ideal in a variety of Schmitt Trigger and waveshaping applications such as Figure 2b.

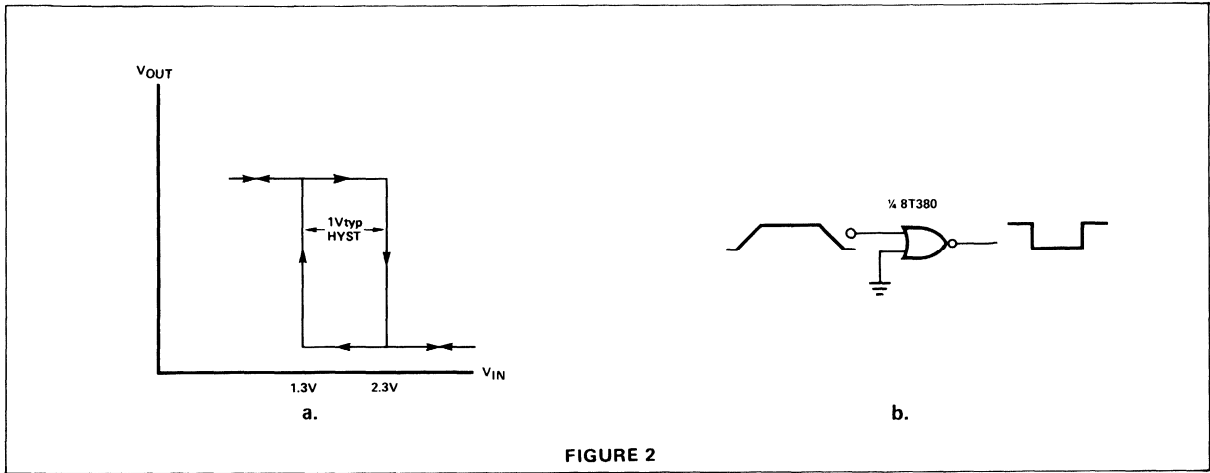


FIGURE 2

MOS/C-MOS INTERFACE

The low input current which is only $50\mu A$ max. in the logical "1" state and no current in the logical "0" state marks the 8T380 an ideal MOS/C-MOS interface element.

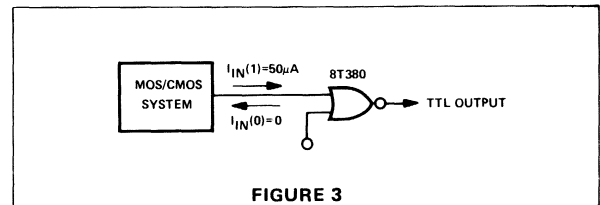


FIGURE 3

SECTION 8

Military Products

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics Mil 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customers to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3 and 4.

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

MIL-REL/883 (RB)

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES				
			Dual-In-Line		
	8-Pin	10-Pin	14-Pin	16-Pin	24-Pin
CB	—	—	F	—	—
EB	—	—	—	F	—
JB	—	—	—	—	I/F*
DB	—	—	W	—	—
FB	—	—	—	W	—
ZC	—	—	—	—	Q
GC	T	—	—	—	—
IC	—	K	—	—	—

*The gold plated versions of these packages will be available for a limited time. All products listed in Military section are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	JAN Qualified	/883	Mil Temp
54/54H	X	X	X
54LS	X	X	X
54S	X	X	X
82/8T	X	X	X
93XX	X	X	X
96XX	—	X	X
Linear	Planned	X	X
Bipolar Memory	Planned	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

883 Method 5004, and is 100% electrically tested to industry data sheets. MIL-REL/883B devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL TEMP/883C (S/RC)

If you need a Military temp. range device, but do not require all the high reliability screening performed in the other processing options, our Mil-Temp. product is ideal. Mil-Temp. parts are the standard full Mil-Temperature range product guaranteed to a 1% AQL to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government

Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet
- Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

PROCESS LEVEL AND MARKING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFF SHORE
JB JM38510/XXXXX	883B	Yes	100%	100%	100%	Yes	No
RB SXXXX/883B	883B	Yes	100%	100%	100%	No	Yes
RC/S SXXXX/883C	883B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A* B	Electrical Test Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied.	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*

Group A is performed on each lot or subplot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS A	JAN Qualified (JB)	MIL Rel (RB)	/883C (RC)
General Mil-M-38510	The manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
1. Pre-Certification						
A. Product Assurance Program Plan						
B. Manufacturer's Certification						
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Pre-cap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling*	1010, Cond. C; (10 cycles, -65°C to +150°C)	100%	X	X	X	X
*For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)						
9. Constant Acceleration	2001, Cond. E; (30kg in YI Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10 ⁻⁸ CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100%	X		N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ -55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS A	JAN Qualified (JB)	MIL Rel (RB)	/883C (RC)
D. Dynamic Test @ 25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @ 25°C		Sub Group 7	X	X	X	X
F. Switching Test @ 25°C		Sub Group 9	X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @ 25°C (A-1). This is controlled by the slash sheets for JB & JBX products. For RBX & RB 10% is standard.	10%	5%	X	X	N/A
16. Marking		Fungus Inhibiting Paint	100%	As Req'd	JM38510/ XXXX Slash Sheet #	M38510/ SXXXX Sig. Basic #
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std-883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per microcircuit group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constant acceleration.	Every 3 months per package type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS (Cont'd)

BIPOLAR MEMORY CROSS REFERENCE

DEVICE	ORGANIZATION	PACKAGE*		OUTPUT CIRCUIT	NUMBER OF PINS
PROMs					
82S23	32X8	F	R	OC	16
82S115	512X8	I	R	TS	24
82S123	32X8	F	R	TS	16
82S126	256X4	F	R	OC	16
82S129	256X4	F	R	TS	16
82S130	512X4	F	R	OC	16
82S131	512X4	F	R	TS	16
82S136	1024X4	F,I	R	OC	18
82S137	1024X4	F,I	R	TS	18
82S140	512X8	I	R	OC	24
82S141	512X8	I	R	TS	24
82S180	1024X8	I	R	OC	24
82S181	1024X8	I	R	TS	24
82S184	2048X4	I	R	OC	18
82S185	2048X4	I	R	TS	18
82S2708	1024X8	I	R	TS	24
FPLAs					
82S100	16X48X8	I	R	TS	28
82S101	16X48X8	I	R	OC	28
82S102	16X9	I	R	OC	28
82S103	16X9	I	R	TS	28
PLAs					
82S200	16X48X8	I	R	TS	28
82S201	16X48X8	I	R	OC	28
RAMs					
3101A	16X4	F	R	OC	16
54S89	16X4	F	R	OC	16
54S189	16X4	F	R	TS	16
54S200	256X1	F	R	TS	16
54S201	256X1	F	R	TS	16
54S301	256X1	F	R	OC	16
82S09	64X9	I	R	TS	28
82S10	1024X1	F,I	R	OC	16
82S11	1024X1	F,I	R	TS	16
82S16	256X1	F	R	TS	16
82S17	256X1	F	R	OC	16
82S25	16X4	F	R	OC	16
ROMs					
82S215	512X8	I	R	TS	24
82S223	32X8	F	R	OC	16
82S224	32X8	F	R	TS	16
82S226	256X4	F	R	OC	16
82S229	256X4	F	R	TS	16
82S230	512X4	F	R	OC	16
82S231	512X4	F	R	TS	16
82S280	1024X8	I	R	OC	24
82S281	1024X8	I	R	TS	24
82S290	2048X8	I	R	OC	24
82S291	2048X8	I	R	TS	24

*NOTE

R = BeO Flat Pack

F = Cerdip

I = Ceramic DIP

LOGIC—5400 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL*		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
5400	Quad 2-Input NAND Gate	/00104	1	1	F	W
5401	Quad 2-Input NAND Gate with o/c	/00107	1	1	F	W
5402	Quad 2-Input NOR Gate	/00401	1	1	F	W
5403	Quad 2-Input NAND Gate with o/c	/00109	1	—	F	—
5404	Hex Inverter	/00105	1	1	F	W
5405	Hex Inverter with o/c	/00108	1	1	F	W
5406	Hex Inverter w/Buffer/Driver with o/c	/00801	—	—	F	W
5407	Hex Buffer/Driver with o/c	/00803	—	—	F	W
5408	Quad 2-Input AND Gate	/01601	1	1	F	W
5409	Quad 2-Input AND Gate with o/c	/01602	1	1	F	W
5410	Triple 3-Input NAND Gate	/00103	1	1	F	W
5411	Triple 3-Input NAND Gate	—	—	—	F	W
5412	Triple 3-Input NAND Gate with o/c	/00106	—	—	F	W
5413	Dual NAND Schmitt Trigger	/15101	2	2	F	W
5414	Hex Schmitt Trigger	/15102	*	2	F	W
5416	Hex Inverter Buffer/Driver with o/c	/00802	—	—	F	W
5417	Hex Buffer/Driver with o/c	/00804	—	—	F	W
5420	Dual 4-Input NAND Gate	/00102	1	1	F	W
5421	Dual 4-Input AND Gate	—	—	—	F	W
5426	Quad 2-Input NAND Gate with o/c	/00805	1	—	F	—
5427	Triple 3-Input NOR Gate	/00404	1	1	F	W
5428	Quad 2-Input NOR Buffer	/16201	*	*	F	W
5430	8-Input NAND Gate	/00101	1	1	F	W
5432	Quad 2-Input OR Gate	/16101	2	2	F	W
5433	Quad 2-Input NOR Buffer with o/c	—	—	—	F	W
5437	Quad 2-Input NAND Buffer	/00302	1	1	F	W
5438	Quad 2-Input NAND Buffer with o/c	/00303	1	1	F	W
5439	Quad 2-Input NAND Buffer	—	—	—	F	W
5440	Dual 4-Input NAND Buffer	/00301	1	1	F	W
5442	BCD-to-Decimal Decoder	/01001	1	1	F	W
5443	Excess 3-to-Decimal Decoder	/01002	1	1	F	W
5444	Excess 3-Gray-to-Decimal Decoder	/01003	1	1	F	W
5445	BCD-to-Decimal Decoder/Driver with o/c	/01004	—	—	F	W
5446A	BCD-to-7 Segment Decoder/ Driver	/01006	—	—	F	W
5447A	BCD-to-7 Segment Decoder/ Driver	/01007	—	—	F	W
5448	BCD-to-7 Segment Decoder/ Driver	/01008	—	—	F	W
5450	Expandable Dual 2-Wide 2- Input A01	/00501	1	1	F	W
5451	Dual 2-Wide 2-Input A01 Gate	/00502	1	1	F	W
5453	4-Wide 2-Input A01 Gate (Expandable)	/00503	1	1	F	W
5454	4-Wide 2-Input A01 Gate	/00504	1	1	F	W
5455	2-Wide 4-Input A01 Gate	/04005	—	—	—	—

NOTE

Per OPL 38510-30 dated
1 September 1977
1 = Level 1 Qualification
2 = Level 2 Qualification
* = In process

LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL*		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
5460	Dual 4-Input Expander	—	—	—	F	W
5470	J-K Flip-Flop	/00206	1	1	F	W
5472	J-K Master-Slave Flip-Flop	/00201	1	1	F	W
5473	Dual J-K Master-Slave Flip-Flop	/00202	1	1	F	W
5474	Dual D-Type Edge-Triggered Flip-Flop	/00205	1	1	F	W
5475	Quad Bistable Latch	/01501	1	1	F	W
5476	Dual J-K Master-Slave Flip-Flop	/00204	1	1	F	W
5477	Quad Bistable Latch	/01502	—	—	F	W
5480	Gated Full Adder	—	—	—	F	W
5483	4-Bit Binary Full Adder	/00302	1	1	F	W
5485	4-Bit Magnitude Comparator	/15001	1	1	F	W
5486	Quad 2-Input Exclusive-OR Gate	/00701	1	1	F	W
5490	Decade Counter	/01307	*	*	F	W
5491	8-Bit Shift Register	—	—	—	F	W
5492	Divide-by-Twelve Counter	/01301	1	1	F	W
5493	4-Bit Binary Counter	/01302	1	1	F	W
5494	4-Bit Shift Register (PISO)	—	—	—	F	W
5495	4-Bit Left-Right Shift Register	/00901	1	1	F	W
5496	5-Bit Shift Register	/00902	1	1	F	W
54100	4-Bit Bistable Latch (Dual)	—	—	—	F	W
54107	Dual J-K Master-Slave Flip-Flop	/00203	1	—	F	—
54109	Dual J-K Positive Edge- Triggered Flip-Flop	—	—	—	F	W
54116	Dual 4-Bit Latch with Clear	/01503	2	—	I	—
54121	Monostable Multivibrator	/01201	1	1	F	W
54122	Retriggerable Monostable Multivibrator	/01202	—	—	—	—
54123	Retriggerable Monostable Multivibrator	/01202	1	1	F	W
54128	Quad Bus Buffer Gate w/Tri-State Outputs	/15101	2	2	F	W
54129	Quad Bus Buffer Gate w/Tri-State Outputs	/15102	2	2	F	W
54128	Quad 2-Input NOR Buffer	—	—	—	F	W
54132	Quad Schmitt Trigger	/15103	*	2	F	W
54145	BCD-to-Decimal Decoder/Driver with o/c	/01005	—	—	F	W
54147	10-Line to 4-Line Priority Encoder	/15601	*	*	F	W
54148	8-Line to 3-Line Priority Encoder	/15602	2	2	F	W
54150	16-Line to 1-Line Mux	/01401	2	—	I	—
54151	8-Line to 1-Line Mux	/01406	1	1	F	W
54152	8-Line to 1-Line Mux	—	—	—	F	W
54153	Dual 4-Line to 1-Line Mux	/01403	1	1	F	W
54154	4-Line to 16-Line Decoder/ Demux	/15201	2	—	I	—
54155	Dual 2-Line to 4-Line Decoder/Demux	/15202	—	—	F	W
54156	Dual 2-Line to 4-Line Decoder/Demux	/15203	—	—	F	W
54157	Quad 2-Input Data Selector (non-inv.)	/01405	1	1	F	W
54158	Quad 2-Input Data Selector (inv.)	—	—	—	F	W
54160	Synchronous 4-Bit Decade Counter	/01303	1	1	F	W

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LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
54161	Synchronous 4-Bit Binary Counter	/01306	1	1	F	W
54162	Synchronous 4-Bit Decade Counter	/01305	1	1	F	W
54163	Synchronous 4-Bit Binary Counter	/01304	1	1	F	W
54164	8-Bit Parallel-Out Serial Shift Register	/00903	1	—	F	—
54165	Parallel-Load 8-Bit Shift Register	/00904	*	*	F	W
54166	8-Bit Shift Register	—	—	—	F	—
54170	4X4 Register File	/01801	—	—	—	—
54174	Hex D-Type Flip-Flop with Clear	/01701	1	1	F	W
54175	Quad D-Type Edge-Triggered Flip-Flop	/01702	1	1	F	W
54180	8-Bit Odd/Even Parity Checker	/01901	1	1	F	W
54181	4-Bit Arithmetic Logic Unit	/01101	1	—	I	—
54182	Look-Ahead Carry Generator	/01102	1	1	F	W
54190	Synchronous Up/Down Counter (BCD)	—	—	—	*	*
54191	Synchronous Up/Down Counter (Binary)	—	—	—	*	*
54192	Synchronous Decade Up/Down Counter	/01308	*	*	F	W
54193	Synchronous 4-Bit Binary Up/Down Counter	/01309	*	*	F	W
54194	4-Bit Bidirectional Universal Shift Register	/00905	*	*	F	W
54195	4-Bit Parallel-Access Shift Register	/00906	*	*	F	W
54198	8-Bit Shift Register	—	—	—	I	Q
54199	8-Bit Shift Register	—	—	—	—	—
54221	Dual Monostable Multivibrator	—	—	—	F	W
54279	Quad S-R Latch	—	—	—	F	W
54298	Quad 2-Input Mux with Storage	—	—	—	F	W
54365	Hex Buffer w/Common Enable (3-State)	/16301	*	*	*	*
54366	Hex Buffer w/Common Enable (3-State)	/16302	*	*	F	W
54367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16303	*	*	F	W
54368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16304	*	*	F	W

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LOGIC—54H SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
54H00	Quad 2-Input NAND Gate	/02304	1	1	F	W
54H01	Quad 2-Input NAND Gate with o/c	/02306	1	1	F	W
54H04	Hex Inverter	/02305	1	1	F	W
54H05	Hex Inverter with o/c	—	—	—	F	W
54H08	Quad 2-Input AND Gate	/15501	1	—	F	W
54H10	Triple 3-Input NAND Gate	/02303	1	1	F	W
54H11	Triple 3-Input NAND Gate	/15502	1	—	F	W
54H20	Dual 4-Input NAND Gate	/02302	1	1	F	W
54H21	Dual 4-Input AND Gate	/15503	1	—	F	W
54H22	Dual 4-Input NAND Gate with o/c	/02307	1	—	F	W
54H30	8-Input NAND Gate	/02301	1	1	F	W
54H40	Dual 4-Input NAND Buffer	/02401	1	1	F	W
54H50	Expandable Dual 2-Wide 2-Input A01	/04001	1	1	F	W
54H51	Dual 2-Wide 2-Input A01 Gate	/04002	1	1	F	W
54H52	Expandable 4-Wide 2-2-2-3 Input AND-OR Gate	—	—	—	F	W
54H53	4-Wide 2-Input A01 Gate (Expandable)	/04003	1	1	F	W
54H54	4-Wide 2-Input A01 Gate	/04004	1	1	F	W
54H55	2-Wide 2-Input A01 Gate	/04005	1	1	F	W
54H60	Dual 4-Input Expander	—	—	—	F	W
54H61	Triple 3-Input Expander	—	—	—	F	W
54H62	3-2-2-3 Input AND-OR Expander	—	—	—	F	W
54H71	J-K Master-Slave Flip-Flop with AND-OR Inputs	—	—	—	F	W
54H72	J-K Master-Slave Flip-Flop	/02201	1	1	F	W
54H73	Dual J-K Master-Slave Flip-Flop	/02202	1	1	F	W
54H74	Dual D-Type Edge-Triggered Flip-Flop	/02203	1	1	F	W
54H76	Dual J-K Master-Slave Flip-Flop	/02204	1	1	F	W
54H101	J-K Negative Edge-Triggered Flip-Flop	/02205	1	1	F	W
54H102	J-K Negative Edge-Triggered Flip-Flop	—	—	—	F	W
54H103	Dual J-K Negative Edge- Triggered Flip-Flop	/02206	1	1	F	W
54H106	Dual J-K Negative Edge- Triggered Flip-Flop	—	—	—	F	W
54H108	Dual J-K Negative Edge- Triggered Flip-Flop	—	—	—	F	—

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LOGIC—54LS SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
54LS00	Quad 2-Input NAND Gate	/30001	1	1	F	W
54LS01	Quad 2-Input NAND Gate with o/c	—	—	—	F	W
54LS02	Quad 2-Input NOR Gate	/30301	1	1	F	W
54LS03	Quad 2-Input NAND Gate with o/c	/30002	2	2	F	W
54LS04	Hex Inverter	/30003	1	1	F	W
54LS05	Hex Inverter with o/c	/30004	1	1	F	W
54LS08	Quad 2-Input AND Gate	/31004	2	2	F	W
54LS09	Quad 2-Input AND Gate with o/c	—	—	—	F	W
54LS10	Triple 3-Input NAND Gate	/30005	1	1	F	W
54LS11	Triple 3-Input NAND Gate	/31001	2	2	F	W
54LS12	Triple 3-Input NAND Gate with o/c	/30006	1	1	F	W
54LS13	Dual NAND Schmitt Trigger	/31301	2	2	F	W
54LS14	Hex Schmitt Trigger	/31302	2	2	F	W
54LS15	Triple 3-Input AND Gate with o/c	/31002	1	1	F	W
54LS20	Dual 4-Input NAND Gate	/30007	1	1	F	W
54LS21	Dual 4-Input AND Gate	/31003	1	1	F	W
54LS22	Dual 4-Input NAND Gate with o/c	/30008	1	1	F	W
54LS26	Quad 2-Input NAND Gate with o/c	/32102	2	2	F	W
54LS27	Triple 3-Input NOR Gate	/30302	2	2	F	W
54LS28	Quad 2-Input NOR Buffer	/30204	2	2	F	W
54LS30	8-Input NAND Gate	/30009	1	1	F	W
54LS32	Quad 2-Input OR Gate	/30501	2	2	F	W
54LS33	Quad 2-Input NOR Buffer with o/c	—	—	—	F	W
54LS37	Quad 2-Input NAND Buffer	/30202	1	1	F	W
54LS38	Quad 2-Input NAND Buffer with o/c	/30203	*	*	F	W
54LS40	Dual 4-Input NAND Buffer	/30201	1	1	F	W
54LS42	BCD-to-Decimal Decoder	/30703	—	—	F	W
54LS51	Dual 2-Wide 2-Input AOI Gate	/30401	1	1	F	W
54LS54	4-Wide 2-Input AOI Gate	/30402	1	1	F	W
54LS55	2-Wide 4-Input AOI Gate	—	—	—	F	W
54LS73	Dual J-K Master-Slave Flip-Flop	/30101	—	—	F	W
54LS74	Dual D-Type Edge-Triggered Flip-Flop	/30102	*	*	F	W
54LS75	Quad Bistable Latch	—	—	—	F	W
54LS76	Dual J-K Master-Slave Flip-Flop	/30110	*	*	F	W
54LS78	Quad Bistable Latch	—	—	—	F	W
54LS83A	4-Bit Binary Full Adder	/31201	*	*	F	W
54LS85	4-Bit Magnitude Comparator	/31101	2	2	F	W
54LS86	Quad 2-Input Exclusive-OR Gate	/30502	2	2	F	W
54LS90	Decade Counter	/31501	*	*	F	W
54LS92	Divide-by-Twelve Counter	/31510	*	*	F	W
54LS93	4-Bit Binary Counter	/31502	*	*	F	W
54LS95	4-Bit Left-Right Shift Register	/30603	*	*	F	W
54LS96	5-Bit Shift Register	/30604	*	*	F	W

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LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
54LS107	Dual J-K Master-Slave Flip-Flop	/30108	*	*	F	W
54LS109	Dual J-K Positive Edge- Triggered Flip-Flop	/30109	2	2	F	W
54LS112	Dual J-K Negative Edge- Triggered Flip-Flop	/30103	2	2	F	W
54LS113	Dual J-K Negative Edge- Triggered Flip-Flop	/30104	*	*	F	W
54LS114	Dual J-K Negative Edge- Triggered Flip-Flop	/30105	—	—	F	W
54LS122	Retriggerable Monostable Multivibrator	/31403	—	—	—	—
54LS125	Quad Bus Buffer Gate w/Tri-State Outputs	/32301	*	*	F	W
54LS126	Quad Bus Buffer Gate w/Tri-State Outputs	/32302	*	*	F	W
54LS132	Quad Schmitt Trigger	/31303	*	*	F	W
54LS136	Quad Exclusive-OR with o/c	—	*	*	F	W
54LS138	3-to-8 Line Decoder/Demux	/30701	*	*	F	W
54LS139	Dual 2-to-4 Line Decoder/ Demux	/30702	*	*	F	W
54LS145	BCD to Decimal Decoder/Dye	—	—	—	F	W
54LS151	8-Line to 1-Line Mux	/30901	*	*	*	*
54LS153	Dual 4-Line to 1-Line Mux	/30902	*	*	F	W
54LS154	4-Line to 16-Line Decoder/ Demux	—	—	—	I	C
54LS155	Dual 2-Line to 4-Line Decoder/Demux	—	—	—	F	W
54LS157	Quad 2-Input Data Selector (non-inv.)	/30503	*	*	F	W
54LS158	Quad 2-Input Data Selector (inv.)	/30504	*	*	F	W
54LS160	Synchronous 4-Bit Decade Counter	/31503	*	*	F	W
54LS161	Synchronous 4-Bit Binary Counter	/31504	*	*	F	W
54LS162	Synchronous 4-Bit Decade Counter	/31511	*	*	F	W
54LS163	Synchronous 4-Bit Binary Counter	/31512	*	*	F	W
54LS164	8-Bit Parallel-Out Serial Shift Register	/30605	2	2	F	W
54LS170	4X4 Register File	—	—	—	F	W
54LS173	Quad D-Type Flip-Flop (Tri-State) (8T10)	—	—	—	F	W
54LS174	Hex D-Type Flip-Flop with Clear	/30106	2	2	F	W
54LS175	Quad D-Type Edge-Triggered Flip-Flop	/30107	*	*	F	W
54LS181	4-Bit Arithmetic Logic Unit	/30901	2	—	F	W
54LS190	Synchronous Up/Down Counter (BCD)	/31513	*	*	F	W
54LS191	Synchronous Up/Down Counter (Binary)	/31509	*	*	F	W

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LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
54LS192	Synchronous Decade Up/Down Counter	/31507	*	*	F	W
54LS193	Synchronous 4-Bit Binary Up/Down Counter	/31508	*	*	F	W
54LS194	4-Bit Bidirectional Universal Shift Register	/30601	*	*	F	W
54LS195	4-Bit Parallel-Access Shift Register	/30602	*	*	F	W
54LS196	Presettable Decade Counter/Latch (8290)	/32001	*	*	F	W
54LS197	Presettable Binary Counter/Latch (8291)	/32002	*	*	F	W
54LS221	Dual Monostable Multivibrator	/31402	*	*	*	*
54LS251	Data Selector/Mux with 3-State Outputs	/30905	*	*	*	*
54LS253	Dual 4-Line to 1-Line Data Selector/Mux	/30906	*	*	F	W
54LS257	Quad 2-Line to 1-Line Data Selector/Mux	/30906	*	*	*	*
54LS258	Quad 2-Line to 1-Line Data Selector/Mux	/30907	*	*	*	*
54LS260	Dual 5-Input NOR Gate	—	—	—	F	W
54LS261	2X4 Parallel Binary Multiplier	—	—	—	F	W
54LS266	Quad Exclusive-NOR Gate	/30303	2	2	F	W
54LS279	Quad S-R Latch	—	—	—	F	W
54LS280	9-Bit Odd/Even Parity Generator/Checker	—	—	—	*	*
54LS283	4-Bit Adder	/31202	*	*	F	W
54LS290	Decade Counter	/32003	*	*	F	W
54LS293	4-Bit Binary Counter	/32004	*	*	F	W
54LS295A	4-Bit Right-Shift Left-Shift Register	/30606	*	*	F	W
54LS298	Quad 2-Input Mux with Storage	—	—	—	F	W
54LS365	Hex Buffer w/Common Enable (3-State)	/32201	*	*	F	W
54LS366	Hex Buffer w/Common Enable (3-State)	/32202	*	*	F	W
54LS367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32203	*	*	F	W
54LS368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32204	*	*	F	W
54LS375	Quad Latch	—	—	—	F	W
54LS388	Exclusive-OR Gate	—	—	—	F	W
54LS395	4-Bit Cascadeable Shift Register (3-State)	/30607	*	*	F	W
54LS445	BCD to Decimal Decoder/Dye	—	—	—	F	W
54LS670	4X4 Register File (Tri-State)	—	—	—	F	W

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LOGIC—54S SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
54S00	Quad 2-Input NAND Gate	/07001	1	1	F	W
54S02	Quad 2-Input NOR Gate	/07301	2	2	F	W
54S03	Quad 2-Input NAND Gate with o/c	/07002	1	1	F	W
54S04	Hex Inverter	/07003	1	1	F	W
54S05	Hex Inverter with o/c	/07004	1	1	F	W
54S06	Quad 2-Input AND Gate	/07005	—	—	—	—
54S07	Quad 2-Input AND Gate with o/c	/07006	—	—	—	—
54S10	Triple 3-Input NAND Gate	/07008	1	1	F	W
54S11	Triple 3-Input NAND Gate	/07009	1	1	F	W
54S15	Triple 3-Input AND Gate with o/c	/07002	2	2	F	W
54S20	Dual 4-Input NAND Gate	/07006	1	1	F	W
54S22	Dual 4-Input NAND Gate with o/c	/07007	1	1	F	W
54S30	8-Input NAND Gate	/07008	—	—	—	—
54S32	Quad 2-Input OR Gate	—	—	—	F	W
54S40	Dual 4-Input NAND Buffer	/07201	2	2	F	W
54S51	Dual 2-Input 2-Input A01 Gate	/07401	1	1	F	W
54S54	4-2-3-2 Input A01 Gate	/07402	2	2	F	W
54S55	4-2-4-2 Input A01 Gate	/07403	2	2	F	W
54S74	Dual D-Type Edge-Triggered Flip-Flop	/07101	2	2	F	W
54S85	4-Bit Magnitude Comparator	/07301	2	—	F	—
54S86	Quad 2-Input Exclusive-OR Gate	/07501	2	2	F	W
54S112	Dual J-K Negative Edge- Triggered Flip-Flop	/07102	*	*	F	W
54S113	Dual J-K Negative Edge- Triggered Flip-Flop	/07103	*	*	F	W
54S114	Dual J-K Negative Edge- Triggered Flip-Flop	/07104	—	—	F	W
54S133	13-Input NAND Gate	/07009	1	1	F	W
54S134	13-Input NAND Gate w/Tri- State Outputs	/07010	2	2	F	W
54S135	Quad Exclusive-OR/NOR Gate	/07502	—	—	—	—
54S136	3-to-8 Line Decoder/Demux	/07701	—	—	—	—
54S139	Dual 2-to-4 Line Decoder/ Demux	/07702	—	—	F	W
54S140	Dual 4-Input NAND Line Driver	/08101	2	2	F	W
54S151	8-Line to 1-Line Mux	/07901	2	2	F	W
54S153	Dual 4-Line to 1-Line Mux	/07902	2	2	F	W
54S157	Quad 2-Input Data Selector (non.inv.)	/07903	2	2	F	W
54S158	Quad 2-Input Data Selector (inv.)	/07904	2	2	F	W
54S174	Hex D-Type Flip-Flop with Clear	/07105	—	—	F	W
54S175	Quad D-Type Edge-Triggered Flip-Flop	/07106	—	—	*	*
54S181	4-Bit Arithmetic Logic Unit	/07801	2	—	F	*
54S182	Look-Ahead Carry Generator	/07802	—	—	*	*
54S184	4-Bit Bidirectional Universal Shift Register	/07601	—	—	—	—
54S185	4-Bit Parallel-Access Shift Register	/07602	—	—	—	—

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LOGIC—54S SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK
54S251	Data Selector/Mux with 3-State Outputs	/07905	—	—	—	—
54S253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	F	W
54S257	Quad 2-Line to 1-Line Data Selector/Mux	/07906	—	—	—	—
54S258	Quad 2-Line to 1-Line Data Selector/Mux	/07907	—	—	—	—
54S260	Dual 5-Input NOR Gate	—	—	—	F	W
54S280	9-Bit Odd/Even Parity Generator/Checker	/07703	—	—	—	—
54S350	4/6 Bit Shifter-Tri-State	—	—	—	F	—

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LOGIC—8200/9300/9600 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED*		MIL REL/883 MIL TEMP	
			Dip	Flat Pack	Dip	Flat Pack
8200	Dual 5-Bit Buffer Register	—	—	—	I	Q
8201	Dual 5-Bit Buffer Register with D Inputs	—	—	—	I	Q
8202	10-Bit Buffer Register	—	—	—	I	Q
8203	10-Bit Buffer Register with D Inputs	—	—	—	I	Q
8230	8-Input Digital Multiplexer	/01402	*	*	F	W
8231	8-Input Digital Multiplexer	—	—	—	F	W
8232	8-Input Digital Multiplexer	—	—	—	F	W
8233	2-Input 4-Bit Digital Multiplexer	—	—	—	F	W
8234	2-Input 4-Bit Digital Multiplexer	—	—	—	F	W
8235	2-Input 4-Bit Digital Multiplexer	—	—	—	F	W
8241	Quad Exclusive-OR Gate	—	—	—	F	W
8242	Quad Exclusive-NOR Gate	—	—	—	F	W
8243	8-Bit Position Scaler	—	—	—	I	Q
8250	Binary-to-Octal Decoder	/15204	2	2	F	W
8251	BCD-to-Decimal Decoder	/15205	2	2	F	W
8252	BCD-to-Decimal Decoder	/15206	—	—	F	W
8260	Arithmetic Logic Unit	—	—	—	I	Q
8261	Fast Carry Extender	—	—	—	F	W
8262	4-Bit Parity Generator and Checker	—	—	—	F	W
8263	3-Input 4-Bit Digital Multiplexer	—	—	—	I	Q
8264	3-Input 4-Bit Digital Multiplexer	—	—	—	I	Q
8266	2-Input 4-Bit Digital Multiplexer	—	—	—	F	W
8267	2-Input 4-Bit Digital Multiplexer	—	—	—	F	W
8268	Gated Full Adder	—	—	—	F	Q
8269	4-Bit Comparator	—	—	—	F	W
8270	4-Bit Shift Register	—	—	—	F	W
8271	4-Bit Shift Register	—	—	—	F	W
8273	10-Bit Serial-In, Parallel-Out Shift Register	—	—	—	F	W
8274	10-Bit Parallel-In, Serial-Out Shift Register	—	—	—	F	W
8275	Quad Bistable Latch	—	—	—	F	W
8276	8-Bit Serial Shift Register	—	—	—	F	—
8277	Dual 8-Bit Shift Register	—	—	—	F	—
8280	Presetable Decade Counter	—	—	—	F	W
8281	Presetable Binary Counter	—	—	—	F	W
8284	Binary Up/Down Counter	—	—	—	F	W
8285	Decade Up/Down Counter	—	—	—	F	W
8288	Divide-by-Twelve Counter	—	—	—	F	W
8290	Presetable High Speed Decade Counter	—	—	—	F	W
8291	Presetable High Speed Binary Counter	—	—	—	F	W
8292	Presetable Low Power Decade Counter	—	—	—	F	W
8293	Presetable Low Power Binary Counter	—	—	—	F	W
9300	4-Bit Shift Register	/15901	—	—	F	W
9301	BCD to Decimal Decoder	/15206	2	2	F	W
9308	Dual 4-Bit Latch w/Clear	—	—	—	I	Q
9309	Dual 4-Input Multiplexer	/01404	I	I	F	W
9310	4-Bit Decade Counter	—	—	—	F	W
9312	8-Input Digital Multiplexer	/01402	*	*	F	W
9316	4-Bit Binary Counter	—	—	—	F	W
9322	Data Selector Multiplexer	—	—	—	F	W
9324	5-Bit Comparator	/15002	*	*	W	—
9334	8-Bit Addressable Latch	/16001	—	—	F	W
9602	Dual Monostable Multivibrator	/01205	*	*	F	W

NOTE

Per QPL 38510-30 dated
1 September 1977
1 = Level 1 Qualification
2 = Level 2 Qualification
* = In Process

LOGIC—8T INTERFACE SERIES

DEVICE	DESCRIPTION	JAN M38510 SHEET	MIL REL/883 MIL TEMP	
			Dip	Flat Pack
8T04	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	—	F	W
8T06	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T09	Quad Bus Driver with Tri-State Outputs	—	F	W
8T10	Quad D-Type Bus Latch (Tri-State)	—	F	W
8T26A	Quad Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T28	Quad Non-Inverting Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T31	8-Bit Bidirectional I/O Port	—	*	*
8T32	Programmable 8-Bit, I/O Port (3-State)	—	I	*
8T33	Programmable 8-Bit, I/O Port (Open Collector)	—	I	*
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	—	F	W
8T96	High Speed Hex Buffers/Inverters (74366/DM8096)	—	F	W
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)	—	F	W
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)	—	F	W

* = Qualification planned

LINEAR PRODUCTS

DEVICE	DESCRIPTION	PACKAGE*
COMPARATORS		
SE521	Dual Comparator	F
SE526	Analog Voltage Comparator	F K
SE527	Analog Voltage Comparator	F K
SE529	Analog Voltage Comparator	F K
LH2111	Dual Comparator	F
LM111	Comparator	F T
LM119	Dual Comparator	F K
LM139	Quad Comparator	F
LM193/193A	Dual Comparator	F T
μA710	Differential Voltage Comparator	F T
μA711	Comparator	F K
DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F
SE511	Dual Differential Amplifier	F
SE515	Differential Amplifier	F K
μA733	Video Amplifier	F K
OPERATIONAL AMPLIFIERS		
LF155/156/157	FET Op Amp	T
LH2101A	Dual Op Amp	F
LH2108A	Dual Op Amp	F
LM101	High Perf. Op Amp	F T
LM101A	High Perf. Op Amp	F T
LM107	General Purpose Op Amp	F F
LM108	Precision Op Amp	F T
LM108A	Precision Op Amp	F T
LM124	Quad Op Amp	F
LM158	Dual Op Amp	F T
MC1556	Op Amp	F T
MC1558	Dual Op Amp	F T
SE530	Hi Slew Op Amp	F T
SE532	Dual Op Amp	— T
SE535	Hi Slew Rate Op Amp	T
SE538	Hi Slew Rate Op Amp	T
SE5530	Dual Hi Slew Op Amp	F K
SE5534	Dual Hi Slew Op Amp	F K
SE5535	Dual Hi Slew Op Amp	F K
SE5538	Lo Noise Op Amp	T
μA709	Op Amp	F T
μA709A	Op Amp	F T
μA741	General Purpose Op Amp	F T
μA747	Dual Op Amp	F K
μA748	General Purpose Op Amp	F T

***NOTE**

F = Cerdip
 K/T/L = Metal can
 DA/DB = TO-3 can
 Flat pack available—special request

†JAN per QPL M38510-30 date 1 September 1977

DEVICE	DESCRIPTION	PACKAGE
PHASE LOCKED LOOPS		
SE567	Tone Decoder P11	F T
SE564	Phase Locked Loop	F T
LINE RECEIVERS		
DM7820	Dual Differential Line Receiver	F
DM7830	Dual Differential Line Receiver	F
TIMERS		
SE555	Timer	F T
SE556	Dual Timer	F
SE558/9	Quad Timer	F
VOLTAGE REGULATORS		
LM109	5 Volt Regulator	DA
SE5551	Dual Track Reg	F
SE5552	Dual Track Reg	F
SE5553	Dual Track Reg	F
SE5554	Dual Track Reg	F
78XX (7)	Positive Reg	DA
79XX (7)	Negative Reg	DA
79MXX (7)	Med Power Reg	DB
μA723	Precision Voltage Regulator	F L
†78HV00 (7)	Hi Voltage Regulator	DA
DRIVERS		
DS1611-1614	Peripheral Drivers	T
D/A		
MC1508-8	8-Bit D/A	F
SE5008	8-Bit D/A	F
SE5009	8-Bit D/A	F
SE5018	8-Bit D/A- μP Compatible	F
INTERFACE		
†55325	Memory Driver	F

JAN-M-38510					
DEVICE	SLASH SHEET	PACKAGE		QUAL. STATUS	
†JB555	10901	F	T	July	1977-Part II
JB556	10902	F		Nov.	1977-Part II
JB101	10103	F	T	Jan.	1978-Part I
JB741	10101	F	T	Dec.	1977-Part I
JB747	10102	F	K	Jan.	1978-Part I

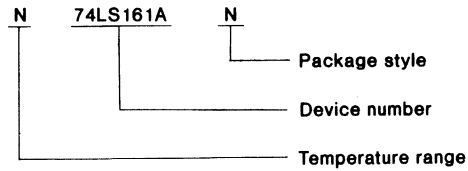
SECTION 9

Packages and Ordering Information

PACKAGES AND ORDERING INFORMATION

The Signetics TTL logic products are available in a variety of packages and two temperature ranges. The correct ordering code or part number for the devices is an alpha-numeric sequence as explained below. The commercial range (7400, N8200, N8T, etc.) devices are available in plastic and ceramic dual-in-line (DIP) packages, and the military range (5400, S8200, S8T, etc.) devices are available in ceramic DIP and ceramic flat packs. All devices are not available in both temperature ranges or all packages. The ordering codes on the individual data sheets indicate the normal or planned availability of the product. However, the availability of specific part numbers can be obtained from your local Signetics sales office or franchised distributor.

Ordering Code



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
N = Commercial range 0°C to 70°C (0°C to 75°C for 8200 and 9300)	74LS161A	F = Ceramic DIP N = Plastic DIP
S = Military range -55°C to 125°C	54LS161A	F = Ceramic DIP I = Ceramic DIP Q = Ceramic flatpack W = Ceramic Flatpack

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
 - a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 or equivalent, solder dipped.
6. Body material: Plastic
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

9. Lead material
 - a. Alloy 52—gold plated, or solder dipped.
 - b. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
 - c. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated.
 - d. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
 - e. ASTM alloy F-15 (KOVAR) or equivalent—tin plated.
10. Body Material
 - a. 1010 Steel—nickel plated or tin plate over nickel.
 - b. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated.
 - c. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
 - d. Ceramic with glass seal at leads.

- e. BeO ceramic with glass seal at leads.
- f. Ceramic with ASTM alloy F-15 or equivalent.

11. Lid Material

- a. 1010 steel, nickel plated, or tin-plate over nickel, weld seal.
 - b. Nickel or tin plated nickel, weld seal.
 - c. Ceramic, glass seal.
 - d. ASTM alloy F-15 or equivalent, gold plated.
 - e. BeO Ceramic with glass seal.
 - f. Translucent $A12O3$, glass seal.
12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
 13. Recommended minimum offset before lead bend.
 14. Maximum glass climb .010 inches.
 15. Maximum glass climb or lid skew is .010 inches.
 16. Typical four places.
 17. Dimension also applies to seating plane.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W)	DESCRIPTION ¹
Standard Dual-in-Line			
8	NE	162/65	
14	NH	150/65	TO-116/MO-001
16	NJ	137/53	MO-001
18	NK	135/53	
20	NL	135/53	
22	NM	120/53	
24	NN	116/53	MO-015
24	NND ³	TBD	
28	NQ	116/53	MO-015
40	NW ³	110/50	MO-015
Power Dual-in-Line			
8	NEA ^{2,3}	TBD	Heatsink
14	NHA ²	95/33	Heatsink
16	NJA ²	95/33	Heatsink
18	NKA ²	90/26	Heatsink
20	NLA ²	90/26	Heatsink
22	NMA ^{2,3}	TBD	Heatsink
24	NNA ²	60/23	Heatsink
28	NQA ²	56/21	Heatsink
40	NWA ^{2,3}	TBD	Heatsink
Power			
3	S	200/70	TO-92
3	UCA	75/3	TO-220
3 + GND	UC	95/15	Single-in-Line (SIL)
4 + GND	UD	95/15	Single-in-Line (SIL)
5 + GND	UEA	TBD	TO-220
7 + GND	UGA ³	TBD	TO-220
12 + GND	PH/PHA	95/15	Batwing

PACKAGES

HERMETIC PACKAGES

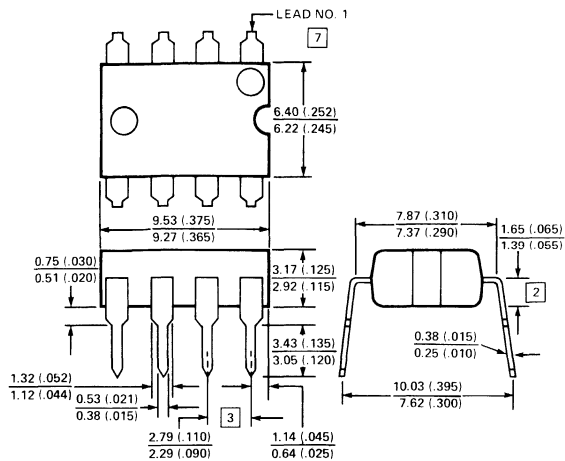
NO. OF LEADS	PACKAGE CODE	$\theta_{ja}/\theta_{jc} (^{\circ}\text{C}/\text{W})$	DESCRIPTION ¹
Metal Headers			
2	DA	TBD	TO-3 Solid Header
3	DB	TBD	TO-39 Solid Header, Short Can
4	DC	TBD	TO-72 Solid Header
4	DE	TBD	TO-72 Glass Filled Header
8	T	150/45	TO-99 Header (.200 Dia.)
10	K	150/45	TO-100 Header, Short Can
10	L	150/45	TO-100 Header, Tall Can
Flat Packs			
10	WF	240/50	Flat Ceramic
14	WH	205/50	Flat Ceramic
16	WJ	200/50	Flat Ceramic
24	WN	155/40	Flat Ceramic
16	RJA	145/26	Flat Ceramic, BeO
18	RKA	107/22	Flat Ceramic, BeO
24	RNA	107/22	Flat Ceramic, BeO
28	RQA	107/22	Flat Ceramic, BeO
40	RWA	TBD	Flat Ceramic, BeO
10	QFA	230/55	Flat Ceramic Laminate
14	QHA	185/45	Flat Ceramic Laminate
16	QJA	170/45	Flat Ceramic Laminate
24	QNA	155/44	Flat Ceramic Laminate
68	GBA ³	TBD	Flat Ceramic Laminate, Leadless
Cerdip Family			
8	FE	TBD	Dual-in-Line Ceramic
14	FH	110/30	Dual-in-Line Ceramic
16	FJ	100/30	Dual-in-Line Ceramic
18	FK	93/27	Dual-in-Line Ceramic
20	FL	TBD	Dual-in-Line Ceramic
22	FM	75/27	Dual-in-Line Ceramic
24	FN	60/26	Dual-in-Line Ceramic
28	FQ ³	TBD	Dual-in-Line Ceramic
40	FW ³	TBD	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
8	IEA	100/30	Dip Laminate
14	IHA	95/25	Dip Laminate
16	IJA	90/25	Dip Laminate
18	IKA	88/25	Dip Laminate
22	IMA	80/25	Dip Laminate
24	INC	65/25	Dip Laminate
28	IQA	60/25	Dip Laminate
40	IWA	55/25	Dip Laminate
50	IZA	42/20	Dip Laminate

NOTES

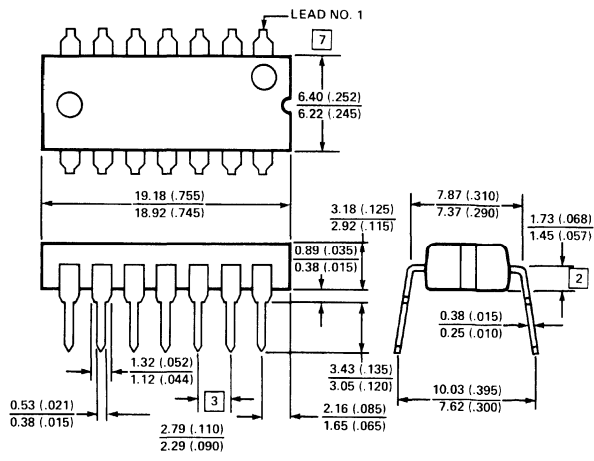
1. Dual-in-Line packages unless otherwise described.
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads
3. Package not yet available, scheduled for 1978 release

PLASTIC: Standard and Power Dual-In-Line

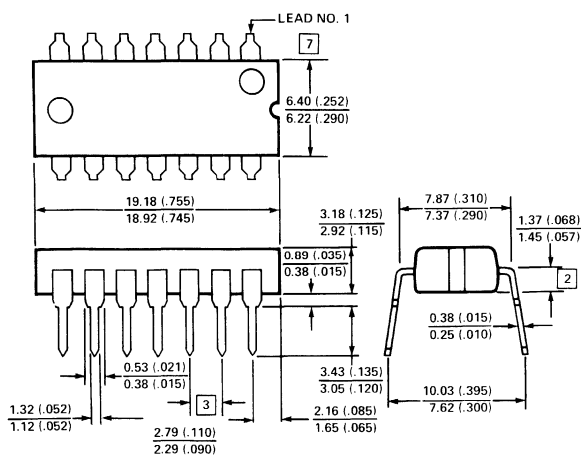
NE Package and NEA Package



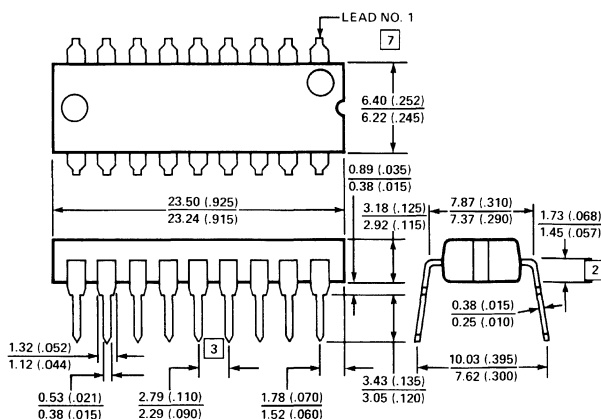
NH Package and NHA Package



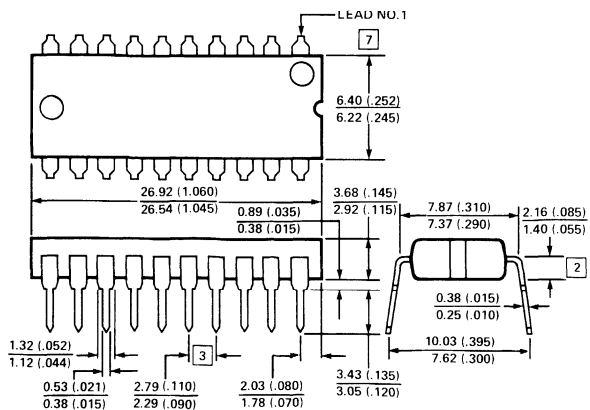
NJ Package and NJA Package



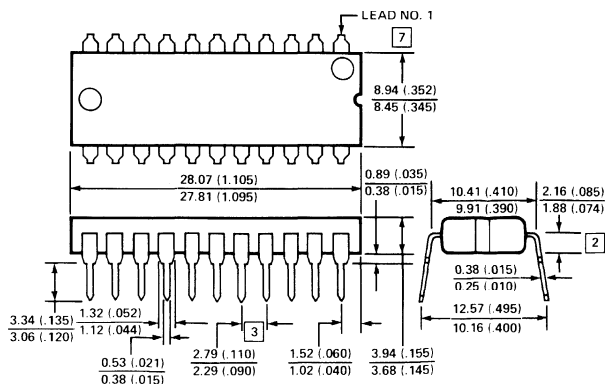
NK Package and NKA Package



NL Package and NLA Package



NM Package and NMA Package



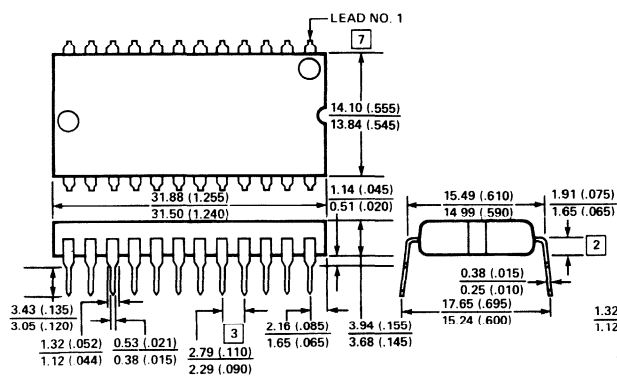
PACKAGES

PLASTIC: Standard and Power Dual-In-Line (cont't.)

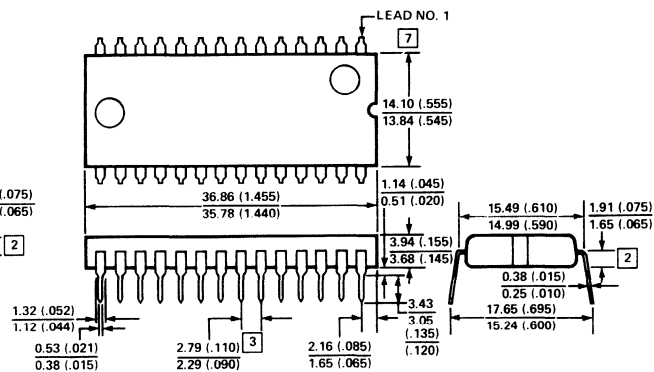
NND Package

Package not yet available.
Scheduled for 1978 release.

NN Package and NNA Package



NQ Package and NQA Package



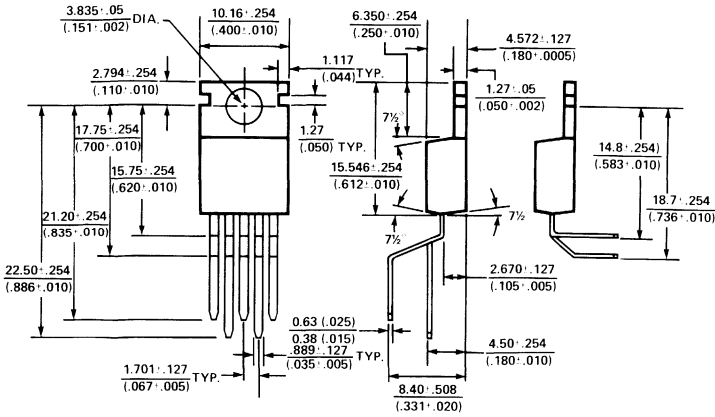
NW Package and NWA Package

Package not yet available.
Scheduled for 1978 release.

PLASTIC: Power (Not Dual-In-Line) (cont'd.)

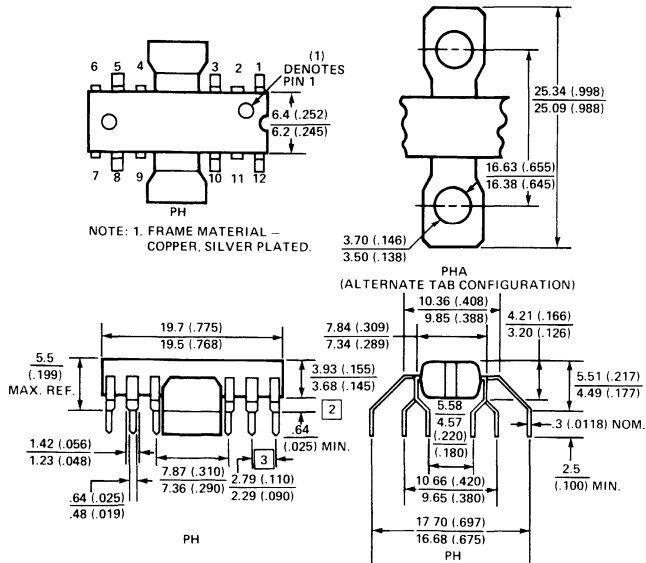
UEA Package

UGA Package



Package not yet available.
Scheduled for 1978 release.

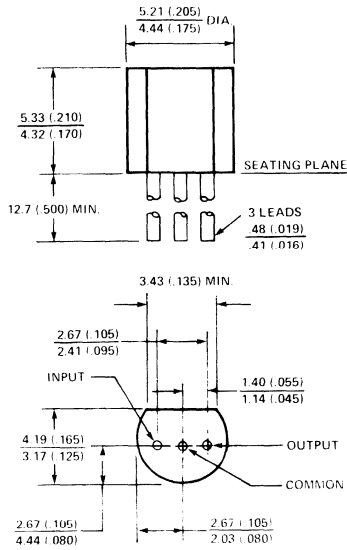
PH/PHA Package



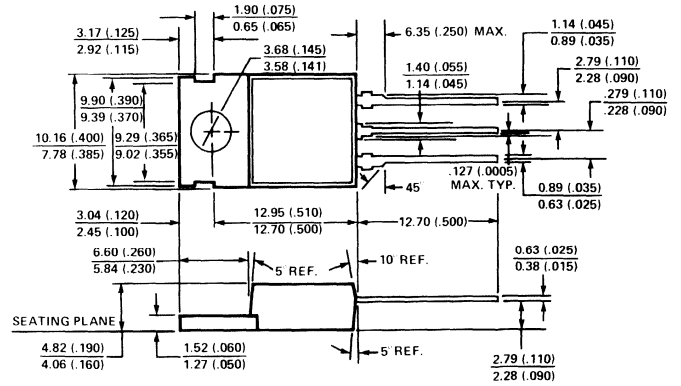
PACKAGES

PLASTIC: Power (Not Dual-In-Line)

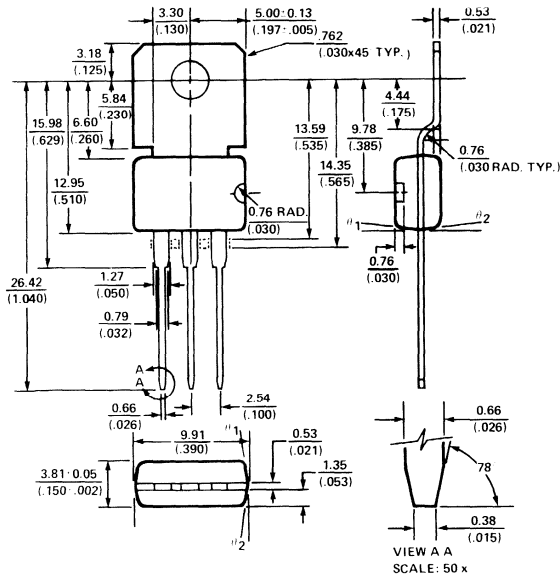
S Package



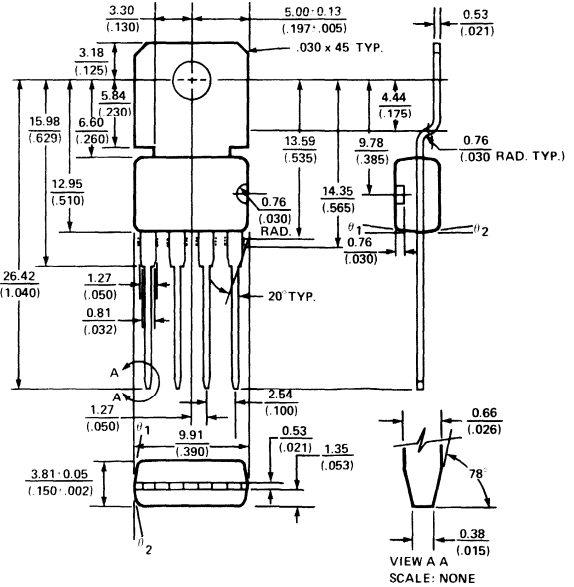
UCA Package



UC Package



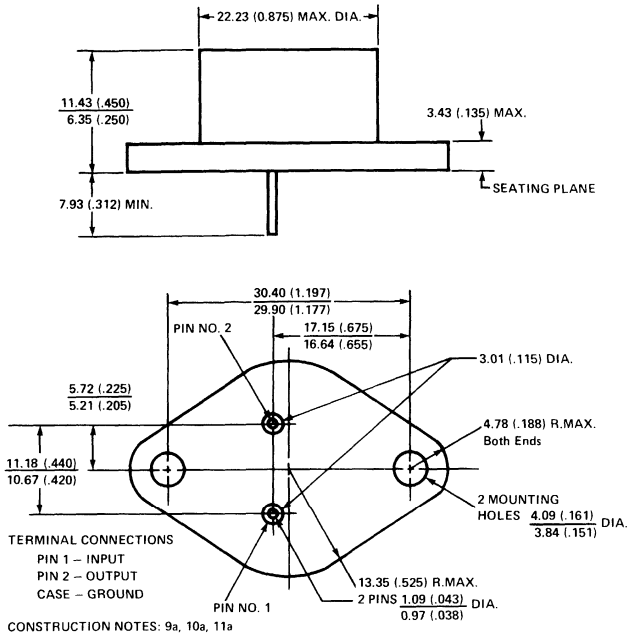
UD Package



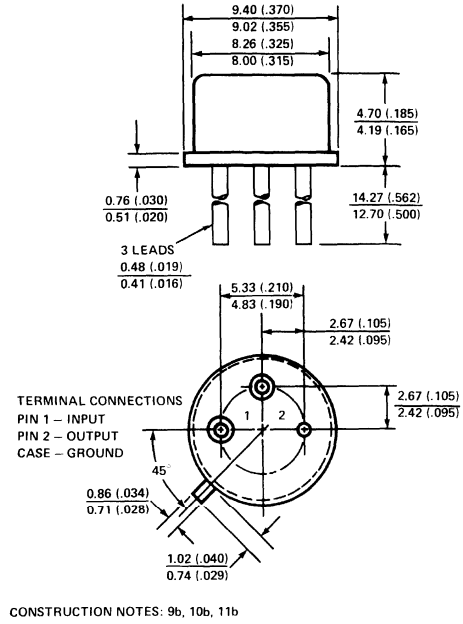
PACKAGES

HERMETIC: Metal Headers

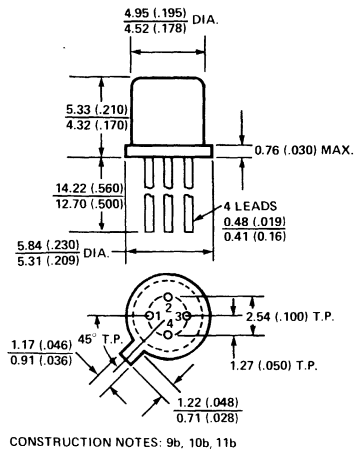
DA Package



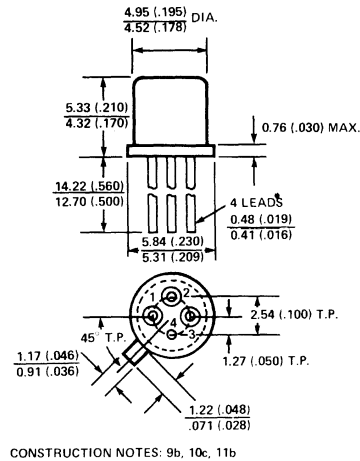
DB Package



DC Package



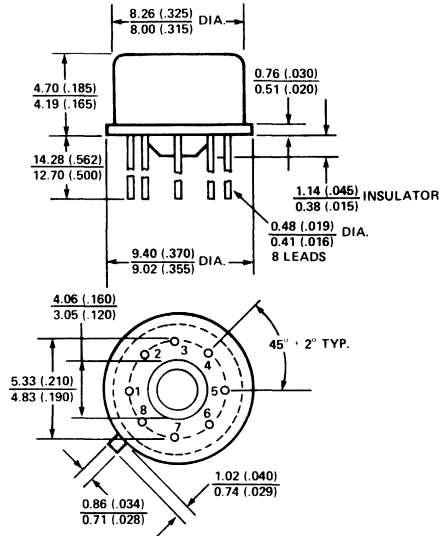
DE Package



PACKAGES

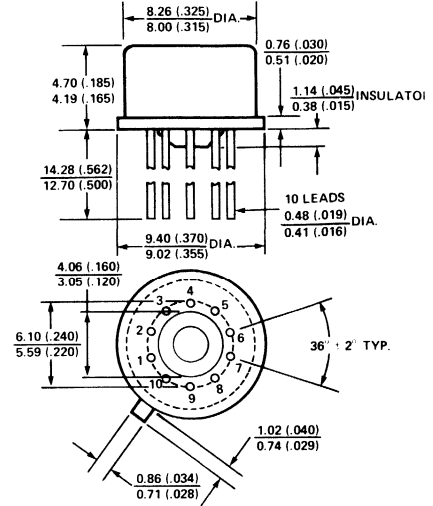
HERMETIC: Metal Headers (cont'd.)

T Package



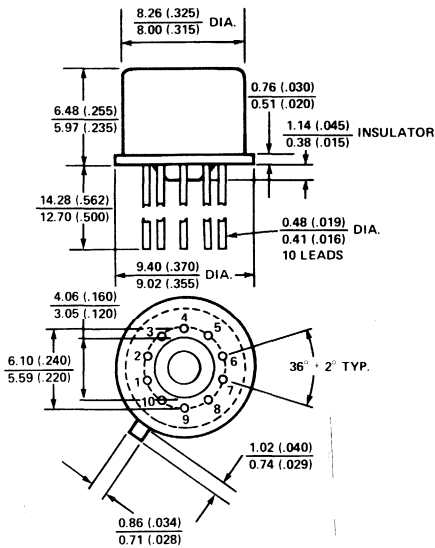
CONSTRUCTION NOTES: 9b, 10c, 11b

K Package



CONSTRUCTION NOTES: 9b, 10c, 11b

L Package

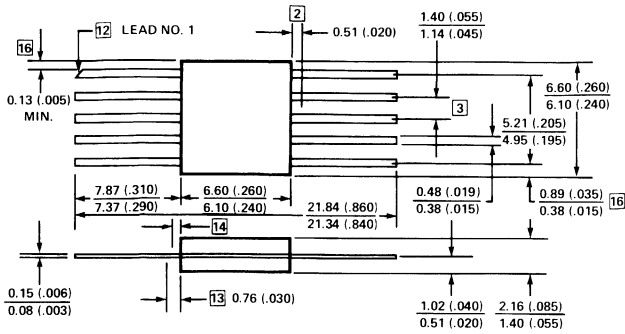


CONSTRUCTION NOTES: 9b, 10c, 11b

PACKAGES

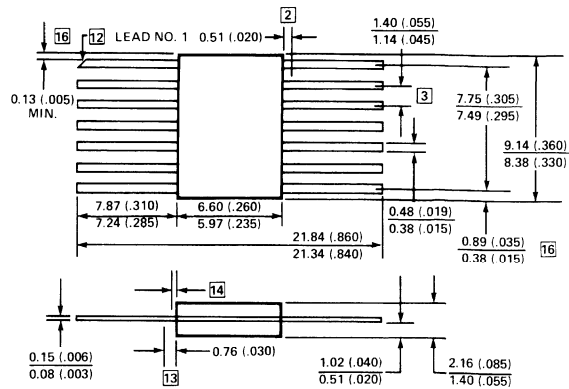
HERMETIC: Flat Packs

WF Package



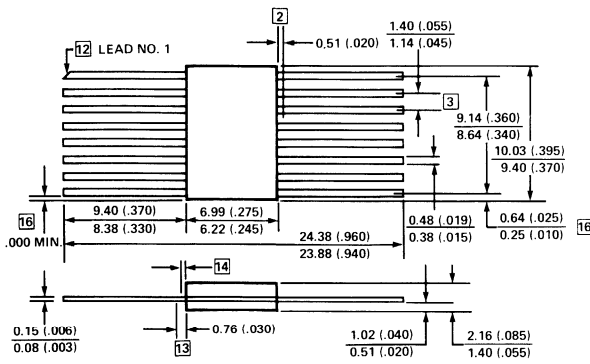
CONSTRUCTION NOTES: 9c, 10d, 11c

WH Package



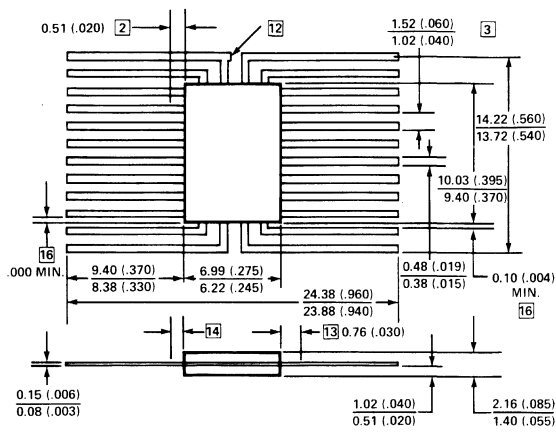
CONSTRUCTION NOTES: 9c, 10d, 11c

WJ Package



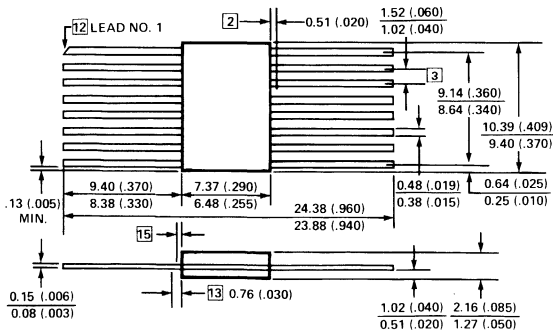
CONSTRUCTION NOTES: 9c, 10d, 11c

WN Package



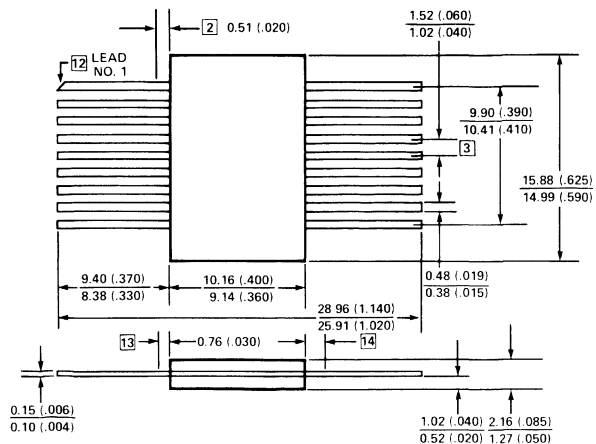
CONSTRUCTION NOTES: 9c, 10d, 11c

RJA Package



RJA CONSTRUCTION NOTES: 9c, 10e, 11e

RKA Package

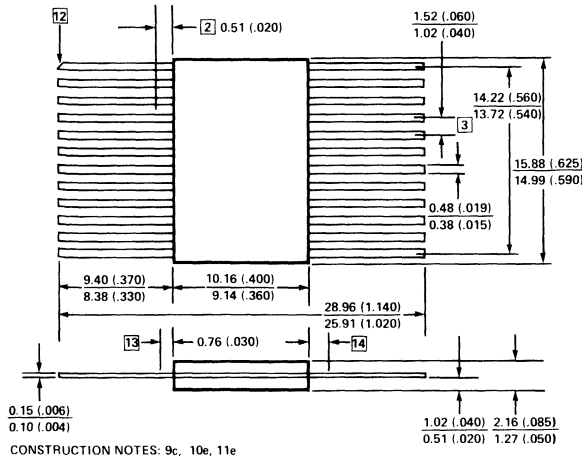


CONSTRUCTION NOTES: 9c, 10e, 11e

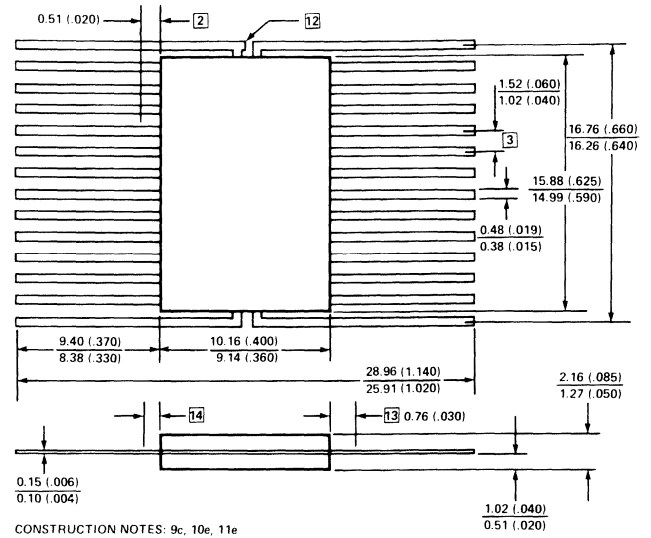
PACKAGES

HERMETIC: Flat Packs (cont'd.)

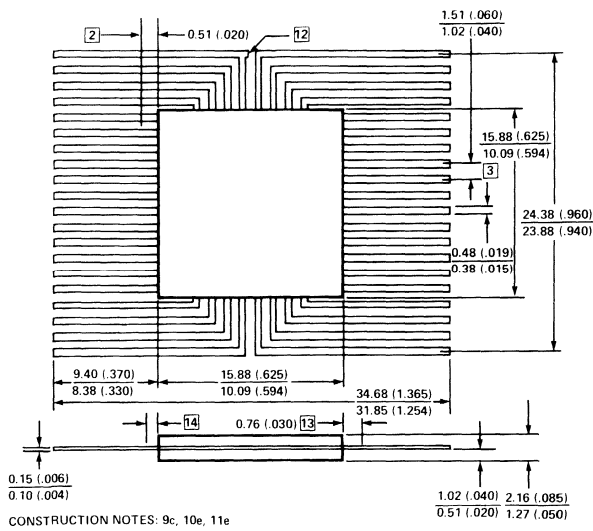
RNA Package



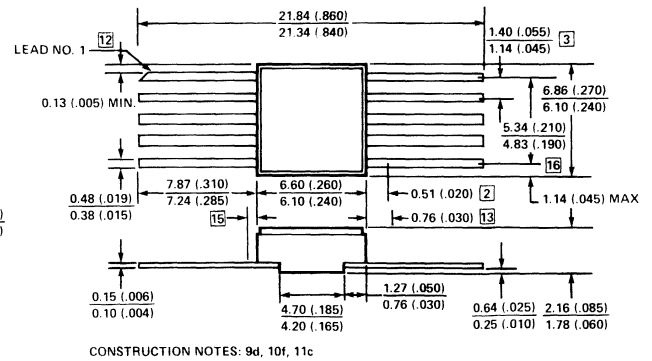
ROA Package



RWA Package

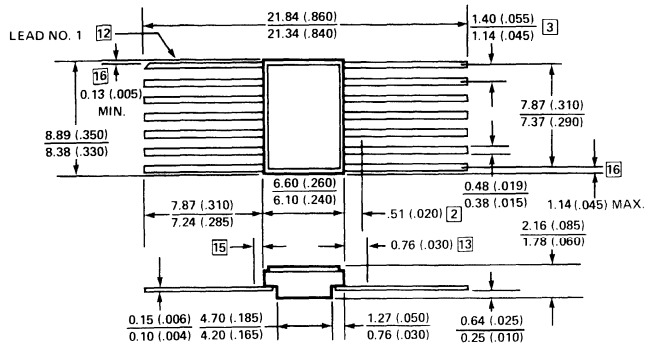


QFA Package



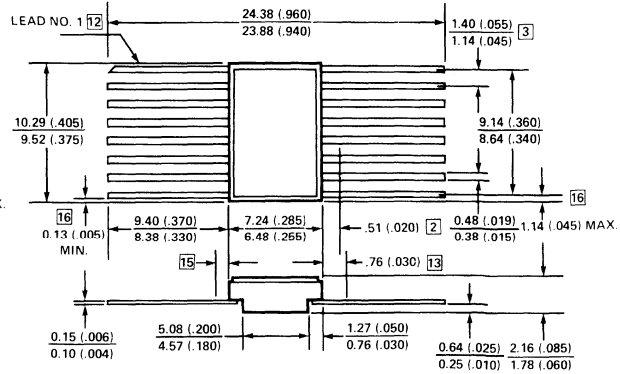
HERMETIC: Flat Packs (cont'd.)

QHA Package



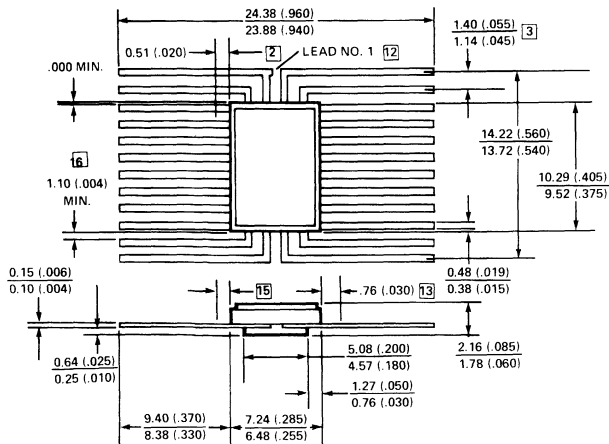
CONSTRUCTION NOTES: 9d, 10f, 11c

QJA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

QNA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

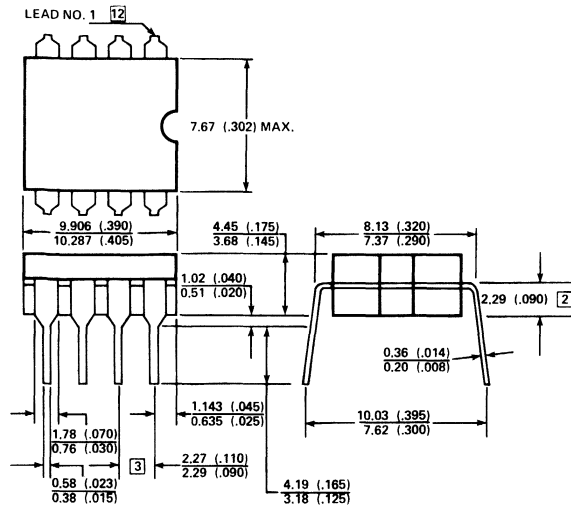
GBA Package

Package not yet available.
Scheduled for 1978 release.

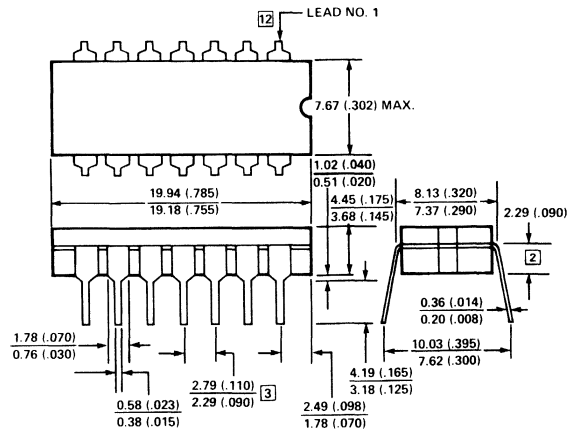
PACKAGES

HERMETIC: Cerdip

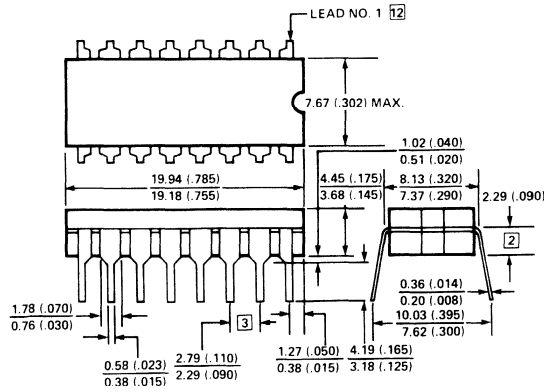
FE Package



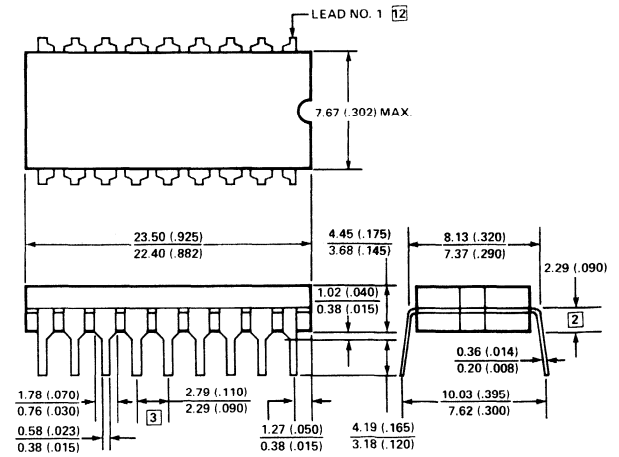
FH Package



FJ Package

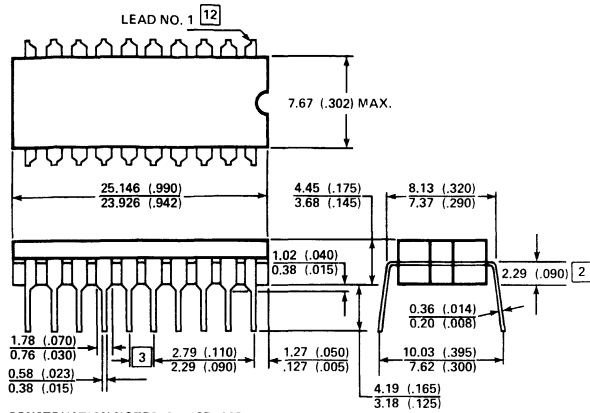


FK Package



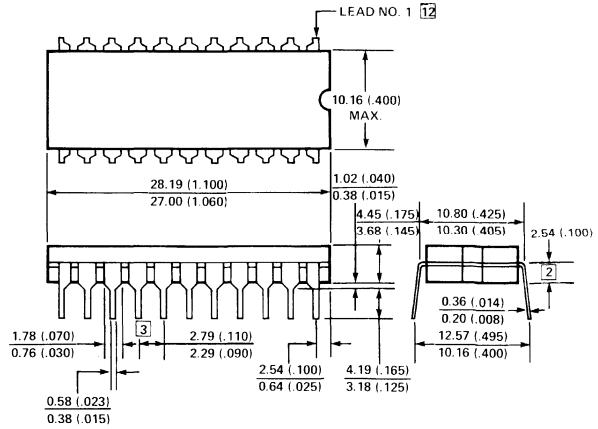
HERMETIC: Cerdip (cont'd.)

FL Package



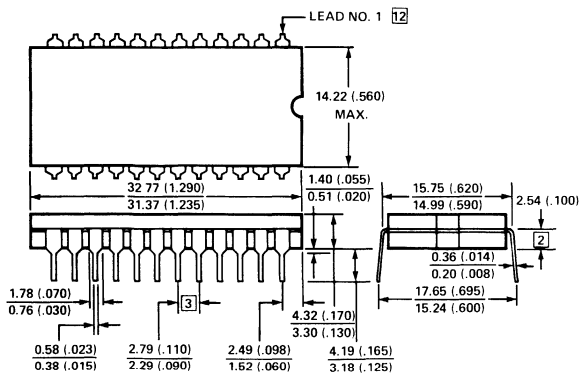
CONSTRUCTION NOTES: 9c, 10d, 11c

FM Package



CONSTRUCTION NOTES: 9c, 10d, 11c

FN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

FQ Package

Package not yet available.
Scheduled for 1978 release.

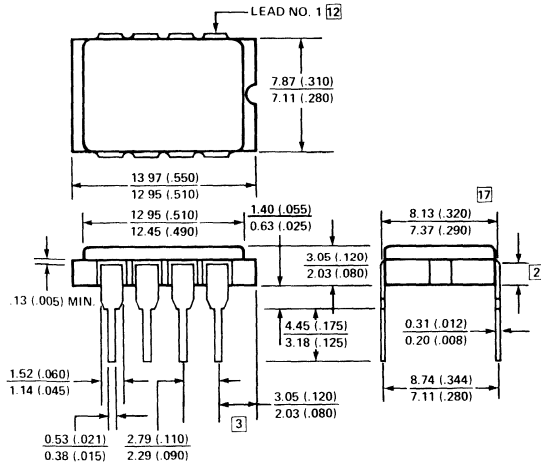
FW Package

Package not yet available.
Scheduled for 1978 release.

PACKAGES

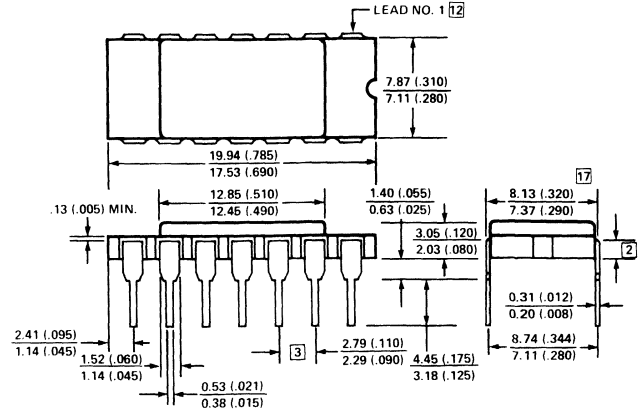
HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package



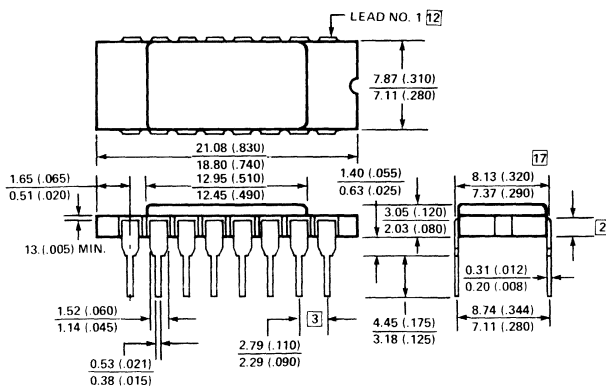
CONSTRUCTION NOTES: 9e, 10f, 11c

IHA Package



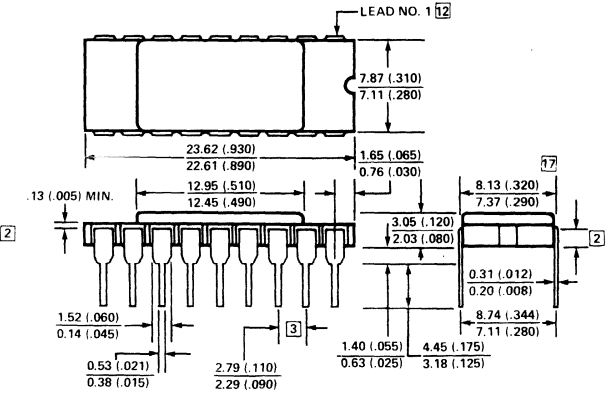
CONSTRUCTION NOTES: 9e, 10f, 11c

IJA Package



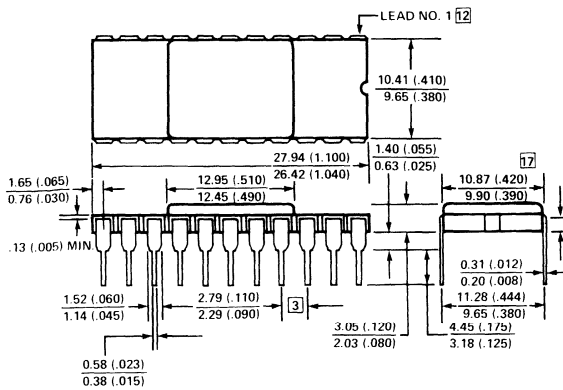
CONSTRUCTION NOTES: 9e, 10d, 11c

IKA Package



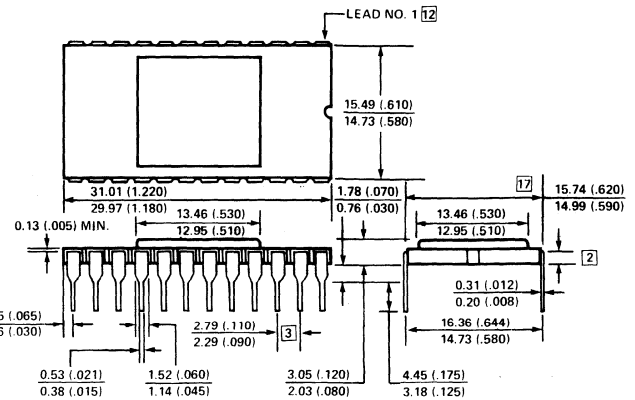
CONSTRUCTION NOTES: 9e, 10f, 11c

IMA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

INC Package

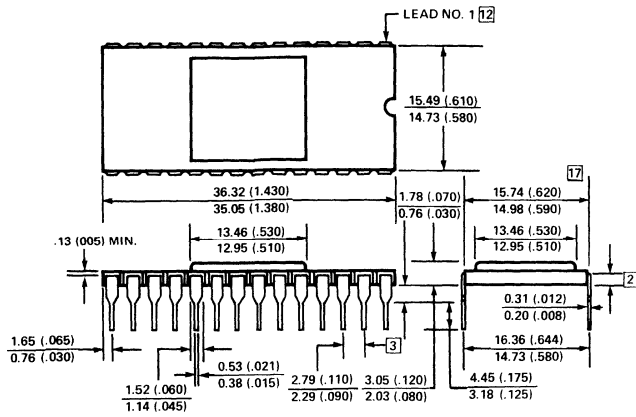


CONSTRUCTION NOTES: 9e, 10f, 11f (IND)

PACKAGES

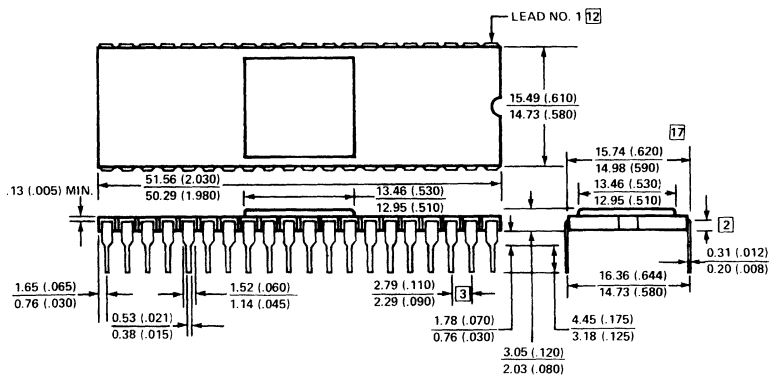
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package



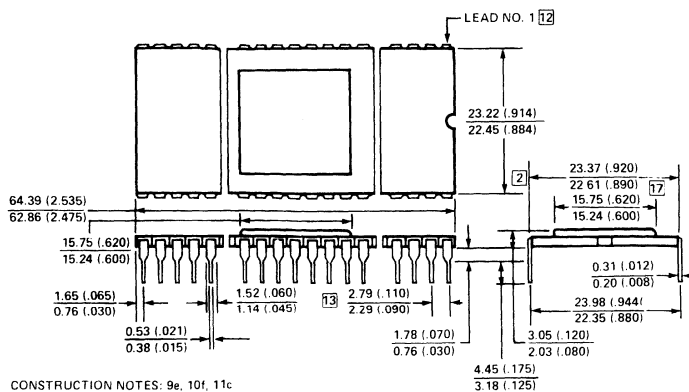
CONSTRUCTION NOTES: 9e, 10f, 11c

IWA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

IZA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

STANDARD (54/74) TTL FAMILY DC CHARACTERISTICS

DC CHARACTERISTICS OVER OPERATING TEMPERATURES (Unless otherwise specified on Data Sheet)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		Min	Typ ¹	Max		
V _{IH}	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL}	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V _{CD}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -12mA		-0.8	-1.5	V
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 16mA			0.4	V
V _{OH}	Output HIGH voltage	V _{CC} = Min, I _{OH} = -800μA	2.4	3.5		V
I _{OH}	Output HIGH current (open collector)	V _{CC} = Min, V _{OUT} = 5.5V			250	μA
I _{OZH}	Output "off" current HIGH (3-state)	V _{CC} = Max, V _{OUT} = 2.4V, V _{OE} = 2.0V			40	μA
I _{OZL}	Output "off" current LOW (3-state)	V _{CC} = Max, V _{OUT} = 0.5V, V _{OE} = 2.0V			-40	μA
I _{IH}	Input HIGH current ²	V _{CC} = Max, V _{IN} = 2.4V			40	μA
I _I	Input HIGH current at max input voltage	V _{CC} = Max, V _{IN} = 5.5V			1.0	mA
I _{IL}	Input LOW current ²	V _{CC} = Max, V _{IN} = 0.4V			-1.6	mA
I _{OS}	Output short circuit current	V _{CC} = Max, V _{OUT} = OV	Mil	-20	-55	mA
			Com	-18	-55	mA

HIGH SPEED (54H/74H) TTL FAMILY DC CHARACTERISTICS

DC CHARACTERISTICS OVER OPERATING TEMPERATURES (Unless otherwise specified on Data Sheet)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		Min	Typ ¹	Max		
V _{IH}	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL}	Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V _{CD}	Input clamp diode voltage	V _{CC} = Min, I _{IN} = -8mA		-0.8	-1.5	V
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 20mA			0.4	V
V _{OH}	Output HIGH voltage	V _{CC} = Min, I _{OH} = -500μA	2.4	3.5		V
I _{OH}	Output HIGH current (open collector)	V _{CC} = Min, V _{OUT} = 5.5V			250	μA
I _{OZH}	Output "off" current HIGH (3-state)	V _{CC} = Max, V _{OUT} = 2.4V, V _{OE} = 2.0V			50	μA
I _{OZL}	Output "off" current LOW (3-state)	V _{CC} = Max, V _{OUT} = 0.5V, V _{OE} = 2.0V			-50	μA
I _{IH}	Input HIGH current ²	V _{CC} = Max, V _{IN} = 2.4V			50	μA
I _I	Input HIGH current at max input voltage	V _{CC} = Max, V _{IN} = 5.5V			1.0	mA
I _{IL}	Input LOW current ²	V _{CC} = Max, V _{IN} = 0.4V			-2.0	mA
I _{OS}	Output short circuit current	V _{CC} = Max, V _{OUT} = OV	-40		-100	mA

NOTES

1. Typical limits are at 25°C and V_{CC} = 5.0V
2. The specified limits reflect one unit load for the family. When more than one load is connected internally, the limits must be multiplied by the number of connected loads. See the INPUT AND OUTPUT LOADING AND FAN-OUT TABLE on the data sheets for the guaranteed limit for each input.

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SCHOTTKY (54S/74S) TTL FAMILY DC CHARACTERISTICS

DC CHARACTERISTICS OVER OPERATING TEMPERATURES (Unless otherwise specified on Data Sheet)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ¹	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL} Input LOW voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V _{CD} Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-0.65	-1.2	V
V _{OL} Output LOW voltage	V _{CC} = Min, I _{OL} = 20mA			0.5	V
V _{OH} Output HIGH voltage	V _{CC} = Min, I _{OH} = -1.0mA	Mil	2.5	3.4	V
		Com	2.7	3.4	V
I _{OH} Output HIGH current (open collector)	V _{CC} = Min, V _{OUT} = 5.5V			250	μA
I _{OZH} Output "off" current HIGH (3-state)	V _{CC} = Max, V _{OUT} = 2.4V, V _{OE} = 2.0V			50	μA
I _{OZL} Output "off" current LOW (3-state)	V _{CC} = Max, V _{OUT} = 0.5V, V _{OE} = 2.0V			-50	μA
I _{IH} Input HIGH current ²	V _{CC} = Max, V _{IN} = 2.7V			50	μA
I _I Input HIGH current at Max input voltage	V _{CC} = Max, V _{IN} = 5.5V			1.0	mA
I _{IL} Input LOW current ²	V _{CC} = Max, V _{IN} = 0.5V			-2.0	mA
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-40		-100	mA

LOW POWER SCHOTTKY (54LS/74LS) FAMILY CHARACTERISTICS

DC CHARACTERISTICS OVER OPERATING TEMPERATURES (Unless otherwise specified on Data Sheet)

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ¹	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V _{IL} Input LOW voltage	Guaranteed input LOW voltage for inputs	Mil		0.7	V
		Com		0.8	V
V _{CD} Input clamp diode voltage	V _{CC} = Min, I _{IN} = -18mA		-0.65	-1.5	V
V _{OL} Output LOW voltage	V _{CC} = Min, I _{OL} = 4.0mA		0.25	0.4	V
	V _{CC} = Min, I _{OL} = 8.0mA (Com. only)		0.35	0.5	V
V _{OH} Output HIGH voltage	V _{CC} = Min, I _{OH} = -400μA	Mil	2.5	3.4	V
		Com	2.7	3.4	V
I _{OH} Output HIGH current (open collector)	V _{CC} = Min, V _{OUT} = 5.5V			100	μA
I _{OZH} Output "off" current HIGH (3-state)	V _{CC} = Max, V _{OUT} = 2.4V, V _{OE} = 2.0V			20	μA
I _{OZL} Output "off" current LOW (3-state)	V _{CC} = Max, V _{OUT} = 0.4V, V _{OE} = 2.0V			-20	μA
I _{IH} Input HIGH current ²	V _{CC} = Max, V _{IN} = 2.7V			20	μA
I _I Input HIGH current at Max input voltage	V _{CC} = Max, V _{IN} = 10V ³			0.1	mA
I _{IL} Input LOW current ²	V _{CC} = Max, V _{IN} = 0.4V			-0.4	mA
I _{OS} Output short circuit current	V _{CC} = Max, V _{OUT} = 0V	-15		-100	mA

NOTES

1. Typical limits are at 25°C and V_{CC} = 5.0V.
2. The specified limits reflect one unit load for the family. When more than one load is connected internally, the limits must be multiplied by the number of connected loads. See the INPUT AND OUTPUT LOADING AND FAN-OUT TABLE on the data sheets for the guaranteed limit for each input.
3. The following LS devices are limited to a 5.5V input breakdown voltage: All inputs of the LS181; clock inputs of LS90, LS92, LS93, LS196, LS197, LS290, LS293, LS390, LS393 and LS490.

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